Common Switch Interface

Common Switch Interface for Fabric Independence and Scalable Switching

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Colin Mick, The Mick Group
Russell Johnson, Power X
Praveen Kumar, XaQti

Presentation Overview

Common Switch Interface

- Introduction
- The Market Issues
- The Technology Issues
- Q & A

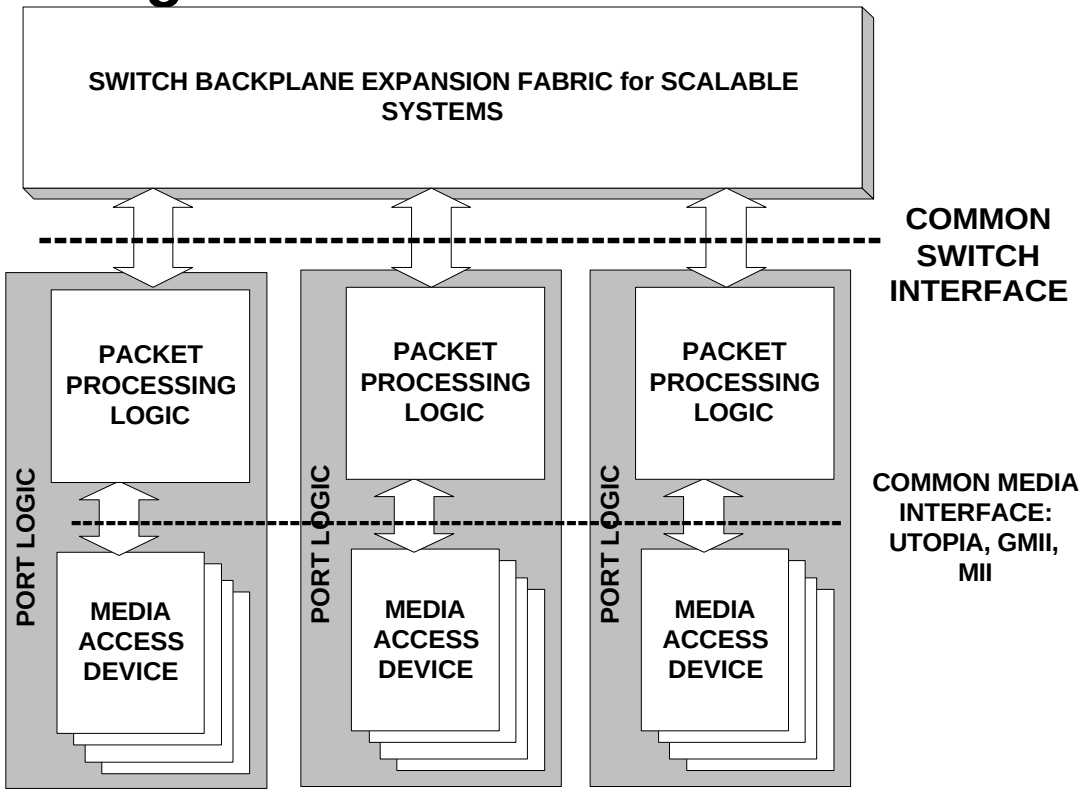
Common Switch Interface

Introduction

- What is CSIX™?
- Project status
- Product status

What is CSIX?

– **CSIX: The Common Switch Interface, is a detailed interface specification between port/packet processor logic and interconnect fabric logic.**



CSIX is the Common Switch Interface

Common Switch Interface

- CSIX is a scalable parallel interface with separate data and control paths
- It is a generic multi-vendor specification to promote the deployment and development of highly scalable network switches
- Permits hardware and software interoperability
- Permits mix and match of interchangeable silicon components, hardware and software
- Concept can be used to expand existing switch architectures: Pt-to-Pt; Shared Memory; Shared Bus

CSIX Interoperability Goals

Common Switch Interface

- **Logical or Message Level**
  - ensure that data or control message protocol exchanged over the interface are properly understood by each end and properly processed by the appropriate function.
- **Interconnection Level**
  - define all the signals with specific functions, meanings, and bit widths, input or output, signal handshake protocols, etc.
- **Physical Level**
  - specify the electrical characteristics such as voltage levels, capacitance, drive strengths, timings etc.

Benefits

- Enables the design of products that can scale from <5 Gbps to 10s of Tbps and from Layer 2 through Layer 3/4+.
- Much lower cost of development for high-speed, high aggregation systems
- Much lower cost of maintaining and operating these new networking systems
- Creates an open and dynamic marketplace for vendors/OEMs with interoperable switch logic and/or fabric expertise
- Dramatic increase in price performance of new network equipment

Common Switch Interface

Current Status

- Project status:
  - **Initial draft of CSIX specification will be released 4Q98**
  - **Target date for completion of the specification is 3Q99.**
- Product status:
  - **First products, based on the first draft of the CSIX interface, will ship in 2Q99.**

Common Switch Interface

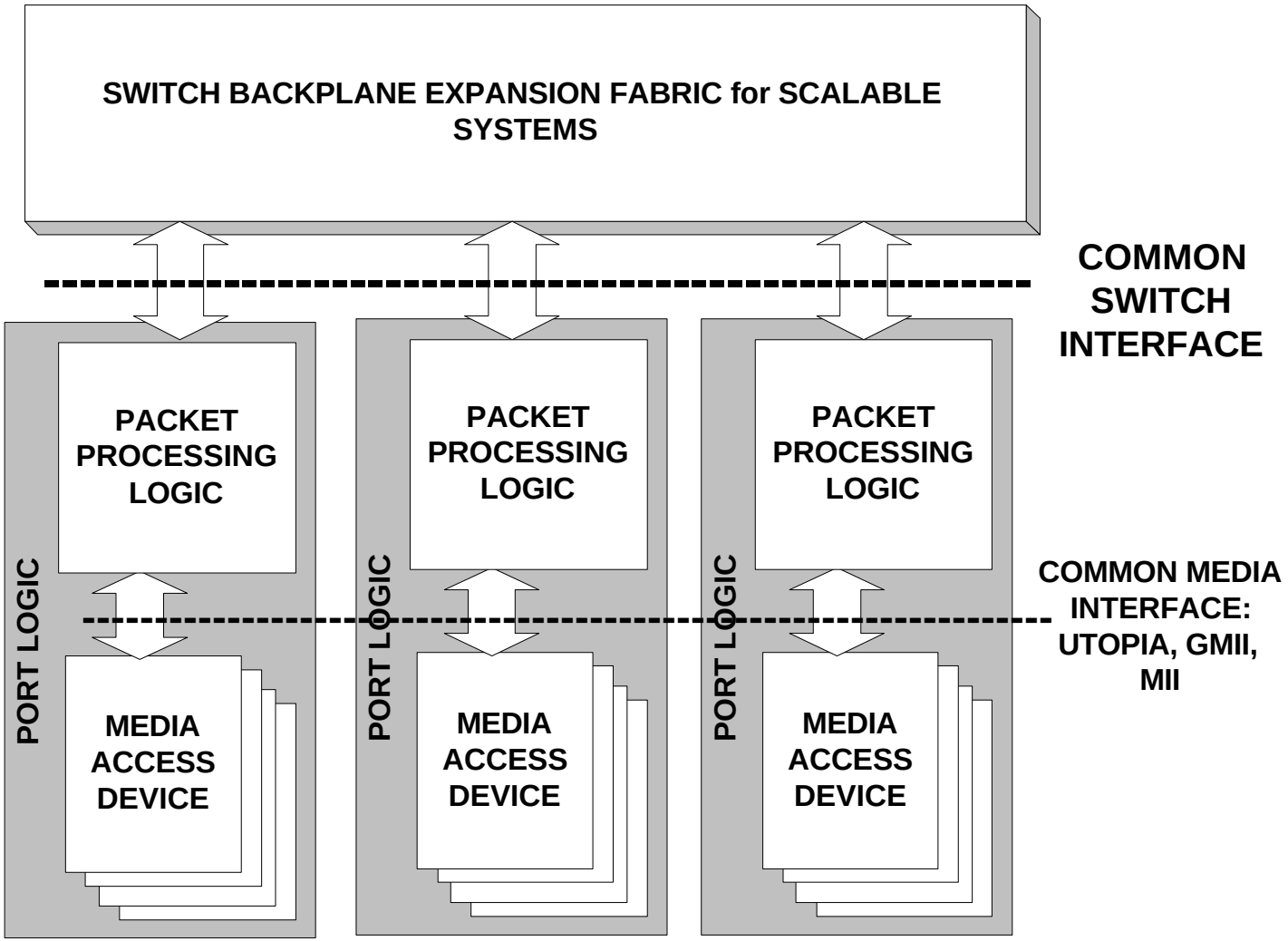
Market Issues

- The changing switch market
- Managing growth
- Evolving switch technology
- Fabric: the point of concentration, where the interconnection happens
- Evolving switch fabric technology
- What does it mean?

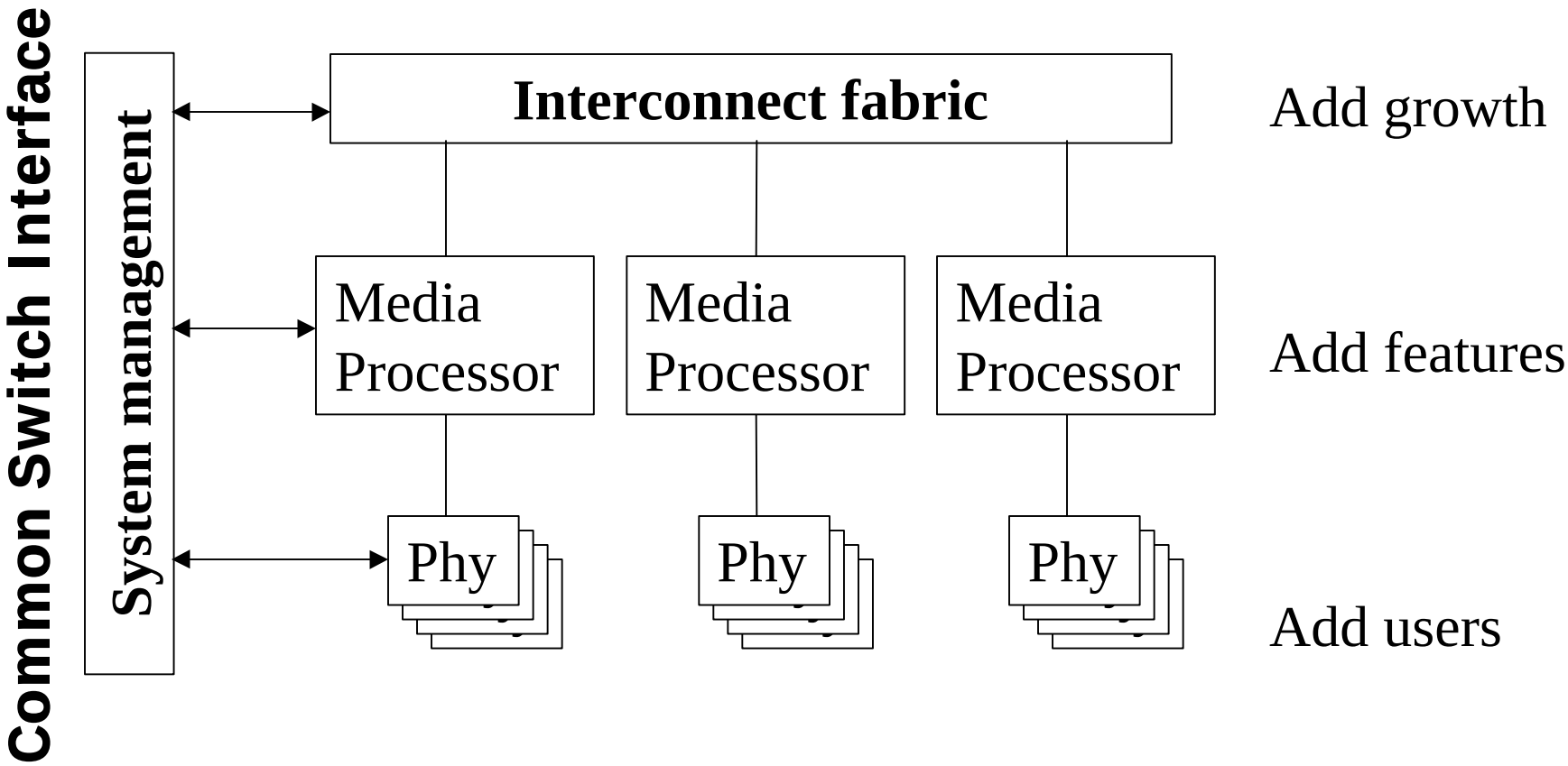
The changing switch market

- **Switch throughput needs to increase due to:**
  - **Increase in port bandwidth (10-> 100->1000->...)**
  - **Increase in number of ports**
- **Demands for QoS and better management capabilities are increasing.**
- **The squeeze**
  - **Increased functionality**
  - **Constrained resources**
    - **Stability, availability, capability**
- **The need for individuality**
  - **Responsiveness, Differentiation, Value add**

Common Switch Interface



Managing growth

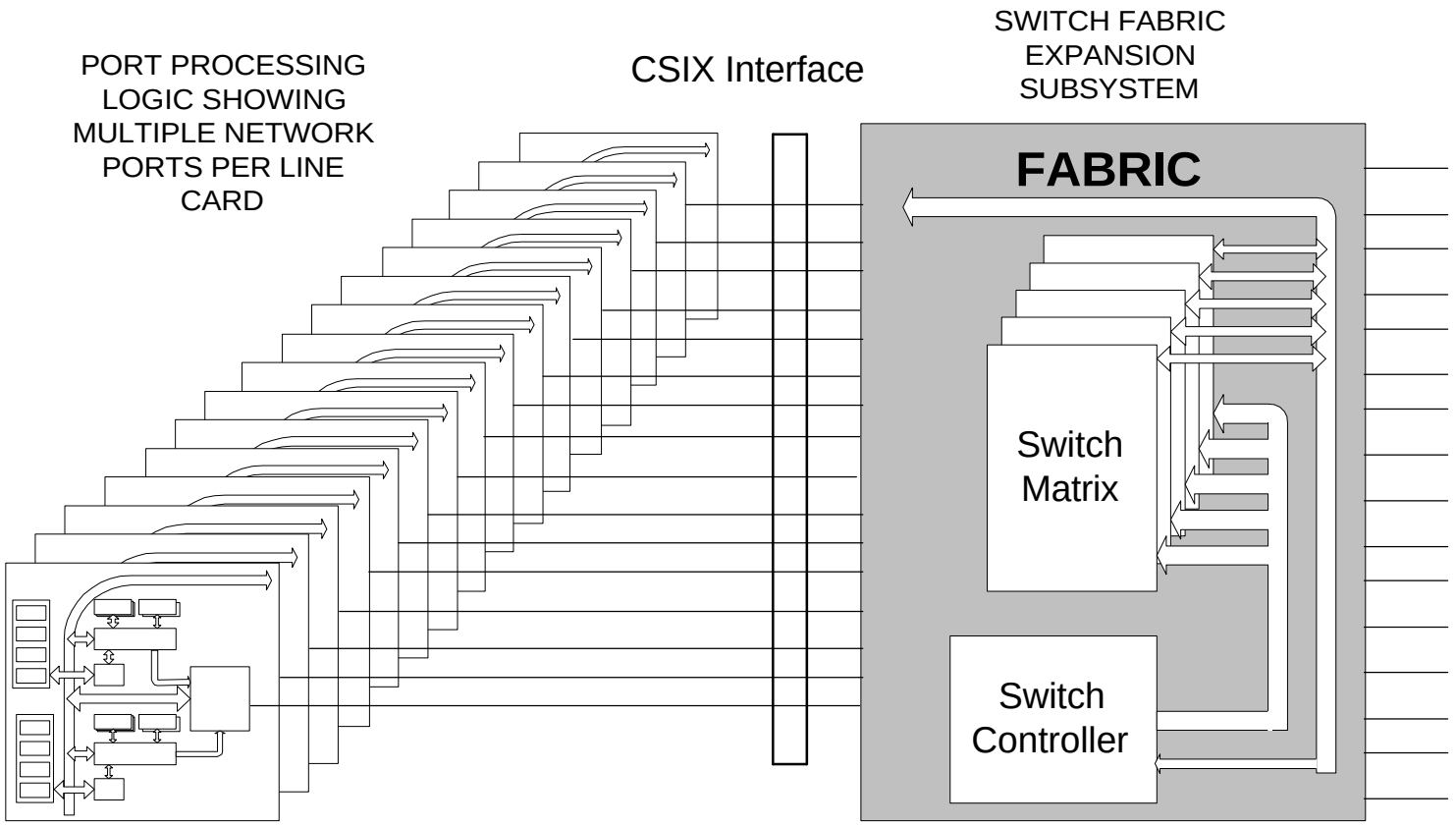


Evolving Switch Technology

Common Switch Interface

- Multiservice and policy based networks
- Soft control of extensive and complex packet processing in hardware before forwarding
- Higher port and bandwidth aggregation increase the density of interconnect fabric hardware
- Efficient scheduling and arbitration across a system of many interconnected ports with guaranteed fairness and QOS
- Increasing Management and Reliability eliminates single point of failure through redundancy.

Fabric: the point of Concentration, where the Interconnection Happens



Evolving Switch Fabric Technology

Common Switch Interface

- **Ability to handle increasing port speeds:**
  - **10, 100, 1000, 2500...**
- **High data density**
  - **Utilization of high speed serial links**
- **Simplicity**
  - **Self Routing Switches**
  - **Buffer management support**
- **Efficiency**
  - **Intelligent Flow control and Congestion handling**
  - **Handling of priorities and QoS issues**
  - **Efficient handling of Multicast**
- **Scalability**

What does it mean?

- Features and functions are added at the media processing layer
- Scalability is added at the fabric layer
- Port and Fabric processing must exchange messages on routing instructions, status, priorities, policies, and service requirements
- We NEED a common electrical and messaging interface to plug the two together

Common Switch Interface

Common Switch Interface

Technical Issues

- CSIX Interfaces
- CSIX Parameters
- Typical Implementation
- CSIX based Systems

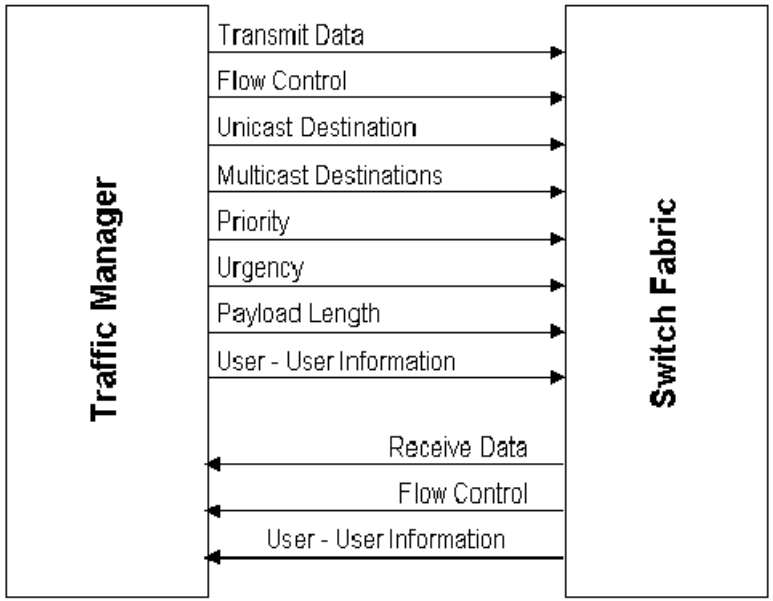
Two Classes of CSIX Interfaces

Common Switch Interface

- **CSIX CLASS A interface supports intelligent switching fabrics with integrated routing.**
  - **requires forwarding and flow control messages to be delivered in line with the data**
- **CSIX CLASS B interface supports non-intelligent switching fabrics**
  - **requires connection scheduling as well as other control messages to be routed to a central or distributed set of intelligent controllers independent of, and in parallel with, the data.**
- **This yields Interoperability within each class**

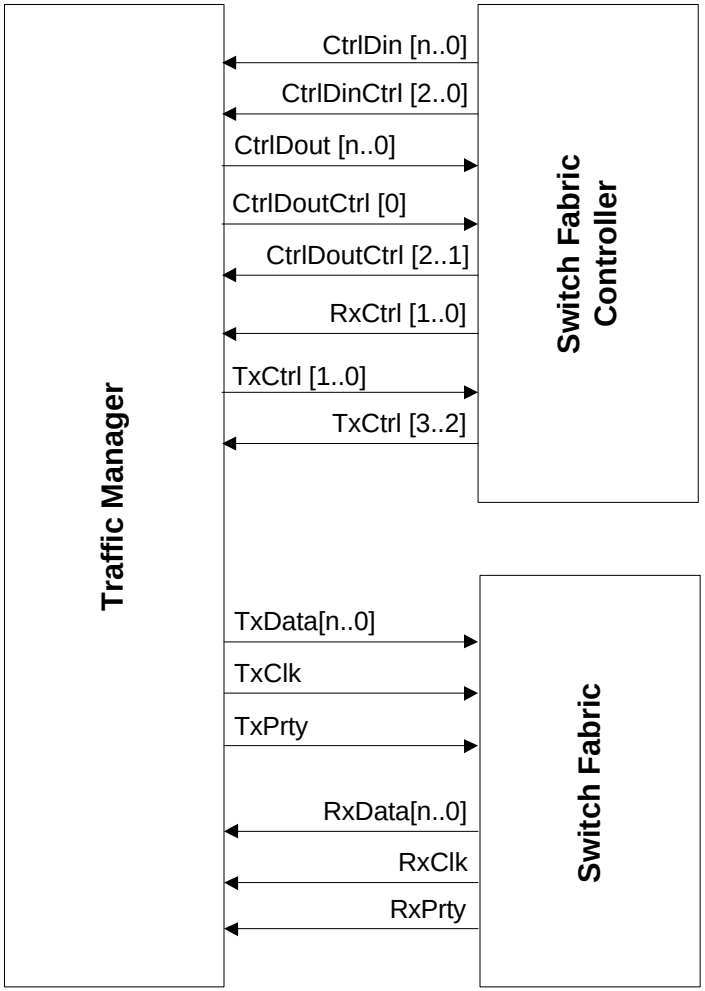
Class A Interface

Common Switch Interface



Class B Interface

Common Switch Interface



Parameters (1)

Common Switch Interface

Clock rate	Up to 100MHz, synchronous or asynchronous to system clock
Data path width	1, 2 or 4 bytes
Packet types	Unicast, multicast-with-mask,multicast-with-ID,broadcast, configuration, user-to-user
Destination addresses	Up to 4096 traffic managers. Sub addressing per traffic manager is supported through user-to-user packets
Priorities	Up to 16 user-definable and configurable priority levels
Urgency	16 levels of urgency within each priority
Header	4 bytes for Class A None on data for Class B

Parameters (2)

Payload	1-256 bytes
Flow Control	In-band for Class A, or through control bus on Class B, per queue, proportional or "pause/resume"
Error management	Parity
Signals	Data(8/16/32), Control (3), Parity (1), Clock (1) in each direction for both Class A and Class B; plus for Class B ControlData(4/8)
Electrical signaling	LVTTL

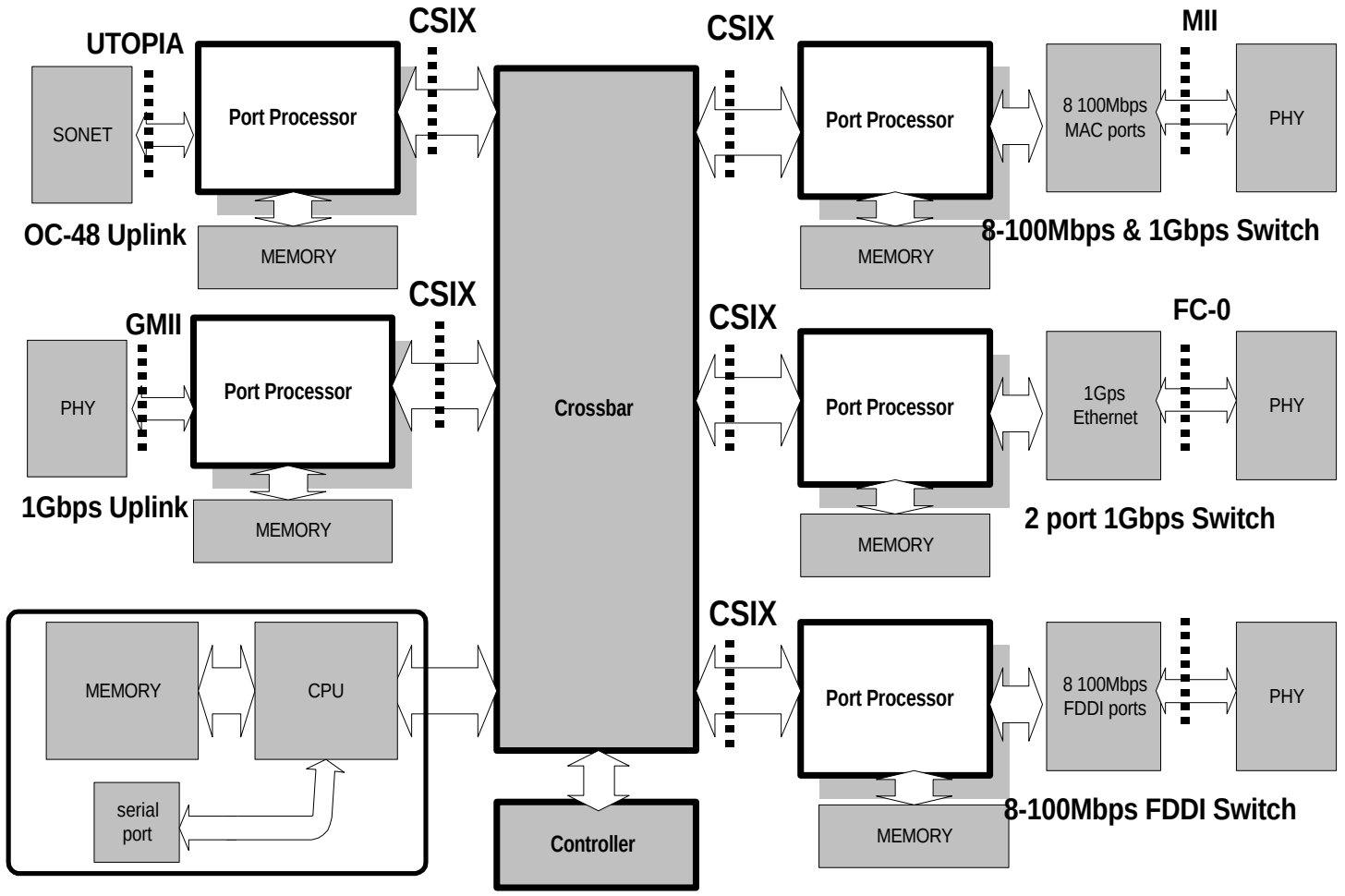
Typical Class A implementation

Common Switch Interface

	Data path (bits)	Packet size (bytes)	Avail. Payload BW	Util. of interface BW	Total pin count
OC-12	8	57	0.74	84%	26
OC-48	32	60	2.83	88%	74
Gigabit Ethernet	16	5-80	>1.3	<75%	42

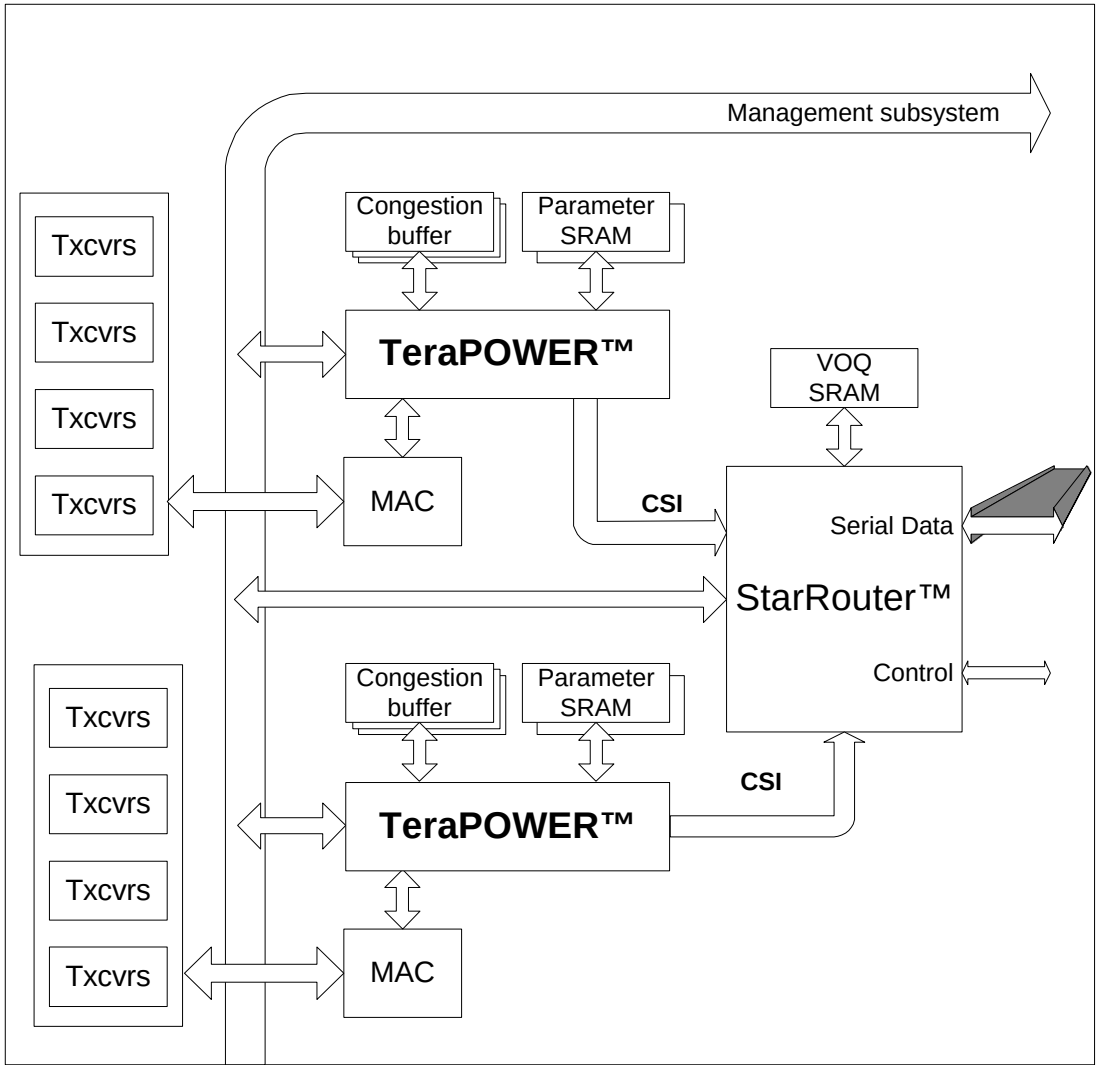
A Scalable Fabric based Switch

Common Switch Interface

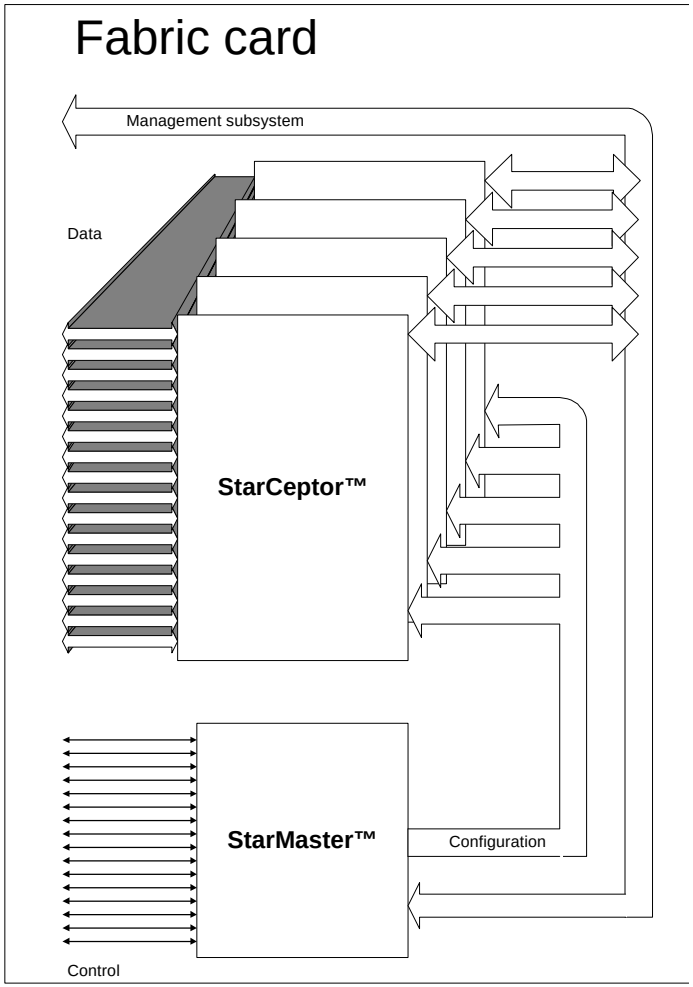


A Switch Line Card

Common Switch Interface



Common Switch Interface Fabric Card



Open Issues

- OC192--pin speed
- Electrical signaling
- Refinement

For more information:

www.csix.org