Delay Histogram Analysis

Paul Hongkyu Jeong
paul.jeong@samsung.com

Geoffrey M. Garner
gmgarner@comcast.net

Eric Hyunsurk Ryu
eric_ryu@samsung.com

SAMSUNG Electronics

IEEE 802.1 A/V Bridge TG
Introduction

- **Worst-case delay has been discussed in IEEE 802 meetings [1-6]**
  - Proposed rule of thumb for rough worst-case delay calculation [2]
  - Some formulas to obtain worst-case delay were presented, along with a mathematical proof given certain assumptions [1], [5]
  - A description was given on how worst-case delay can increase in bunching scenarios [5], [6]
  - Simulation results were presented [2], [3], [4]
- **2 ms is normally considered as acceptable delay bound**
- **The current presentation investigates the frequency of near-worst-case delay (including worst-case delay) and influential factors**
  - **Tools**
    - Cumulative Distribution Function (CDF)
    - Histogram (using sample distribution)
  - **Interesting points**
    - Frequency (or probability) of near-worst-case delay
    - Factor that most influences near-worst-case delay
Purpose of Present Simulation Work

- Find the factor that most influences an increase in end-to-end delay
  - Utilization
  - Frame Size
  - Forwarding technique
  - Traffic pattern
  - Number of streams
  - Topology

- Compare the frequency (or probability) of Ethernet frame errors (obtained from link BER) and near-worst-case delay

- Compare delay bounds between conventional method and just forwarding method
  - Detailed description will be given in slide 13
BER Calculation in Ethernet Link

- **Assumptions**
  - Ethernet BER (BER is in the range $10^{-8}$ to $10^{-12}$)
    - $10^{-8}$: 100BASE-T4 in 802.3 (Clause 23.1.2)
    - $10^{-12}$: 1000BASE-X in 802.3 (Clause 36.1.2)
  - Ethernet size (except preamble)
    - Minimum: 64 bytes (= 512 bits)
    - Maximum: 1518 bytes (= 12144 bits)
  - Poisson error process
  - Number of links from sender to receiver in a topology (at slide 6): 9 links

- **Calculation (Maximum Ethernet size case)**
  - **BER 1e-8**
    - 1518 byte Maximum size frame → $10^{-3}$
    - 246 Byte TS stream case → $1.7 \times 10^{-4}$
    - 56 byte minimum frame → $4 \times 10^{-5}$
  - **BER 1e-12**
    - 1518 byte Maximum size frame → $10^{-7}$
    - 246 byte TS stream case → $1.7 \times 10^{-8}$
    - 56 byte minimum frame → $4 \times 10^{-9}$
Simulation Scenarios

- All sources are time sensitive, CBR traffic with nominal rates set to produce desired link utilization
- Sources have various different frequency offsets that are all within ±100ppm
- 7 switch to switch hops
- 100 Mbps link bandwidth
- 9 traffic sources
- Packet size (1526 bytes/ 763 bytes/ 382 bytes/ 191 bytes including Ethernet header and FCS)
  - Switch to switch link utilization ≈ 30%, 50%, 70%, 100%
  - Ethernet Inter-Frame Gap (IFG) (i.e. 12 bytes) is applied to link utilization calculation
  - Exact description of 100% utilization: 99.76%/ 99.99%/ 99.53%/ 99.93% for each
- Source start time of each source is ideally configured to show worst case delay
- Description of network topology 1
  - 3 sources at first switch (nodes 1 – 3)
  - Traffic from 2 of these sources go to final switch (nodes 16 and 18)
  - Traffic from 3rd source (node 3) is dropped at 2nd switch
  - At switches 2 – 7 (nodes 20 – 25 in figure), traffic added from single CBR source, carried 1 hop, and dropped
Simulation Scenarios (Cont.)

Achieved simulation results

- delay CDF and histogram (using sample distribution)
- results given for node 18
- dashed line in each CDF corresponds to $10^{-4}$ exceedance probability (i.e., 99.99 percentile)
Topology
Scenario 1 - 1526 bytes

At least under 1e-4

2ms
Scenario 2 - 763 bytes

- 763Byte Util. 30% CDF Node 18
- At least under 1e-4

- 763Byte Util. 50% CDF Node 18
- At least under 1e-4

- 763Byte Util. 70% CDF Node 18
- At least under 1e-4

- 763Byte Util. 100% CDF Node 18
- At least under 1e-4

- 763Byte Util. 30% Histogram Node 18
- 1ms

- 763Byte Util. 50% Histogram Node 18
- 1ms

- 763Byte Util. 70% Histogram Node 18
- 1ms

- 763Byte Util. 100% Histogram Node 18
- 1ms
Scenario 3 - 382 bytes

CDF
Node 18

At least under 1e-4

CDF
Node 18

At least under 1e-4

CDF
Node 18

At least under 1e-4

CDF
Node 18

At least under 1e-4

Histogram
Node 18

At least under 1e-4

Histogram
Node 18

At least under 1e-4

Histogram
Node 18

At least under 1e-4

500us

500us

500us

500us

440us

520us

500us

500us

500us

500us
Scenario 4 - 191 bytes

CDF Node 18

191 Byte Util. 30%

At least under 1e-4

191 Byte Util. 50%

At least under 1e-4

191 Byte Util. 70%

At least under 1e-4

191 Byte Util. 100%

At least under 1e-4

200us

Histogram Node 18

200us

200us

200us
Delay Upper Bound

- Frame size has significant impact on delay upper bound
  - Utilization has much less impact

Delay upper bound is under 2ms
Delay Upper Bound (cont.)

- Worst-case delay bound (of ranged area under 1e-4 probability) when small and big size frames are simultaneously transmitted to switches
  - Necessary delay of maximum size frame (i.e. 1526 bytes) when it pass over 7 hop switches: 122.08 us (tx_delay) + (122.08 us + 2 us (proc_delay)) * 8 = 1.11 ms
  - Additional delay (i.e. delay by buffering) of maximum size frame at 100% utilization: 1.84 ms – 1.11 ms = 0.73 ms
  - 191 bytes case: necessary delay is 0.15 ms, so worst-case delay bound is 0.15 ms + 0.73 ms = 0.88 ms
  - 382 bytes case: necessary delay is 0.29 ms, so worst-case delay bound is 0.29 ms + 0.73 ms = 1.02 ms
  - 763 bytes case: necessary delay is 0.56 ms, so worst-case delay bound is 0.56 ms + 0.73 ms = 1.29 ms
  - 1526 bytes case: worst-case delay bound is the same as 1.84 ms

(Chart: Delay bound range vs. Size [bytes])
For the AV stream and real-time applications

- We may not need to perform a CRC check on the whole frame since an errored frame need not be retransmitted.

**Proposed Ethernet Frame**

- **Preamble**: 7 bytes
- **Start of frame delimiter**: 1 byte
- **Destination Address**: 6 bytes
- **Source Address**: 6 bytes
- **Type or Length**: 2 bytes
- **Data (Payload)**: 46~1500 bytes
- **CRC**: 4 bytes

**A/V Bridge**

1. Processing header information (After receiving part of header)
2. Scheduling
3. Transmission

**Buffering until transmission**
The delay enhancement with that approach

- **Performance expectation**
  - Assumption: In a single switch/ No buffered frame
  - Major factors influencing at switch
    - Transmission delay: depends on frame size
    - Processing delay: under 2 usec
  - Minimum size cases (of Fast Ethernet); 64 byte
    - Store and forward: 2 usec + 5.12 usec = 7.12 usec
      - Transmit only correct frame
    - Cut-through (based on having to buffer 22 bytes): 1.76 usec + 2 usec = 3.76 usec
      - Transmit all frames without checking error
    - Check the header error case (based on having to buffer 24 bytes): 1.92 usec + 2 usec = 3.92 usec
      - Transmit only frames with correct header
        (44% delay reduction compared to store and forward method)
  - Maximum size cases (of Fast Ethernet); 1526 byte
    - Store and forward: 122.08 usec + 2 usec = 124.08 usec
    - Cut-through: 1.76 usec + 2 usec = 3.76 usec
    - Check the header error case: 1.92 usec + 2 usec = 3.92 usec
      (97% delay reduction per hop compared to store and forward method)
Simulation Scenarios

- All sources are time sensitive, CBR traffic with nominal rates set to produce desired link utilization
- Sources have various different frequency offsets that are all within ±100 ppm
- 7 switch to switch hops
- 100 Mbps link bandwidth
- 9 traffic sources
- Packet size (1526 bytes including Ethernet header and FCS)
  - Switch to switch link utilization ≈ 30%, 50%, 70%, 100%

- Description of network topology 1
  - 3 sources at first switch (nodes 1 – 3)
  - Traffic from 2 of these sources go to final switch (nodes 16 and 18)
  - Traffic from 3rd source (node 3) is dropped at 2nd switch
  - At switches 2 – 7 (nodes 20 – 25 in figure), traffic added from single CBR source, carried 1 hop, and dropped

- Achieved simulation results
  - delay of CDF and histogram (using sample distribution)
  - results given for node 18
Scenario - 1526 bytes

At least under 1e-4

0.8ms

1ms

1ms

1ms

1ms

1ms
Transition of Delay Distribution Shape

- Case: Size 1526 bytes and utilization 70%

<table>
<thead>
<tr>
<th>Util (%)</th>
<th>Conventional</th>
<th>Just forwarding</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>1.64 ms</td>
<td>0.88 ms</td>
</tr>
<tr>
<td>50</td>
<td>1.76 ms</td>
<td>1.30 ms</td>
</tr>
<tr>
<td>70</td>
<td>1.79 ms</td>
<td>1.31 ms</td>
</tr>
<tr>
<td>100</td>
<td>1.84 ms</td>
<td>1.44 ms</td>
</tr>
</tbody>
</table>

In the just forwarding case, the 99.99 percentile was reduced by 0.4 – 0.8 ms
Conclusion

- Frame error rate in end-to-end links with given assumptions are
  - $1e^{-3}$; when Ethernet link BER is $1e^{-8}$
  - $1e^{-7}$; when Ethernet link BER is $1e^{-12}$

- Simulation results of scenario 1 to 4 show that every case within acceptable delay bound range (equal or bigger than $1 - 1e^{-4}$ probability) do not exceed 2ms, acceptable delay bound
  - Probability (or area) of delay longer than 1.84 ms is less than $1e^{-4}$ even in the case of 1526 byte and 100% utilization (which is worst scenario)

- If we just forward Ethernet frame not having header error, we may reduce end-to-end link delay by 0.4 – 0.8 ms

- Most influential factors are frame size and forwarding method in this study environment

- Studying impact of traffic pattern, number of stream and topology change can be future works
Reference


