IEEE 802.1AS
Time Sync Interface

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Application

• A time-aware bridged network can synchronize all of the nodes to a grand master, but...

• How does the grand master get its time reference; and

• What do the slave nodes do with their synchronized time?
Deployment

• Grand master devices require some kind of time input.
• Slave devices may require some kind of time output.
• All end stations must be grand master capable.
• Most bridges should be grand master capable.
I/O Requirements

- Low pin count
- Simple
- Precise
- Master (input) and slave (output) operation
I/O Requirements (2)

• Syncs both frequency and phase (time of day)
• Low-frequency, single-ended signaling
• Implementable using low-cost FPGAs
Mode

- Free-running
  - Device that has time reference constantly drives time values across the interface
- It is presumed that a single CPU can communicate directly or indirectly to both devices on either side of the time sync interface (minimizing the interface’s functional requirements)
Signals

- heartbeat (8 KHz)
- bit_clock (1 MHz–5 MHz)
- time_code (serial data)
Signal: heartbeat

- 8 KHz continuous square wave
- Convenient, telecom-friendly frequency
- Rising edge used as sync point
- Time stamps of heartbeat taken at sync point
Signal: bit_clock

- Synchronous to heartbeat
- May be set to any useful frequency between 1 MHz and 5 MHz.
- Used to shift bits on time_code
Signal: time_code

- synchronous to bit_clock
- presents time stamp from preceding rising edge of heartbeat
- Conveys: epoch[15:0], seconds[31:0], nanoseconds[31:0], lock and clock_quality[7:0], crc[7:0]
Further Issues

• 6 pins or 3 pins?
• Two unidirectional interfaces or one bidirectional interface?
• Additional functionality or signaling?
• Master/slave indications and/or negotiations?