Common Public Radio Interface

CPRI overview Input requirements for CPRI

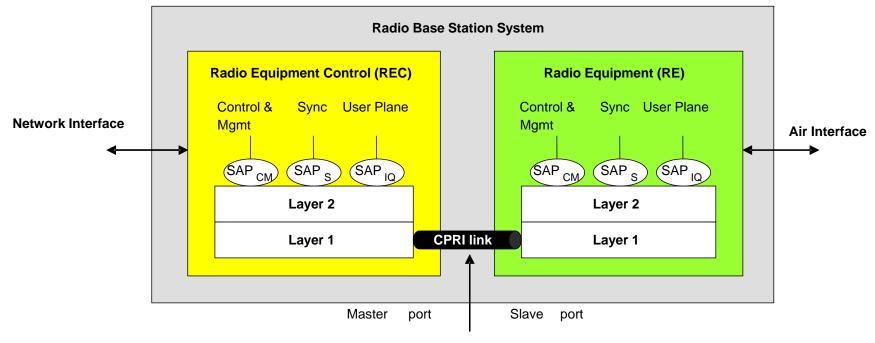
Some history

- Industrial cooperation jointly created by 5 parties:
 - Ericsson,
 - Huawei,
 - NEC,
 - Nortel Networks,
 - Siemens Mobile
- Provide a framework to facilitate Radio Equipment products development for mobile telecommunications systems
- CPRI specification V1.0 published in 2003

CPRI Basic System Architecture

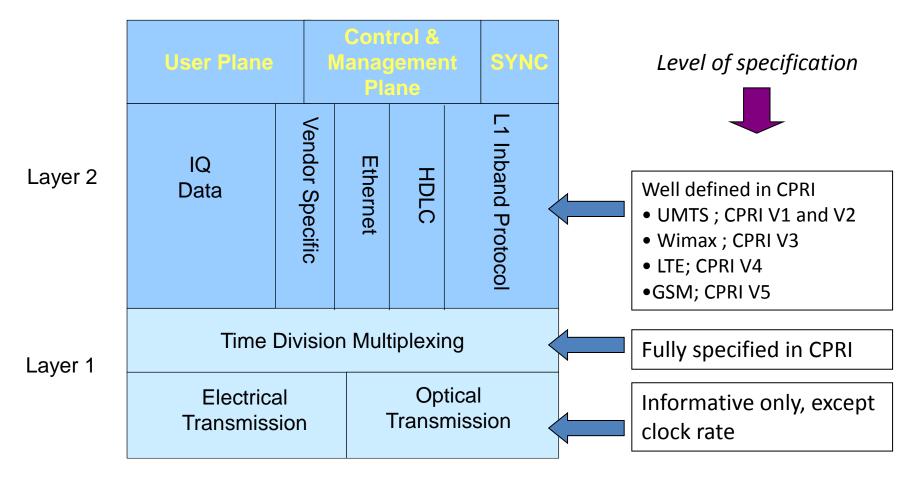
- Based on a Radio Base Station architecture dividing the Radio Base Station into a radio part and a control part
- CPRI specification defines the Radio Base Station internal interface between these two parts
- Simple
- Flexible

CPRI Basic System Architecture



Common Public Radio Interface

CPRI Protocol Stack



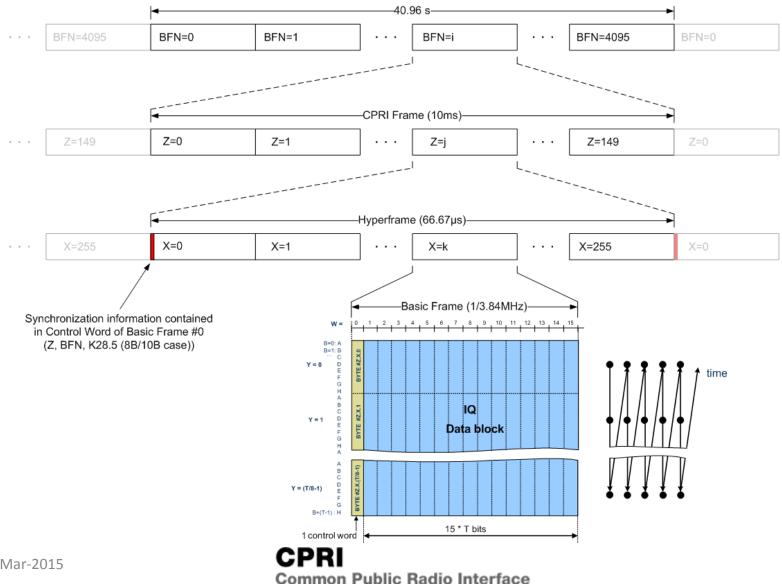
CPRI

Common Public Radio Interface

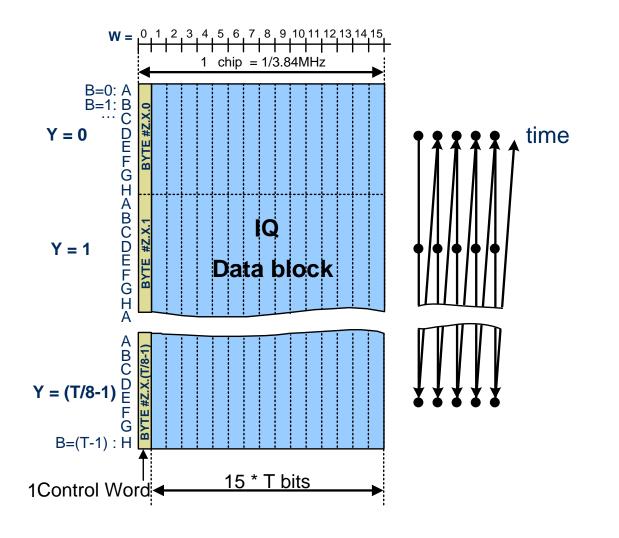
CPRI Main Characteristics

- Bit synchronous interface
- Symmetrical serial data link between REC and RE
- Steady data stream, "Always one"
- Time Division Multiplexing (TDM) of Antenna data streams in form of In-phase (I) and Quadrature (Q) Samples
- Embedded Ethernet or HDLC streams (C&M plane data)
- BER=10⁻¹²

CPRI Frame Structure



CPRI Basic Frame



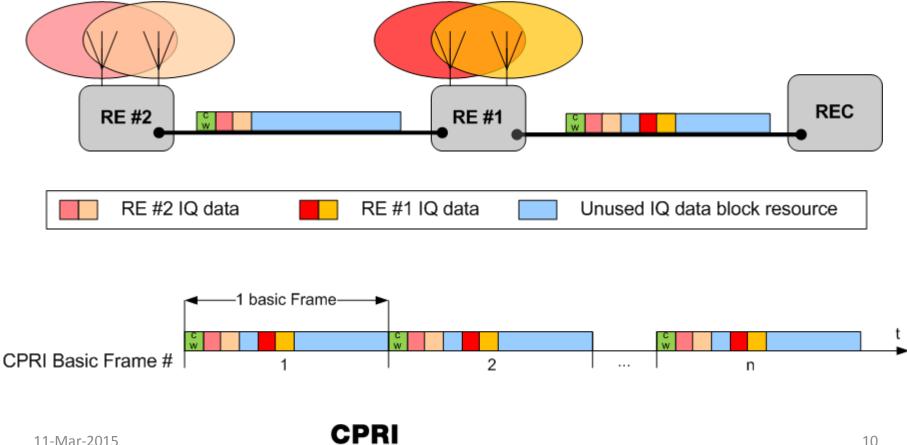
CPRI Common Public Radio Interface

CPRI Control Word usage

- 1/16 of the available CPRI bandwidth
 - Synchronization and Timing
 - Fast and/or Slow C&M channel
 - Low level link control (LOS/LOF/...)
 - Vendor Specific
 - Fast Real Time Control

CPRI Transport Capacity allocation

« static » allocation of the IQ data block resource



Common Public Radio Interface

CPRI Line Bit Rate Options and User-Plane Transport Capacity

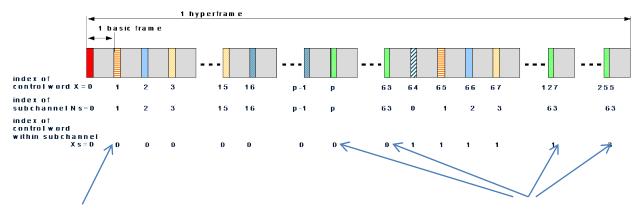
Line bit rate	Line Coding	Transport Capacity (#WCDMA AxC)	Transport Capacity (# 20 MHz LTE AxC)
614.4 Mbit/s	8B/10B	4	/ \
1228.8 Mbit/s	8B/10B	8	/ 1 \
2457.6 Mbit/s	8B/10B	16	2
3072.0 Mbit/s	8B/10B	20	2
4915.2 Mbit/s	8B/10B	32	4
6144.0 Mbit/s	8B/10B	40	5
8110.08 Mbit/s	64B/66B	64	8 1
9830.4 Mbit/s	8B/10B	64	8
10137.6 Mbit/s	64B/66B	80	10
12165.12 Mbit/s	64B/66B	96	12/

Each 20MHz LTE AxC stream requires ~1Gbps!

CPRI Common Public Radio Interface

C&M-Plane Transport

Line bit rate	Maximum Slow C&M Bitrate [Mbit/s]	Maximum Fast C&M Bitrate [Mbit/s]
614.4 Mbit/s	0.48	21.12
1228.8 Mbit/s	0.96	42.24
2457.6 Mbit/s	1.92	84.48
3072.0 Mbit/s	2.4	105.6
4915.2 Mbit/s	3.84	168.96
6144.0 Mbit/s	4.8	211.2
>=8110.08 Mbit/s	7.68	337.92



CPRI Slow C&M channel transported in CW of second CPRI basic frame of each Hyperframe

CPRI fast C&M channel transported in CWs of Basic frame with number p, p+1,..,63,64+p...127, 128+p...191, p+192,...,255 (p-pointer configurable from 16 ... 63)

11-Mar-2015

CPRI

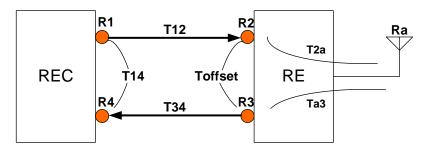
Common Public Radio Interface

Synchronization and Timing

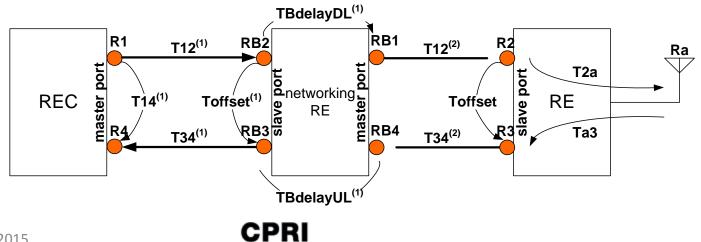
- Slave port side recovers the clock signal from the incoming serial bit stream (slave port "locked" to master port clock).
- Sync Control Word marks the start of a Hyperframe
- Time information (BFN, HFN) is obtained from specific control words
- Cable Delay calibration process delivers one-way delay values (T12 and T34 respectively) (assumes symmetrical cable delay values)

CPRI Delays

• Single hop configuration



• Multi hop configuration



CPRI documents

- CPRI specification
 - section 4 : defines mandatory and optional parts of the CPRI specification
 - Annex A: Specification details
 - Informative and normative sections
 - Scrambling (Normative)
 - 64B/66B line coding (Normative)
 - Delay Calibration Example (Informative)
 - Electrical Physical Layer Specification (Informative)
 - Networking (Informative)
 - E-UTRA /GSM sampling rates (Informative)

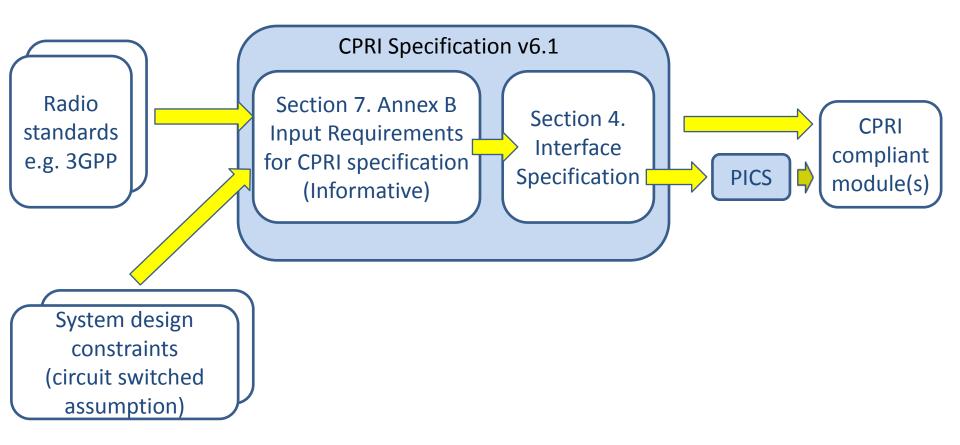
CPRI documents

- CPRI specification
 - Annex B: Input Requirements for the CPRI Specification (Informative)
 - Used for the development of the CPRI specification
 - Requirements to be met by the CPRI specification and used as a baseline for future enhancements of the CPRI specification
 - Does not specify the requirements on a CPRI compliant device

CPRI documents

- Protocol Implementation Conformance Statement (PICS)
 - Lists of CPRI capabilities and options implemented
 - Interoperability
 - Implementation, test and verification

Relation between "input requirements" and "interface specification"



- Timing and Synchronization relevant excerpt:
 - Max. Frequency Error contribution: 0.002ppm
 - Max. Bit Error Ratio:
 - Link delay accuracy:
 - Max. round trip delay (excl. cable): 5µs

 10^{-12}

 $\pm T_{c}/32$

- R-17, R-18, R-18A: Frequency Synchronization
 - Requirement were written to provide a clean clock reference for the RE, the total frequency error budget being 50 ppb for RNC -> BASE Station -> Radio Equipment.

- R-19, R-20 R-21, R-21A: Delay accuracy
 - These requirements are driven by 3GPP specifications

Feature	Timing accuracy	Source
UTRA-FDD Tx Diversity UTRA-FDD MIMO	+/- 32.5 ns	3GPP TS 25.104
E-UTRA TDD	+/- 1.5us	3GPP TS 36.133
E-UTRA Tx Diversity E-UTRA MIMO	+/- 32.5 ns	3GPP TS 36.104
E-UTRA Intra-band contiguous Carrier Aggregation	+/- 65 ns	3GPP TS 36.104
UTRA RTT	+/- 130 ns	3GPP TS 25.133

- R-26: Maximum Delay
 - In order to have maximum signal processing time, the transport latency of the antenna data shall be minimized

- R-27: Bit Error Ratio
 - This requirement is to define signal quality transport, the reason is to avoid FEC for this rate to minimize delay and cost

Thank You

Time for questions



