Common Public Radio Interface

CPRI overview
Input requirements for CPRI
Some history

• Industrial cooperation jointly created by 5 parties:
  – Ericsson,
  – Huawei,
  – NEC,
  – Nortel Networks,
  – Siemens Mobile

• Provide a framework to facilitate Radio Equipment products development for mobile telecommunications systems

• CPRI specification V1.0 published in 2003
CPRI Basic System Architecture

• Based on a Radio Base Station architecture dividing the Radio Base Station into a radio part and a control part
• CPRI specification defines the Radio Base Station internal interface between these two parts
• Simple
• Flexible
CPRI Basic System Architecture

Radio Base Station System

Radio Equipment Control (REC)
- Control & Mgmt
  - SAP_CM
  - SAP_S
  - SAP_Q
- Sync
- User Plane

Radio Equipment (RE)
- Control & Mgmt
  - SAP_CM
  - SAP_S
  - SAP_Q
- Sync
- User Plane

Layer 1
Layer 2

Network Interface
Air Interface

Common Public Radio Interface

Master port Slave port
CPRI Protocol Stack

Layer 1
- Time Division Multiplexing
- Electrical Transmission
- Optical Transmission

Layer 2
- IQ Data
- Vendor Specific
- Ethernet
- HDLC
- L1 Inband Protocol

Control & Management Plane

User Plane

SYNC

Level of specification
- Well defined in CPRI
  - UMTS; CPRI V1 and V2
  - WiMax; CPRI V3
  - LTE; CPRI V4
  - GSM; CPRI V5
- Fully specified in CPRI
- Informative only, except clock rate
CPRI Main Characteristics

• Bit synchronous interface
• Symmetrical serial data link between REC and RE
• Steady data stream, ”Always one”
• Time Division Multiplexing (TDM) of Antenna data streams in form of In-phase (I) and Quadrature (Q) Samples
• Embedded Ethernet or HDLC streams (C&M plane data)
• BER=10^{-12}
CPRI Frame Structure

- **BFN**: Digitized sampling frame
- **Z**: Basic frame number
- **X**: Combination of Z and BFN

- **BFN=0**: Frame start
- **BFN=1**: Frame middle
- **BFN=i**: Frame end

- **Z=0**: Frame start
- **Z=1**: Frame middle
- **Z=j**: Frame end
- **Z=149**: Frame start (next cycle)

- **X=255**: Frame start
- **X=0**: Frame end
- **X=k**: Frame middle

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**Synchronization information contained in Control Word of Basic Frame #0**
(Z, BFN, K28.5 (8B/10B case))

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**Basic Frame (1/3.84MHz)**

- **IQ Data block**
- **15 * T bits**
- **1 control word**

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CPRI Basic Frame

1 Control Word

15 * T bits

IQ Data block

Y = (T/8 - 1)

Y = 1

Y = 0

B = (T-1)

B = 1:

B = 0:

W = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

1 chip = 1/3.84MHz

1 chip = 1/3.84MHz

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CPRI Control Word usage

• 1/16 of the available CPRI bandwidth
  – Synchronization and Timing
  – Fast and/or Slow C&M channel
  – Low level link control (LOS/LOF/...)
  – Vendor Specific
  – Fast Real Time Control
CPRI Transport Capacity allocation

- « static » allocation of the IQ data block resource
CPRI Line Bit Rate Options and User-Plane Transport Capacity

<table>
<thead>
<tr>
<th>Line bit rate</th>
<th>Line Coding</th>
<th>Transport Capacity (#WCDMA AxC)</th>
<th>Transport Capacity (# 20 MHz LTE AxC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>614.4 Mbit/s</td>
<td>8B/10B</td>
<td>4</td>
<td>--</td>
</tr>
<tr>
<td>1228.8 Mbit/s</td>
<td>8B/10B</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>2457.6 Mbit/s</td>
<td>8B/10B</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>3072.0 Mbit/s</td>
<td>8B/10B</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>4915.2 Mbit/s</td>
<td>8B/10B</td>
<td>32</td>
<td>4</td>
</tr>
<tr>
<td>6144.0 Mbit/s</td>
<td>8B/10B</td>
<td>40</td>
<td>5</td>
</tr>
<tr>
<td>8110.08 Mbit/s</td>
<td>64B/66B</td>
<td>64</td>
<td>8</td>
</tr>
<tr>
<td>9830.4 Mbit/s</td>
<td>8B/10B</td>
<td>64</td>
<td>8</td>
</tr>
<tr>
<td>10137.6 Mbit/s</td>
<td>64B/66B</td>
<td>80</td>
<td>10</td>
</tr>
<tr>
<td>12165.12 Mbit/s</td>
<td>64B/66B</td>
<td>96</td>
<td>12</td>
</tr>
</tbody>
</table>

Each 20MHz LTE AxC stream requires ~1Gbps!
# C&M-Plane Transport

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>614.4 Mbit/s</td>
<td>0.48</td>
<td>21.12</td>
</tr>
<tr>
<td>1228.8 Mbit/s</td>
<td>0.96</td>
<td>42.24</td>
</tr>
<tr>
<td>2457.6 Mbit/s</td>
<td>1.92</td>
<td>84.48</td>
</tr>
<tr>
<td>3072.0 Mbit/s</td>
<td>2.4</td>
<td>105.6</td>
</tr>
<tr>
<td>4915.2 Mbit/s</td>
<td>3.84</td>
<td>168.96</td>
</tr>
<tr>
<td>6144.0 Mbit/s</td>
<td>4.8</td>
<td>211.2</td>
</tr>
<tr>
<td>&gt;=8110.08 Mbit/s</td>
<td>7.68</td>
<td>337.92</td>
</tr>
</tbody>
</table>

**CPRI Slow C&M** channel transported in CW of second CPRI basic frame of each Hyperframe

**CPRI fast C&M** channel transported in CWs of Basic frame with number p, p+1,...,63,64+p...127, 128+p...191, p+192,...,255 (p-pointer configurable from 16 ... 63)
Synchronization and Timing

• Slave port side recovers the clock signal from the incoming serial bit stream (slave port “locked” to master port clock).
• Sync Control Word marks the start of a Hyperframe
• Time information (BFN, HFN) is obtained from specific control words
• Cable Delay calibration process delivers one-way delay values (T12 and T34 respectively) (assumes symmetrical cable delay values)
CPRI Delays

- Single hop configuration

- Multi hop configuration
CPRI documents

• CPRI specification
  – section 4: defines mandatory and optional parts of the CPRI specification
  – Annex A: Specification details
    • Informative and normative sections
      – Scrambling (Normative)
      – 64B/66B line coding (Normative)
      – Delay Calibration Example (Informative)
      – Electrical Physical Layer Specification (Informative)
      – Networking (Informative)
      – E-UTRA /GSM sampling rates (Informative)
CPRI documents

• CPRI specification
  – Annex B: Input Requirements for the CPRI Specification (Informative)
    – Used for the development of the CPRI specification
    – Requirements to be met by the CPRI specification and used as a baseline for future enhancements of the CPRI specification
    – Does not specify the requirements on a CPRI compliant device
CPRI documents

• Protocol Implementation Conformance Statement (PICS)
  – Lists of CPRI capabilities and options implemented
  – Interoperability
  – Implementation, test and verification
Relation between “input requirements” and “interface specification”
Input Requirements for CPRI

• Timing and Synchronization relevant excerpt:
  – Max. Frequency Error contribution: 0.002ppm
  – Max. Bit Error Ratio: $10^{-12}$
  – Link delay accuracy: $\pm T_C/32$
  – Max. round trip delay (excl. cable): 5$\mu$s
Input Requirements for CPRI

• R-17, R-18, R-18A: Frequency Synchronization
  – Requirement were written to provide a clean clock reference for the RE, the total frequency error budget being 50 ppb for RNC -> BASE Station -> Radio Equipment.
Input Requirements for CPRI

- R-19, R-20 R-21, R-21A: Delay accuracy
  - These requirements are driven by 3GPP specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Timing accuracy</th>
<th>Source</th>
</tr>
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<tbody>
<tr>
<td>UTRA-FDD Tx Diversity</td>
<td>+/- 32.5 ns</td>
<td>3GPP TS 25.104</td>
</tr>
<tr>
<td>UTRA-FDD MIMO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E-UTRA TDD</td>
<td>+/- 1.5us</td>
<td>3GPP TS 36.133</td>
</tr>
<tr>
<td>E-UTRA Tx Diversity E-UTRA MIMO</td>
<td>+/- 32.5 ns</td>
<td>3GPP TS 36.104</td>
</tr>
<tr>
<td>E-UTRA Intra-band contiguous Carrier Aggregation</td>
<td>+/- 65 ns</td>
<td>3GPP TS 36.104</td>
</tr>
<tr>
<td>UTRA RTT</td>
<td>+/- 130 ns</td>
<td>3GPP TS 25.133</td>
</tr>
</tbody>
</table>
Input Requirements for CPRI

• R-26: Maximum Delay
  – In order to have maximum signal processing time, the transport latency of the antenna data shall be minimized
Input Requirements for CPRI

• R-27: Bit Error Ratio
  – This requirement is to define signal quality transport, the reason is to avoid FEC for this rate to minimize delay and cost
Thank You

Time for questions