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802.1Qcr Updates

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General

Administrative

- Prepare a "skeleton"-draft for Atlanta in January 2017
 - Based on the last Qbv draft framemaker files
 - Structure and sections for the planned contents, find the appropriate places
 - Editor's notes describing outlining the contents
 - Integrate some existing figures

Technical

- Consecutive slides sketch the intended technical content planned right now
- Stay high level the author believes that detailed technical discussions should be based on specific drafts of 802.1Qcr, complemented by future presentations for specific topics

Model for 802.1Qcr

- 1. Basic model as described in May 2016, Budapest: <u>http://www.ieee802.org/1/files/public/docs2016/Qcr-specht-specification-mapping-proposal-0516-v01.pdf</u>
- 2. Additions based on feedback on this model from TSN members, which the author believes can already be incorporated
- 3. Additions in order to be in line with the PAR

Additions (Feedback and PAR)

1. Shaper Algorithm Bug

There was an arithmetic bug in the pseudo code of the shaper. Thanks for pointing it out and fixing it!

2. Priority Mapping and Re-Mapping

ATS streams can vary their priority at different ports along their paths. The model show in Budapest introduced a new mapping mechanism. However, it seems IPV (cmp. 802.1Qci and 802.1Qch) provides a majority of what is needed, as opposed contrast to PCP/DEI in 802.1Q tags.

3. Delay Calculation (Informative Annex)

"The project provides an informative framework for worst case delay analysis in static networks/configurations."

(cmp. <u>https://development.standards.ieee.org/P946200033/par</u>, sec. 5.2.b.)

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4. Model vs. Implementation (Informative Annex)

The presented model has the intention to re-use as much as possible from what is already 802.1Q, including contents from 802.1Qci. As a consequence, the essential shaper arithmetic is at ingress near Qci meters, the queueing is at egress. However, Implementers are free to implement this model:

- Directly in this distributed manner,
- entirely on egress (cmp. <u>http://www.ieee802.org/1/files/public/docs2015/new-tsn-specht-ubs-queues-0521-v0.pdf</u>),
- etc.

We can have an informative annex to describe potential differences, while the normative parts use the proposed model as long as interoperability is ensured.



Thank you for your Attention! **Questions, Opinions, Ideas?**

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Updated Shaper FSM Algorithm

Shaper FSM: Per Frame Processing



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Parameters

- Committed Information Rate (CIR) [bit/s] The (constant) data rate of the token bucket
- Committed Burst Size (CBS) [bit] The capacity of the token bucket

State

- Bucket Empty Time [time] The time at which the token bucket was empty, initialized to "-inf"
- Bucket level storage <u>not</u> needed

Error Handling

- On exceeded Maximum Residence Time
- On exceeded Frame Length ... Qci does already provide this on per stream level¹ → can be skipped here if applicable

<pre>void processFrame(Frame frame, RxPriority rxPriority, Shaper shaper) {</pre>
<pre>time dLengthRecover = frame.length /</pre>
<pre>shaper.param.committedInformationRate;</pre>
<pre>time dEmptyToFull = shaper.param.committedBurstSize /</pre>
<pre>shaper.param.committedInformationRate;</pre>
<pre>time tShaperEligible = shaper.state.tBucketEmpty + dLengthRecover;</pre>
<pre>time tBucketFull = shaper.state.tBucketEmpty + dEmptyToFull;</pre>
<pre>boolean frameValid = true;</pre>
<pre>frame.tEligible = max(frame.tArrival,</pre>
tShaperEligible);
<pre>frameValid &= frame.tEligible <= frame.tArrival +</pre>
<pre>frameValid &= frame.length <= shaper.param.lengthLimit;</pre>
<pre>if (frameValid){</pre>
// Normal: Frame pagges and state is undated
ryDriority state tEligible - frame tEligible:
shaper state tBucketEmpty = (frame tEligible < tBucketEull) 2
dLengthRecover + shaper state tBucketEmpty :
dlengthRecover + frame tEligible - dEmptyToFull:
} else {
// Error: Drop frame and trigger further reaction (blocking etc.)
}
, }
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1: 802.1Qci, 8.6.5.1, item e)1)