

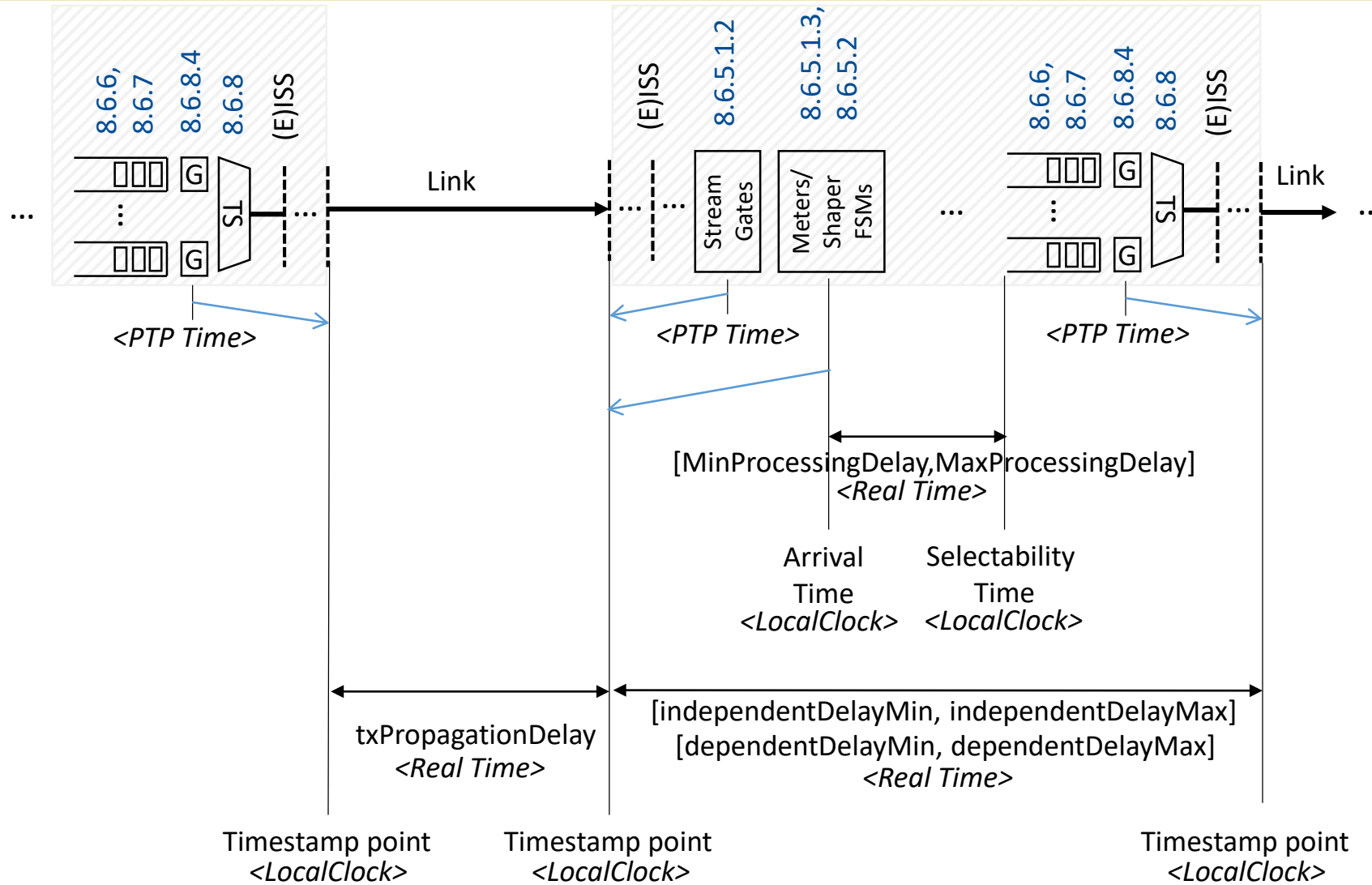
# Bridge Timing

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## Background and Motivation

- Initial bridge timing model proposals during last July Plenary Meeting:
  - Norm Finn: <http://www.ieee802.org/1/files/public/docs2017/cr-finn-timing-model-0617-v00.pdf>
  - Verbally during P802.1Qcr-D0.1 comment resolution
- Purpose of a bridge timing model (examples):
  - **Configuration**  
How to setup  $Q_{ci}+Q_{bv}$  time slots, a.k.a. gate events?
  - **Specification**  
How to handle bridge internal delays/delay variations by the ATS shaping algorithm?
  - **Analysis**  
What is the maximum End-to-End delay bound of stream X along path Y, for Qcr and others?

# Big Picture

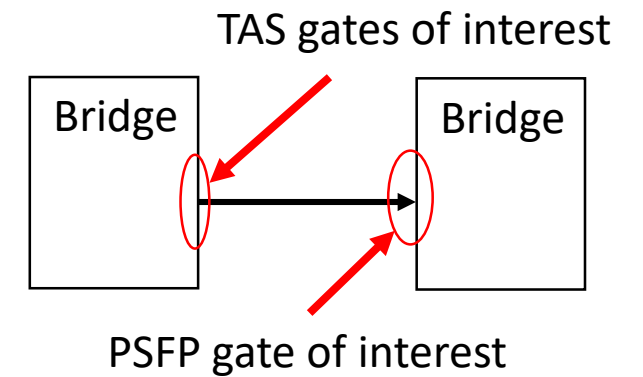
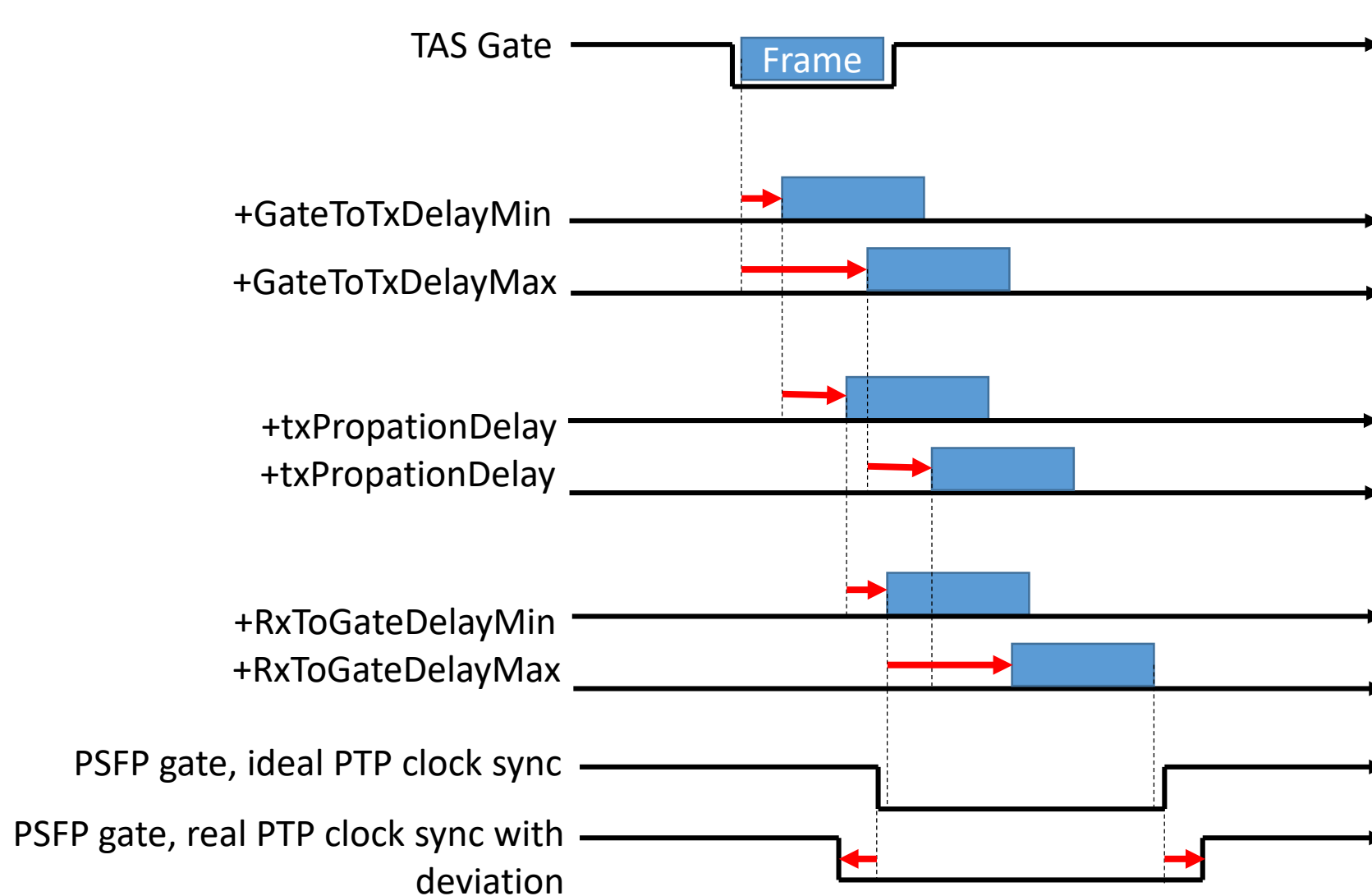


Sources: 802.1Q-Rev D1.4, 802.1AS-Rev D5.0, 802.1Qcc D1.6, 802.1Qci D2.2, and 802.1Qcr D0.1, augmented with content from comment dispositions, maintenance requests, etc.

# Issue: Delay Variations

- PFSP and TAS gate events are configured according to the reference plane time (SFD on the link).
- There can be a variation between the reference plane and the gates in bridges:  
<http://www.ieee802.org/1/files/public/docs2017/cr-finn-timing-model-0617-v00.pdf>
- **Proposal:**
  - Add [GateToTxDelayMin, GateToTxDelayMax] for TAS, and [RxToGateDelayMin, RxToGateDelayMax] for PSFP, however ...
  - ... only for consist explanation.
  - Managed objects for the variation are sufficient:
    - GateToTxDelayVariation := GateToTxDelayMax – GateToTxDelayMin
    - RxToGateDelayVariation := RxToGateDelayMax – RxToGateDelayMin

# Single Hop Example

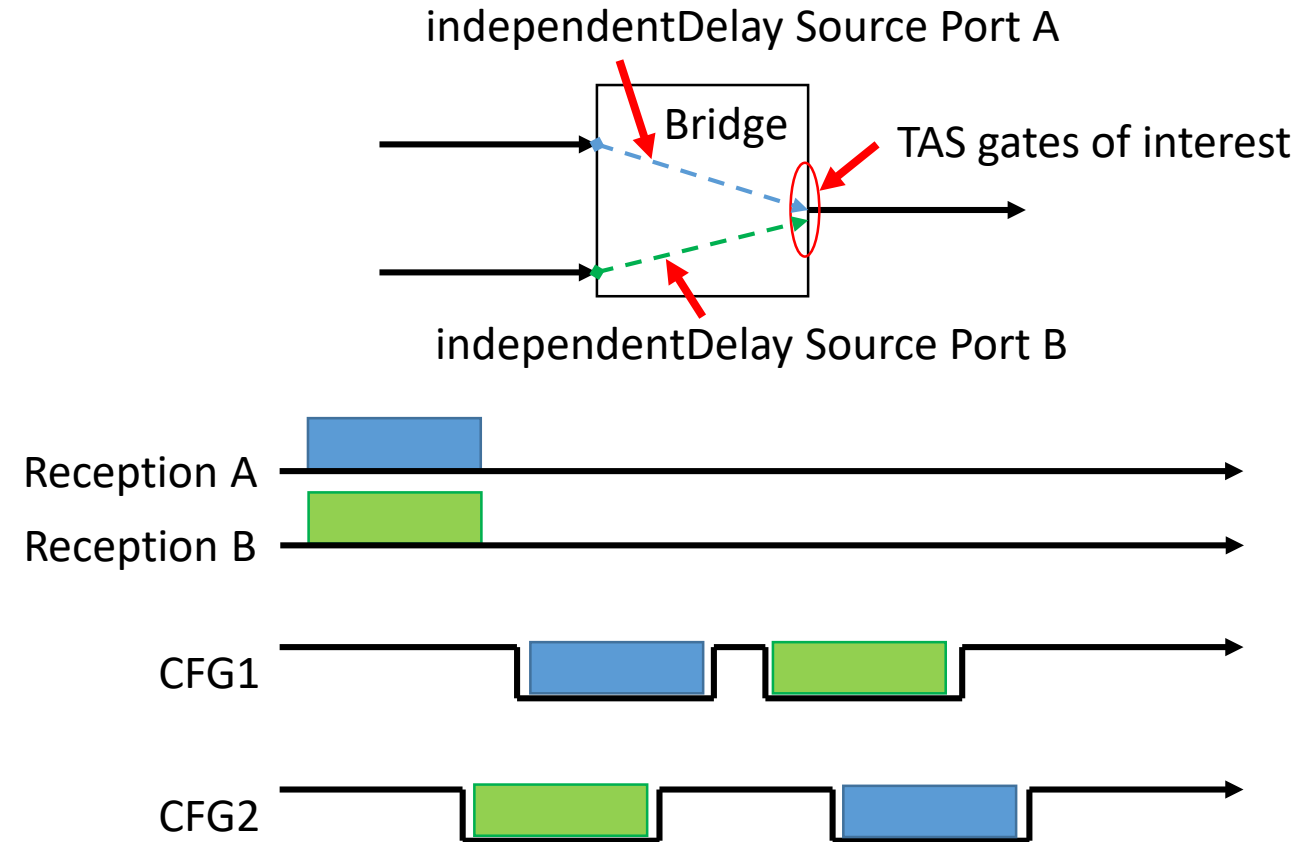


# Issue: “Oscillating” Configurations

- From 802.1Qcc/D1.6:  
*“If the Bridge design varies based on the configuration of features in the Bridge, the delays are returned according to the current configuration of the Bridge...”*
- This statement appears too general. If The Bridge delays change by, for example, changing input and output gate events, a CNC may never find a configuration.
- **Proposal:**
  - Black-list features/functions/parameters that are not allowed to affect the delay parameters.
  - Examples:
    - Input Gate Event List Entries
    - TAS Gate Event List Entries

# Simplified Example

- Assumptions:
  - Cut-Through @ 1 Gbit/s, 100 Byte frames
  - $\text{independentDelayMin} = \text{independentDelayMax}$
- Step 0: No gate events configured
  - $A = 1000$  ns,  $B = 2000$  ns reported to CNC
- while (true) {**
- Step 1: TAS Gate configuration CFG1 by CNC
  - $A = 2300$  ns,  $B = 700$  ns reported to CNC
- Step 2: TAS Gate configuration CFG2 by CNC
  - $A = 1000$  ns,  $B = 2000$  ns reported to CNC
- }**



# Thank you for your Attention!

## *Questions, Opinions, Ideas?*

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