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Implementation Architecture, Suggested Preambles and Study, VLSI Components for Standard 1 Mbit/s GFSK and for Higher Bit Rate FQPSK, Offset QPSK WLAN

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Abstract

This paper describes Implementation Architecture's, Suggested Preambles Study and VLSI Components for FQPSK, Offset QPSK for Higher Bit Rate WLAN. Various coherent demodulation schemes are discussed in different environments such as AWGN, Rician and Rayleigh fading environments and it is shown that carrier recovery for coherent demodulation is possible with reasonably short preambles. Moreover, with present LSI technology and also by assuming availability of some RF components under development, the cost or hardware penalty of coherent demodulation if there is any, will be negligible small. In overall, the fully digitalized burst modem coupled with FQPSK modulation can achieve not only better spectral efficiency but also better reliability with comparable cost to that of differential detection or discriminator modems.

The FQPSK and FQPSK-KF family of nonlinearly amplified modem/radio systems utilize the patents listed in the references. License will be provided "on a reasonable and non-discriminatory basis" and other terms stipulated by IEEE. Notice of Patent Applicability is given in Dr. K. Feher, ECE Dept. University of California, Davis, Davis, CA 95616 submission No. IEEE P802.11-93/139. Additional patents related to faster carrier synchronization belonging to NTT, Nippon Telegraph and Telephone Corporation, Japan could be offered free of charge if the Committee requests the same and these systems would become part of the standard.

1 Introduction

In Wireless Local Area Networks Communications, spectral efficiency is one of the most important parameters to specify the systems in addition to the cost of the system. Along with this purpose, a family of off-set QPSK modulation, FQPSK, FQPSK-KF have been proposed (1)-(8) and discussed assuming not expensive hardware implementation of the modem.

On the other hand, in satellite time division multiple access (TDMA) communication systems, the Offset QPSK burst modem has been in commercial use(9) and more sophisticated Offset QPSK modem has been under development(10). The former employs 17.6 Mb/s Offset QPSK modulation and this is the first employment of Offset QPSK modems in commercial systems. This modem is used and will be used in additive White Gaussian noise environments. Moreover, coherent modulation and demodulation systems have been studied in fading environments. For example, the dual carrier filter (DCF) type coherent demodulation scheme and its improved version were proposed to demodulate QPSK or OQPSK signals in Rician fading environments.(11),(12) Furthermore, in Rayleigh fading environments, there have been proposals of coherent demodulation. (13)-(16)

In addition, LSIC implementation has been going on in various institutions to realize sophisticated functions in a simple chip. Along with this target, a number

of LSICs for forward error correction (FEC), TDMA synchronization unit and modems have been developed. (17)-(21) These include a full digital 60 Mb/s modulator LSIC and also a full digital 60 Mb/s coherent demodulator for QPSK and OQPSK signals. (22)

Based on these advanced technologies, this paper presents implementation architecture, preamble study and VLSI components for the spectrally efficient modulation scheme, FQPSK and its families.

2 Coherent vs non-coherent modem

The points of this paper, coherent vs. non-coherent dmodulation are summarized in Table 1. Although the FQPSK-KF modulation scheme achieves better spectral efficiency and better bit error rate performance, the cost or hardware size penalty if there is any, will be a code word for carrier recovery, hardware size and power consumption.

3 Preambles for carrier and clock recovery

(1) Approach 1 : based on High Speed Demodulator LSIC

The estimated carrier recovery (CR) and BTR length are listedin Table 2. The full digital 60 Mb/s LSIC employs 40 symbols for both CR and BTR since this LSIC must operate in low C/N environments (less than 8 dB). On the other hand, the burst demodulator for wireless LAN has about 10 dB (or more) better C/N environments than this and this leads significant CR and BTR length reduction. The carrier recovery scheme is a reverse-modulation type and the carrier will be recovered first followed by bit timing.

(1) Approach 2 : based on Burst DEM for PHP system

Another burst demodulator LSIC which is under develpment is for the personal handy phone (PHP) system which will be a Japanese personal communication standard near future. This will operate at a bit rate of 384 kb/s. This carrier recovery is also based on reverse-modulation type carrier recovery, but in this case, the bit timing will be recovered first followed by carrier. This approach leads 0 symbol for carrier recovery if there is 16 symbols for bit timing recovery. The estimated and experimentally confirmed preamble length are listed in Table 3.

Preambles for Carrier and Bit Timing Recovery
: 16 Symbols in all is enough

4 Architecture

(1) Basic Modulator Configurations (Fig. 1).

(2) Alternative Configurations for FQPSK and GFSK Modulator (Fig. 2).

(3) Demodulator Configuration

Basic demodulator configurations are shown in Fig. 3 for both coherent and differential detection. The essentila difference is a carrier recovery circuit which is required for coherent demodulation.

(a) Typical Carrier recovery circuits (Fig. 4).

The most suitable carrier recovery circuit to achieve short carrier recovery code word is the "reverse-modulation carrier recovery circuit".

(b) Typical Clock Recovery Circuit (Fig. 5)

The phase estimation method with DFT requires short code word for clock recovery.

5 LSIC Implementation

(1) Approach 1 : based on 60 Mb/s burst modem

Table 4 and 5 summarize major parameters of the 60 Mb/s modulator and demodulator LSICs. A block diagram of the 60 Mb/s burst demodulator for FQPSK signals is shown in Fig. 6. The present high speed LSIC requires 120 k gate and consumes 0.9 W but FQPSK burst demodulator LSIC for wireless LAN will require only 30 k gate and consume less than 20 mW as shown in Table 6.

(2) Approach 2 : Customized FQPSK demodulator for WLAN

A block diagram of FQPSK demodulator which is customized for wireless LAN is shown in Fig. 7.

-Experimental Evaluation-

(i) BER/FER vs. Eb/No

BER/FER vs. EB/No in flat fading environments is shown in Fig. 8. In both cases, coherent detection achieves better performance.

(ii) BER vs. Td/Ts

BER vs. Td/Ts (Td/2: delay spread, Ts: Symbol duration) in 2 ray Rayleigh fading environments is shown in Fig.9. There is no significant difference in BER performance in both schems.

(iii) FER vs. Td/Ts

FER (Frame Error) vs. Td/Ts is shown in Fig.10. The coherent demodulation scheme achieves clearly better performance than differential one.

-Burst Demodulator LSIC for Wireless LAN-

The present burst demodulator LSIC under development which operates at 384 kb/s requires 10 k gate and consumes 5 mw. The estimated power consumption of the demodulator LSIC for wireless LAN is less than 10mW as shown in Table 6.

6 Conclusion

This paper has described Implementation Architecture, Suggested Preambles Study and VLSI Components for FQPSK, Offset QPSK for Standard and for Higher Bit Rate WLAN. It is shown that carrier recovery for coherent demodulation is possible with a reasonably short preambles. Moreover, various modem configuration have been discussed to compare hardware sizes of coherent and non-coherent modems. Furthermore, with present LSI technology and also by assuming availability of a couple of RF components under development, the size, power or cost penalty of coherent demodulation if there is any, will be negligible small. In overall, the fully digitalized burst modem coupled with FQPSK modulation can achieve not only better spectral efficiency and much higher bit rate (e.g. 1.5 Mb/s instead of 1 Mb/s) but also more robust C/I performance with comparable cost to that of differential detection or discriminator modems.

Necessity of adaptive equalizers, frequency stability and AGC/Limitershall be left for further study.

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Table 1 Summary of GFSK (non-coherent) and FQPSK-KF(coherent)

	GFSK non-coherent detection	FQPSK-KF coherent detection
Electrical Performance		
Spectral efficiency	1Mb/s/MHz	1.5Mb/s/MHz
Bit error rate performance in AWGN(10^{-5})	19.3dB	16dB
Clock recovery	Required	Required
Carrier recovery	Nil	Required/Nil
Hardware		
Volume	○	△→○ (LSIC Implementation)
Power Consumption	○	△→○ (LSIC Implementation)

Table 2 Preambles for carrier and clock recovery (Approach 1 : based on high speed demodulator LSIC)

High Speed Burst DEM	
Modulation	OQPSK
CR length	40symbol
BTR length	40symbol

Burst DEM for Wireless LAN	
Modulation	FQPSK
CR length	8symbol
BTR length	8symbol

Table 3 Preambles for carrier and clock recovery (Approach 2 : based on Burst DEM for PHP system)

Burst DEM for PHP system	
Modulation	π/4 shift DQPSK
CR length	0symbol
BTR length	16symbol

Burst DEM for Wireless LAN	
Modulation	FQPSK
CR length	0symbol
BTR length	16symbol

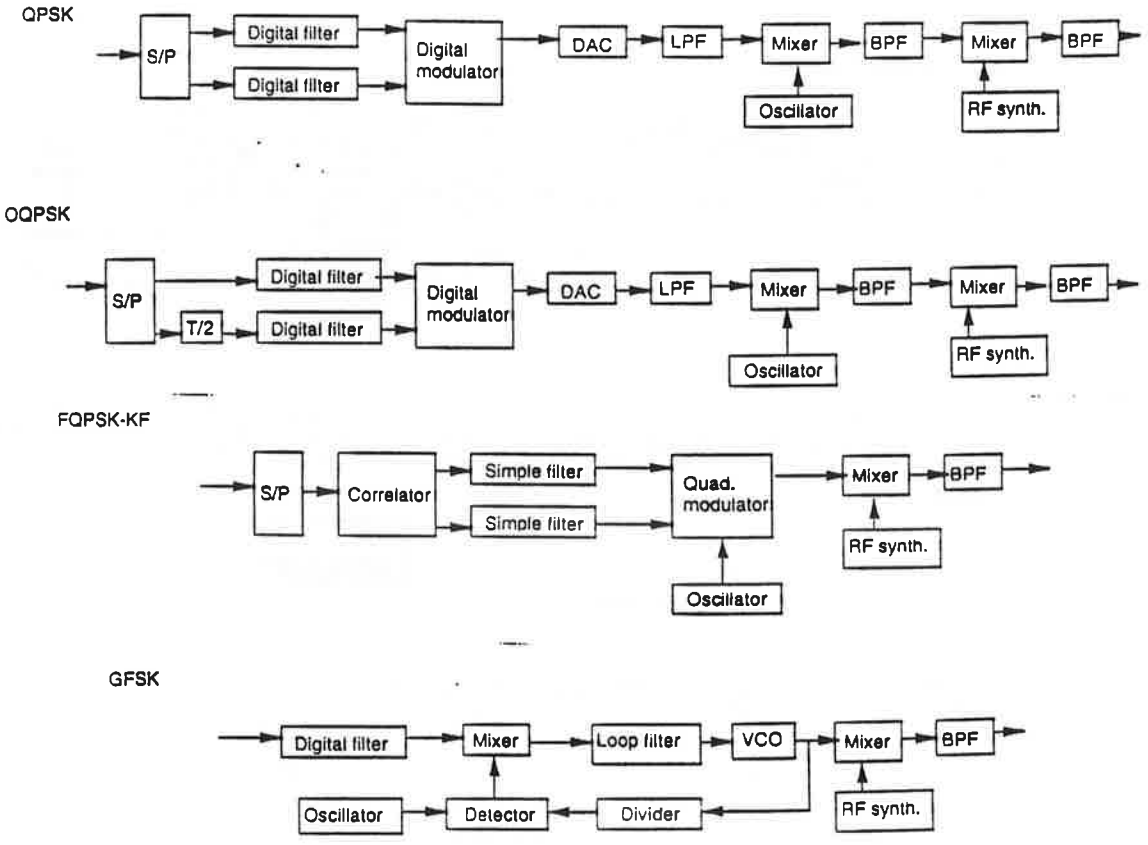
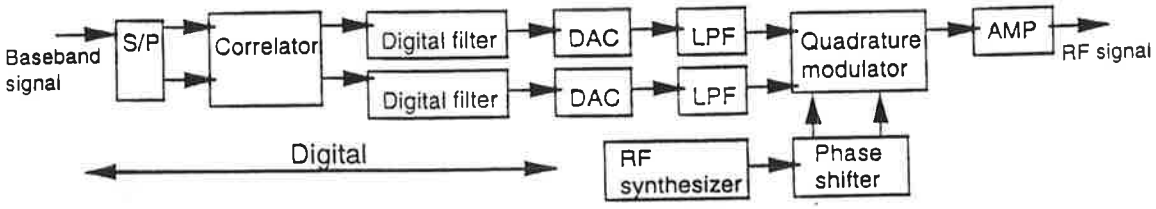


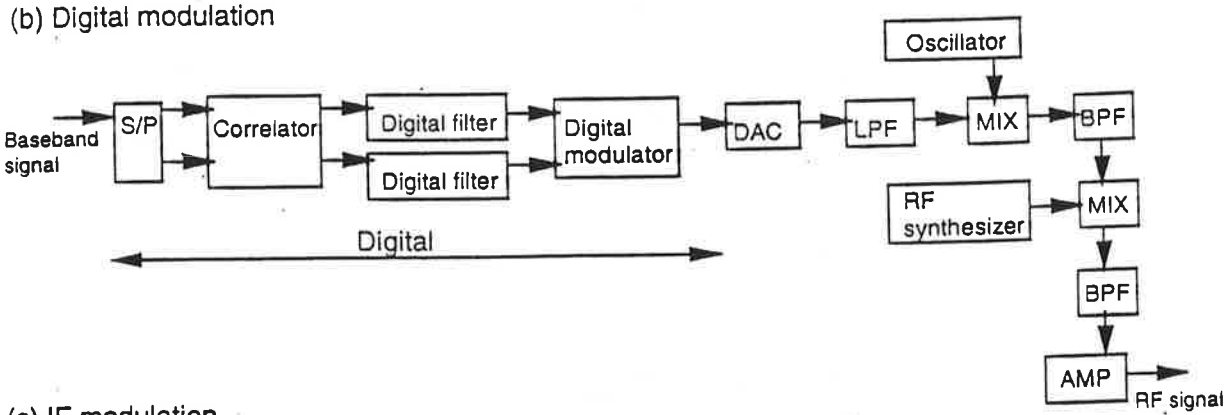
Fig. 1 Basic modulator configuration

(1)FQPSK

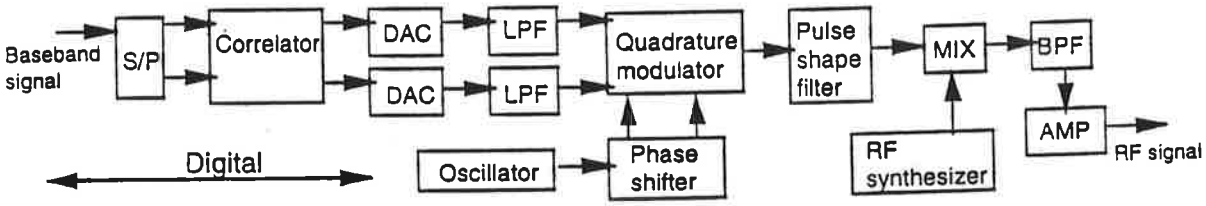
(a) Direct modulation



(b) Digital modulation

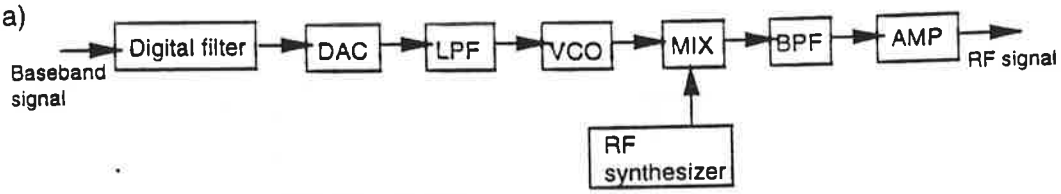


(c) IF modulation



(2) GFSK

(a)



VCO Stability OK?

(b)

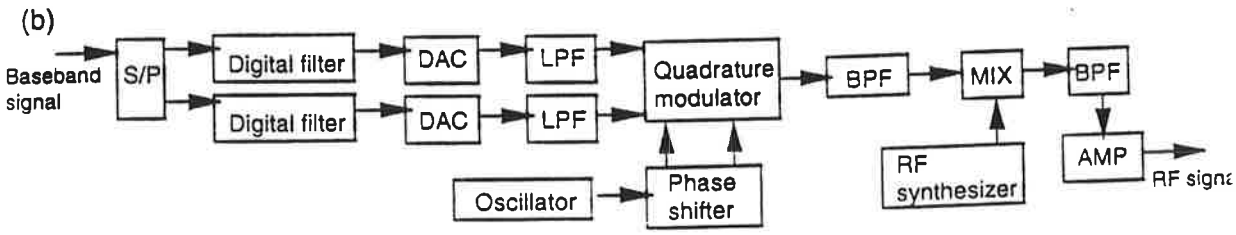
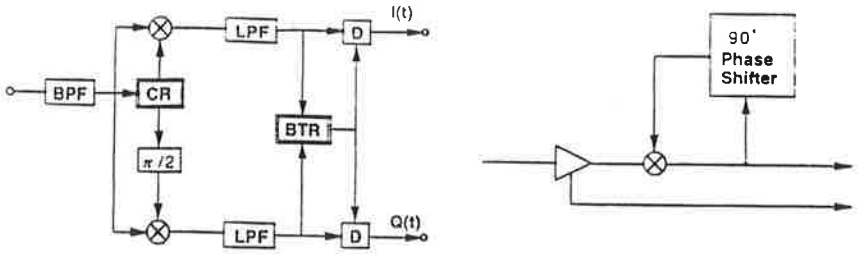


Fig. 2 Alternative configurations for FQPSK and GFSK Modulator



Coherent Detection **Differential Detection**

Fig. 3 Basic demodulator configurations

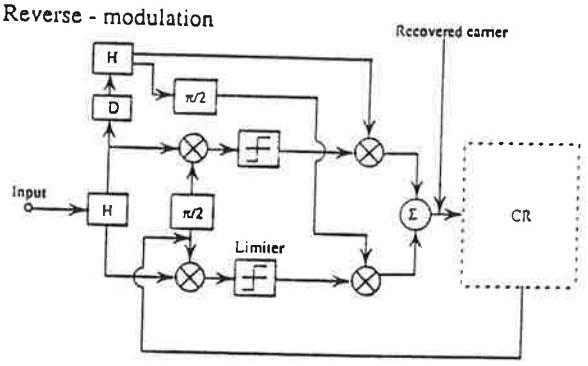
Table 4 Major parameters of the modulator VLSIC (NUMODE-M)

Process	CMOS 0.8 μm master slice
Number of gate	10,000 + ROM, RAM (total 110kgate)
Maximum clock rate	30 MHz (60 Mbit/s)
Supply voltage	+5 V
Package	160 pin QFP (0.65 mmm pitch)
Modulation	QPSK, OQPSK burst/continuoud mode
Band limitation	Raised cosine roll-off (α=0.4 implemented) , etc.

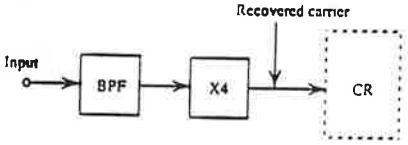
Table 5 Major parameters of the demodulator VLSIC (NUMODE-D)

Process	CMOS 0.5 μm master slice
Number of gate	120,000 + ROM, RAM
Maximum clock rate	30 MHz (60 Mbit/s)
Supply voltage	+3.3 V
Package	208 pin plastic QFP (0.5 mm pitch)
Modulation	QPSK, OQPSK burst mode
Band limitation	Raised cosine roll-off , etc.
Preamble length without unique word	Less than 80 symbols
Inter burst level difference	20 dBp-p

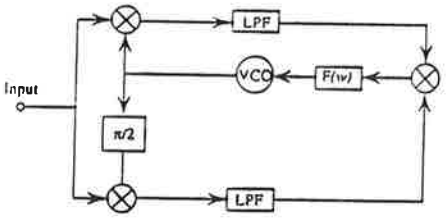
(1) Reverse - modulation



(2) X4



(3) Costas



■ Preamble length
small (1) < (2), (3) large

Fig. 4 Typical carrier recovery circuit

(1) Phase estimation
Phase estimation with DFT

(2) Maximum Amplitude Method
average position of max. amp.

(3) Wave Difference Method
average Zero-slope position

(4) Zero-crossing Method

■ Required sample rate (fs: Symbol rate)
(1), (4) : 2xfs
(2), (3) : >16xfs

■ Preamble length
small (1), (2) < (3) < (4) large

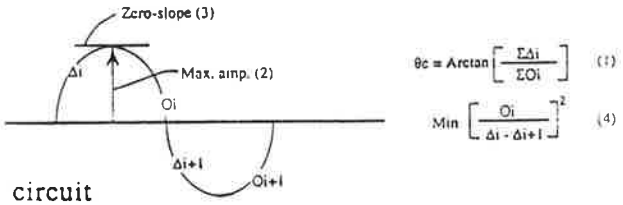


Fig. 5 Typical clock recovery circuit

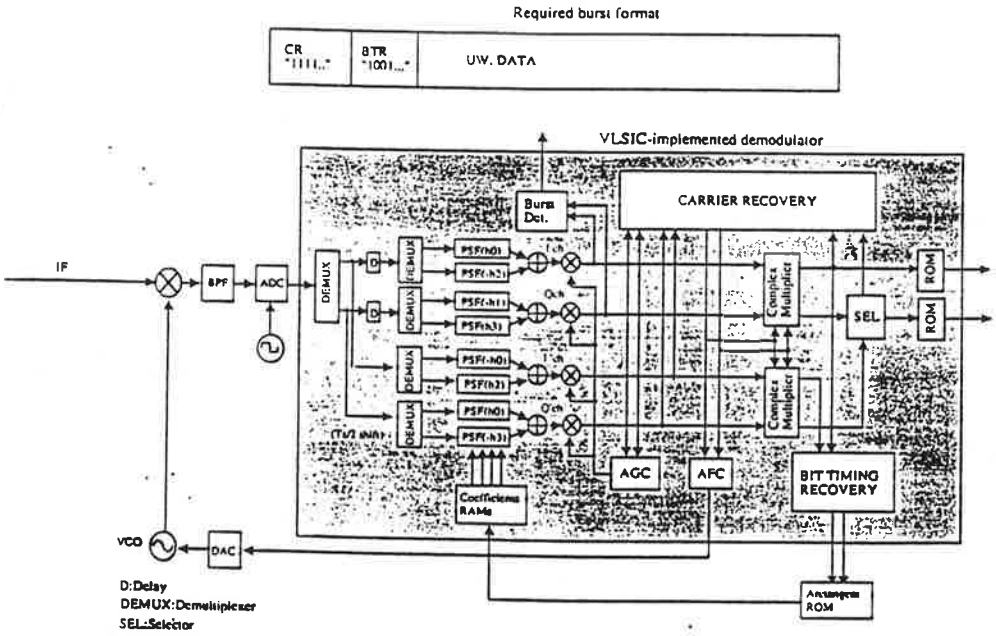


Fig. 6 Block diagram of FQPSK demodulator
(High speedburst dem. NUMODE-D)

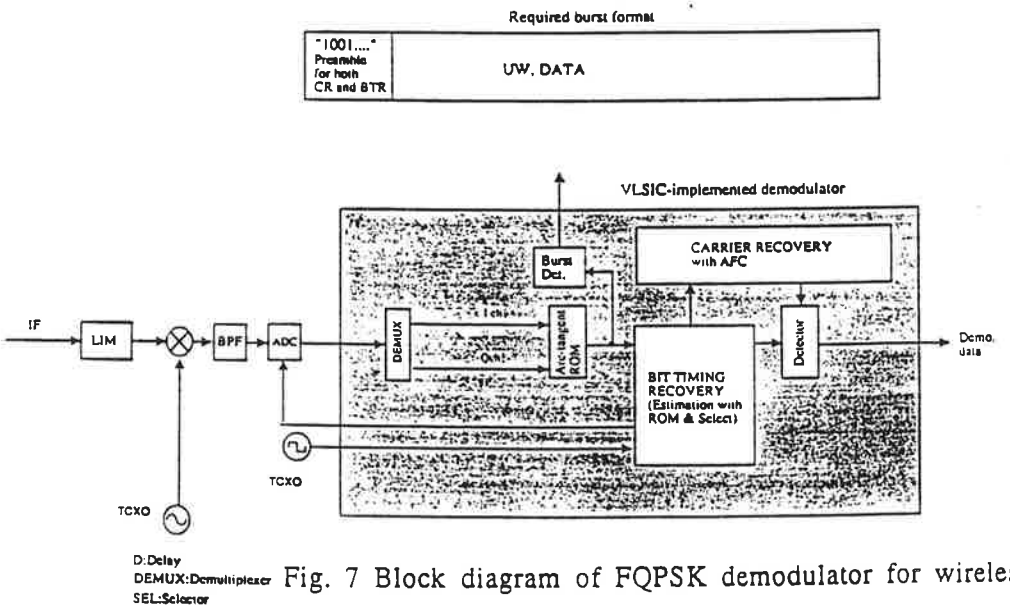


Fig. 7 Block diagram of FQPSK demodulator for wireless LAN

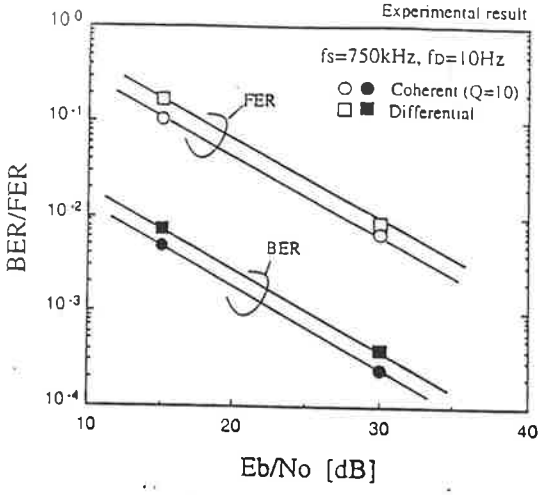


Fig. 8 BER/FER v.s. Eb/No
(Flat fading)

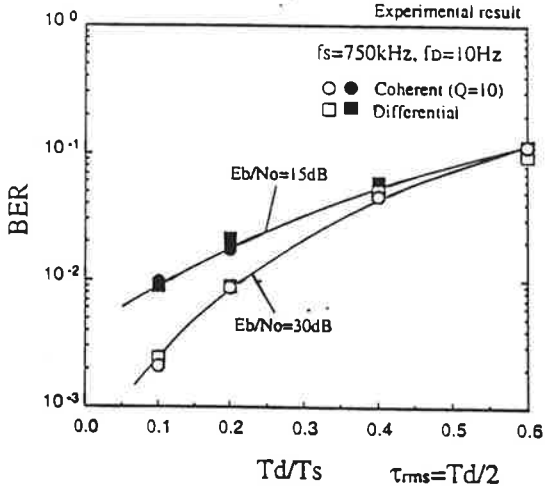


Fig.9 BER v.s. Td/Ts
(2 ray Rayleigh fading)

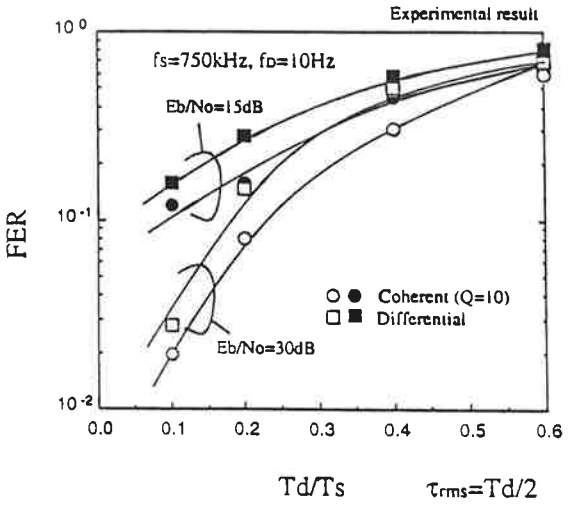


Fig.10 FER v.s. Td/Ts
(2 ray Rayleigh fading)

Table 6 Burst demodulator LSIC for Wieless LAN

High Speed Burst DEM LSIC (already realized)	
No. of gates	120Kgate
Power consumption	0.9W(60Mbit/s)

↓

Burst DEM LSIC for Wireless LAN	
No. of gates	**30Kgate**
Power consumption	**<20mW(1.5Mbit/s)**

Table 7 Demodulator LSIC for wireless LAN

Burst DEM for PHP system (LSIC under development)	
No. of gates	10Kgate
Power consumption	<5mW(384kbit/s)

↓

Burst DEM LSIC for Wireless LAN	
No. of gates	**10Kgate**
Power consumption	**<10mW(1.5Mbit/s)**