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DS-SS and Higher-Speed FH-SS Modem VLSI Implementations

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Abstract

A VLSI implementation is presented for a baseband modem processor applicable to the approved DS-SS 2 Mb/s DQPSK and OQPSK standard, the higher-bit-rate frequency hopping standard, as well as the compatible NLA (Non-Linear Amplifier) FQPSK systems. The design features low gate count, low power consumption, and low chip area resulting in a high-yield low-cost chip. The VLSI design, layout, simulation and fabrication was carried out with standard software and MOSIS 0.8 micron process to yield a complete OQPSK, DQPSK, and FQPSK baseband modulator including cross-correlator and all filters in a chip area of 2.1mm × 3.5mm. The same basic VLSI chip with slight modification can be used for either the 1 MHz or 2 MHz DS-SS or the higher-bit-rate frequency hopping (1.4 Mb/s - 2 Mb/s range) baseband modem using double-jump, raised cosine, or other FIR filters. This chip performs a similar function to those proposed by Shuko Kato of NTT Japan in submission No. IEEE P802.11-93/137 and No. IEEE P802.11-93/189 thus providing another choice for VLSI components applicable to FQPSK and OQPSK for the DS-SS and HS-FH-SS standards.

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1 Introduction

The key factors in characterizing Wireless Local Area Networks Communications are cost, spectral efficiency, and bit error rate. A family of off-set QPSK modulation systems (OQPSK and FQPSK-kf) have been proposed [1]-[14] with good spectral efficiency and bit error rate. In this paper we look at a key component of the baseband processor for both the Direct Sequence (DS-SS) and the higher-speed frequency hopping (HS-FH-SS) standards to demonstrate the ease of VLSI implementation in a single chip. The baseband processor we have chosen for implementation as a VLSI chip is the FQPSK-kf baseband processor which consists of two major components. The first component is the FQPSK-kf cross-correlator described in section 5.1. This takes less than one square millimeter (1.0mm $\times$ 0.7mm) to implement in 0.8 micron CMOS technology. The second major component are the two identical baseband low-pass filters described in section 5.2. These filters can vary from less than three square millimeters (2.0mm $\times$ 1.3mm) to over sixteen square millimeters (5.1mm $\times$ 3.2mm) depending on the filter used. Commercial production of these VLSI chips would likely yield chips in the range of fifty cents to several dollars depending on the number of chips produced and the size and complexity of the chip. Each FQPSK-kf VLSI chip requires one FQPSK-kf cross-correlator and two identical low-pass filters.

2 System Overview

Figure 1 shows the block diagram for the FQPSK-kf baseband processor. The data coming into the FQPSK-kf baseband processor consists of a 2 Mb/s bit stream for the DS-SS application and a 1.5 Mb/s bit stream for the HS-FH-SS application. This bit stream is divided into two parallel bit streams (I and Q channels) each at a data rate of f_s, called the "*symbol rate*" equal to one-half of the input signal rate by the serial-to-parallel ("S/P") converter that simply steers bits alternately to the I or Q channel [2].

After the "S/P" conversion, the signals are passed on to a cross correlator [15]. In the case of the DS-SS modulator, these signals are first multiplied by the pseudo-random noise (Barker Code) while in the case of the HS-FH-SS modulator, the signals are simply passed on to the cross-correlator [2]. The block in Figure 1 labeled FQPSK-kf cross-correlator [11, 12] is a combination of the IJF encoder and cross-correlator described in the original patent application [2]. The two I and Q channel bit streams are converted to 12-bit data streams at eight times the basic I and Q channel bit frequencies by the IJF encoders [2]. This conversion consists of reading from a ROM the 12-bit representation of half cosine wave on the trailing edge of each pulse and a similar operation for the second-half of the cosine wave on the leading edge of each pulse. After passing through the IJF encoders, a cross-correlation is done between the two channels. Further details on both the IJF encoders and the cross-correlation can be found in the original patent information [2].

We have chosen to combine the S/P converter, PN Barker code filter (if needed), and the cross correlation circuit into a single FQPSK-kf cross correlator block as shown in Figure 1. This entire function can be conveniently carried out using simple ROM table-look-up [2, 11, 12]. The I and Q channel outputs of this FQPSK-kf cross-correlator are then passed through identical low-pass digital filters. These filters are realized by standard digital filters such as raised cosine filters or double-jump filters. In order to preserve the phase information, we have used the commercial software package MATLAB® to design a linear-phase FIR digital filter approximation to the desired double-jump filter. MATLAB's FIR2 filter design program with a Kaiser window [16] was used to generate an "n"-th order linear-phase FIR filter that matches the magnitude of the desired filter at specified points. The higher n, the better the match in filters, but the at the cost of increased hardware.

3 DS-SS Application

In order to reduce the side lobes of the transmitted signal after nonlinear amplification, filtering is done in the baseband [17]. This is carried out in two stages. The first stage is the IJF encoder on the I and Q channels that was described earlier and is part of the FQPSK-kf cross-correlator [2]. The second stage is the two identical low-pass baseband filters shown in the block diagram of Figure 1. These filters are identical for the I and Q channels and must be selected in such a way as to achieve a 30db attenuation of the signal power measured after the nonlinear amplifier at the "*chipping frequency*" f_c from the carrier frequency. For our example, $f_c = 1/T_c = 11$MHz, where T_c is the "*chipping period*". We next describe two possible filters for the DS-SS application. It should be noted that these are examples filters. Many other filters will also work.

3.1 Double-Jump Filter

Figure 2 shows a plot of a typical baseband low-pass filter for the DS-SS application. The vertical axis is the gain of the filter relative to the DC gain. The horizontal axis is the frequency normalized to the chipping frequency f_c. This particular filter is a simple 7-th order, linear-phase approximation to a double-jump filter with $\alpha = 0.62$. The coefficients of this linear-phase FIR filter are given by:

30db double-jump 7-th order FIR			
Coeff.	Value	Coeff.	Value
1	1.0000000e+00	8	1.0000000e+00
2	-4.1113395e+00	7	4.1113395e+00
3	-1.1497902e+01	6	-1.1497902e+01
4	-1.7770778e+01	5	-1.7770778e+01

These coefficients were obtained by matching 256 points of an ideal double-jump filter with $\alpha = 0.62$ to a linear-phase FIR filter using MATLAB's FIR2 design program with Kaiser windowing ($\beta = 0$) [16].

3.2 Raised-Cosine Filter

Figure 3 shows a plot of a baseband low-pass filter for the DS-SS application based on a raised-cosine filter. The vertical axis is the gain of the filter relative to the DC gain. The horizontal axis is the frequency normalized to the chipping frequency f_c. This particular filter is a simple 7-th order, linear-phase raised-cosine filter with $\alpha = 1.00$. The coefficients of this linear-phase FIR filter are given by:

7-th Order Raised Cosine			
Coeff.	Value	Coeff.	Value
1	1.0000000e+00	8	1.0000000e+00
2	-2.1917390e+00	7	-2.1917390e+00
3	-9.0515679e+00	6	-9.0515679e+00
4	-1.5092738e+01	5	-1.5092738e+01

4 HS-FH-SS Application

As in the DS-SS case, the side lobes of the transmitted HS-FH-SS signal must be reduced after nonlinear amplification by filtering done in the baseband [18]. As with the DS-SS modulator, the first stage of filtering is the IJF encoder on the I and Q channels that was described earlier and is part of the FQPSK-kf cross-correlator [2]. The second stage is the two baseband low-pass filters shown in the block diagram of Figure 1. These filters are identical for the I and Q channels and must be selected to achieve a 20db attenuation of the signal power measured after the nonlinear amplifier at the frequency $0.71 f_s$ from the carrier frequency. Here f_s is the "*symbol frequency*" which for our example was given by $f_s = 1/T_s = 750$kHz, where T_s is the "*symbol period*". As in the case of the DS-SS modem, many possible filters may be used for the baseband low-pass filter. In what follows we discuss one possibility.

Figure 4 shows a plot of a 48-th order, linear-phase approximation to a double-jump filter with $\alpha = 0.48$. The vertical axis in the graph of Figure 4 is power spectral density in relative db (dbr) and the horizontal axis is normalized frequency fT_s such that $f = 1.0$ corresponds to a frequency f_s away from the carrier frequency. This approximation was done using MATLAB's FIR2 design program [16] to match 250 points of the $\alpha = 0.48$ double-jump filter to the 48-th order linear-phase FIR filter using a Kaiser Window ($\beta = 0$). The resulting FIR filter coefficients are:

48-th Order 20db Double-Jump			
Coeff.	Value	Coeff.	Value
1	1.0000000e+00	49	1.0000000e+00
2	1.1690245e+00	48	1.1690245e+00
3	9.7284135e-01	47	9.7284135e-01
4	4.0838174e-01	46	4.0838174e-01
5	-4.2658244e-01	45	-4.2658244e-01
6	-1.3425269e+00	44	-1.3425269e+00
7	-2.0910275e+00	43	-2.0910275e+00
8	-2.4168097e+00	42	-2.4168097e+00
9	-2.1195939e+00	41	-2.1195939e+00
10	-1.1131346e+00	40	-1.1131346e+00
11	5.3188588e-01	39	5.3188588e-01
12	2.5723679e+00	38	2.5723679e+00
13	4.6113079e+00	37	4.6113079e+00
14	6.1504718e+00	36	6.1504718e+00
15	6.6704009e+00	35	6.6704009e+00
16	5.7248022e+00	34	5.7248022e+00
17	3.0324477e+00	33	3.0324477e+00
18	-1.4511107e+00	32	-1.4511107e+00
19	-7.4970672e+00	31	-7.4970672e+00
20	-1.4611459e+01	30	-1.4611459e+01
21	-2.2089333e+01	29	-2.2089333e+01
22	-2.9108017e+01	28	-2.9108017e+01
23	-3.4845046e+01	27	-3.4845046e+01
24	-3.8601284e+01	26	-3.8601284e+01
25	-4.0200772e+01	25	-4.0200772e+01

5 VLSI Design Details

The complete FQPSK-kf baseband processor (Figure 1) has been implemented on a single VLSI chip using MOSIS 0.8 micron CMOS technology. MOSIS technology was chosen because of its ready availability and reasonable cost for producing a small number (25 chips) of VLSI chips. MOSIS 0.8 micron technology is representative of industry standard CMOS technology. Our design uses an area of 2.1mm $\times$ 3.5mm, has 32,315 gates, consumes 150mW maximum power when operated at 100MHz (considerably less power at lower frequencies), and we estimate would be about fifty cents to several dollars per chip in volume production.

We employ a fairly standard VLSI design process. Schematic capture is carried out using the Workview® software package from Viewlogic [19] which we run on IBM-PC's and on various workstations. The Viewlogic software was used for schematic

capture and simulation of the circuits. The FQPSK-kf cross-correlator portion of the VLSI design was laid out using the LAGER automatic routing and layout program [20]. The spectral mask filters were laid out using the FIRGEN automatic FIR filter generation and layout program [21]. The details of VLSI layout and design of these two circuits is described in the sections 5.1 and 5.2. The complete VLSI chip is described in section 5.3.

5.1 Detailed Design of the FQPSK-kf Cross Correlator

Figure 5 shows the schematic generated in Workview® for the FQPSK-kf cross correlator portion of the baseband processor. There are three inputs to the FQPSK-kf cross correlator:

1. the data input signal (shown as "Data In" on the block diagram of Figure 1. This is the top input pad on the left side of the schematic of Figure 5.),
2. the system clock (second input pad from the top on the left side of the schematic of Figure 5), and
3. the two-bit (ie: two-line) clock select signal (bottom two input pads on the left side of the schematic of Figure 5).

There are also three outputs (one output on the left side and two 12-bit outputs appearing on the right side of the schematic of Figure 5) as follows:

1. the filter clock output used to clock the I-channel and Q-channel filters (center output pad on the left side of the schematic of Figure 5),
2. the 12-bit I-channel output (upper twelve output pads on the right side of the schematic of Figure 5), and
3. the 12-bit Q-channel outputs (lower twelve output pads on the right side of the schematic of Figure 5).

The FQPSK-kf cross correlator steers data input alternately to the I and the Q channel. In each channel, three successive inputs are collected and a three bit code indicating the sequence of these three successive inputs is issued for both the I and Q channels. This three-bit code is formed at the output of the top shift register "RS4" block for the I channel and the bottom shift register "RS4" block for the Q channel in Figure 5. In order to generate this code, the system clock rate is reduced by a factor of eight through the use of a three-bit ripple counter shown as "FD" in the center on the left side of the schematic of Figure 5. The output of this ripple

counter is used to clock the "Data In" to the I and Q channels and to clock the "FDR" flip flops in the lower left corner of the schematic. These D flip flops ("FDR" in the lower left corner) are used to generate the clock pulse for the two "RS4" blocks that generate the three-bit codes for the I and Q channels. These codes provide the inputs to "STORE1" and STORE2" which accomplish the cross-correlation function [11, 12]. The output of "STORE1" is the 12-bit I-channel output of the FQPSK-kf cross correlator and the output of "STORE2" is the 12-bit Q-channel output of the FQPSK-kf cross correlator. The details of the "STORE1" circuit are shown in Figure 6 and the details of the "STORE2" circuit are shown in Figure 7. These are a straight-forward implementation of the cross-correlation algorithm [2]. The outputs of the "STORE1" and "STORE2" blocks in the schematic of Figure 10 are buffered by output latches located between the "STORE" circuits and the output pads on the I and Q channels. These output latches are shown in detail in Figure 8.

5.2 Detailed Design of the Baseband Low-Pass Filters

The public domain software FIRGEN [21] was used to generate the FIR filters for the I and Q channels. The coefficients are input to the FIRGEN program and it automatically generates the FIR filter and the layout for the MOSIS CMOS process [21]. FIRGEN is extremely efficient in realizing FIR filters because it uses *Canonical Signed Digit* (CSD) coding to represent the filter coefficients. FIRGEN also has an option to optimize linear-phase FIR filters so that the symmetry of the filter can be utilized to reduce the number of multipliers required to implement the FIR filter [21].

Figure 9 shows the schematic diagram for a seventh-order (eight coefficient) FIR filter. This filter has been optimized for linear phase. As shown, it could implement the eight-coefficient raised cosine filter of Figure 3 or the eight-weight linear phase approximation to the double-jump filter of Figure 2. Figure 10 shows two 48-th order (49-weight) FIR filters generated by FIRGEN. These filters have also been optimized for linear phase. As shown they would implement both the I and J channel filters of Figure 4.

Each tap (eg: one multiplier, adder, and delay of Figure 9, 10 or 11) of the FIR filter is realized in CSD by an array of adders as shown in Figure 12 [21]. Each row of adders represents a digit in CSD. The number of digits required for a particular tap depends completely on the value of the CSD filter coefficient and thus the weight of the tap. These weights have not been optimized for our example, but with optimization could result in further saving in area on the VLSI chip [21].

5.3 Detailed Design of the VLSI Chip

Figure 13 shows the chip layout for the complete FQPSK-kf baseband modem processor using the 7-th order linear-phase FIR filter approximation to the double jump

filter (Figure 2). The layout for the chip is typical regardless of the order of the filter. Thus the two filters will be laid out on the top and the bottom with the FQPSK-kf correlator (labeled "IFJ & CORR." in Figure 13) sandwiched in the middle.

The sizes for the raised cosine filter (Figure 3), the double-jump filter for the DS-SS application (Figure 2), and the double-jump filter for the frequency hopping application (Figure 4) when implemented in MOSIS standard 0.8 micron technology are as follows:

Items	Width (mm)	Height (mm)	Die Area (sq. mm)
Raise Cosine 30dB Filter	1.437	2.163	3.108
Double Jump 30dB Filter	1.347	2.006	2.702
Double Jump 20dB Filter	3.166	5.069	16.048
FQPSK-kf Cross-Correlator	0.703	1.024	0.720
FQPSK-kf Cross-Correlator with Raised Cosine 30dB Filter	3.650	2.225	8.121
FQPSK-kf Cross-Correlator with Double Jump 30dB Filter	3.468	2.055	7.127
FQPSK-kf Cross-Correlator with Double Jump 20dB Filter	5.138	7.055	36.249

6 Conclusions

Figure 14 shows the final VLSI chip for the FQPSK-kf baseband modem processor using the two 7-th order filters of Figure 3. The chip's performance has been evaluated for DS-SS, HS-FH-SS, and related applications and found to perform quite will [17, 18, 22]. The chip design has not been optimized with regard to layout as can be seen by the large amount of empty space on the chip in Figure 14. Nonetheless, the chip is only 2.1mm $\times$ 3.5mm. Using a better layout and more reasonable packing densities, we estimate that a seventy percent reduction in the chip area could be achieved yielding a chip of about 2.3mm $\times$ 2.3mm. Our chip contains 32,315 gates and consumes 150mW at maximum operating frequency of 100MHz. We note that these numbers are consistent with results obtained by others using FIRGEN (eg: power dissipation of 150mw to 340mw have been reported for similar circuits operating in the range of 25MHz to 112MHz [21]). Based on the reduced area chip, the number of gates, the technology used, and comparisons with similar commercial chips, we would estimate that volume production of these chips would result in chips priced in the range of fifty cents to a couple of dollars. We also note that another VLSI chip for just the IJF portion of the baseband processor has been produced at UC Davis [23] and this has been interfaced with standard filters designed using the Analog Devices ADSP-21020 digital signal processing chip [24].

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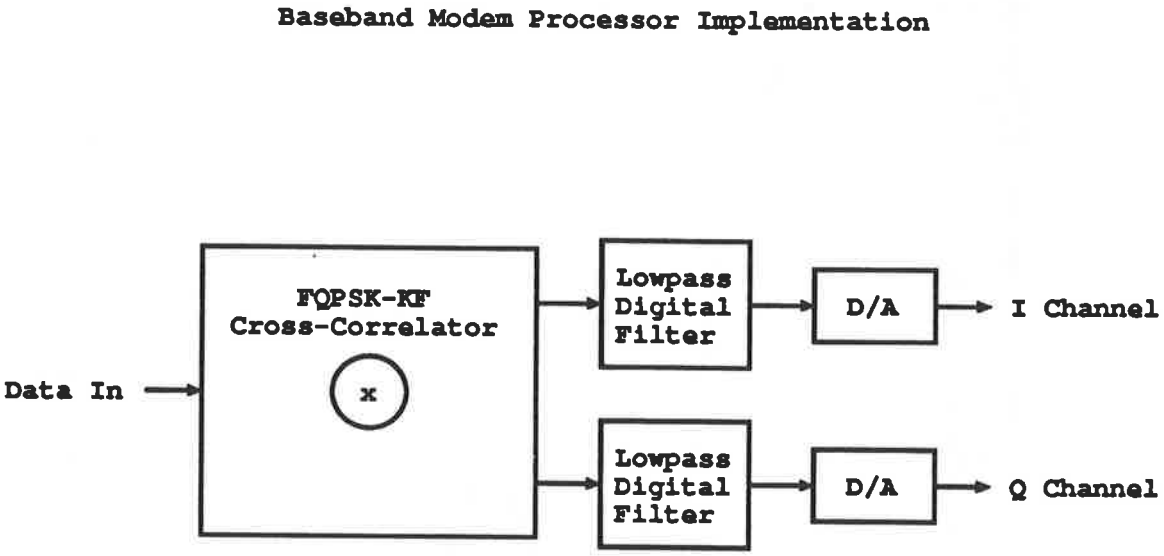

Figure 1: Block Diagram of FQPSK-kf Baseband Processor

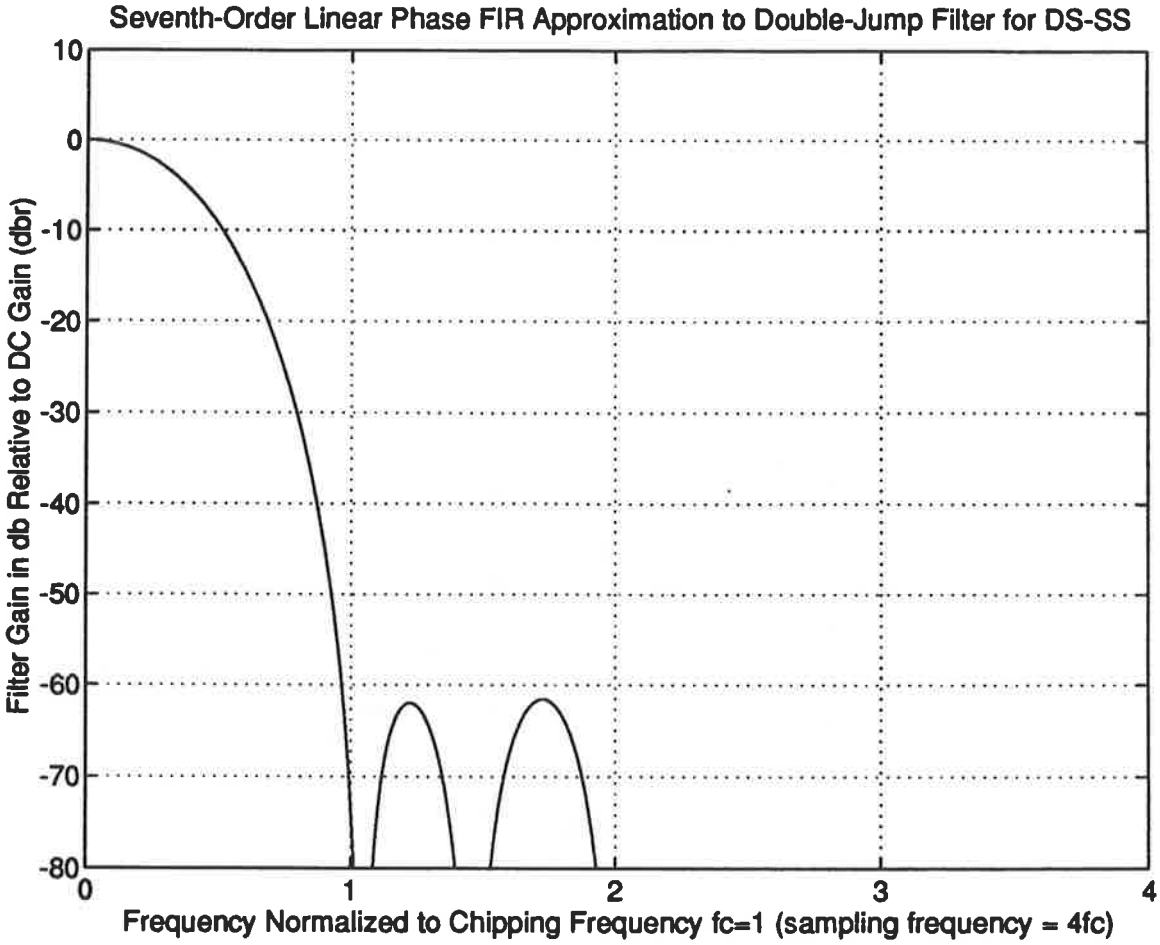

Figure 2: 7-th Order Linear Phase FIR Filter Approximation to Double-Jump Filter ($\alpha = 0.62$) for the DS-SS Application

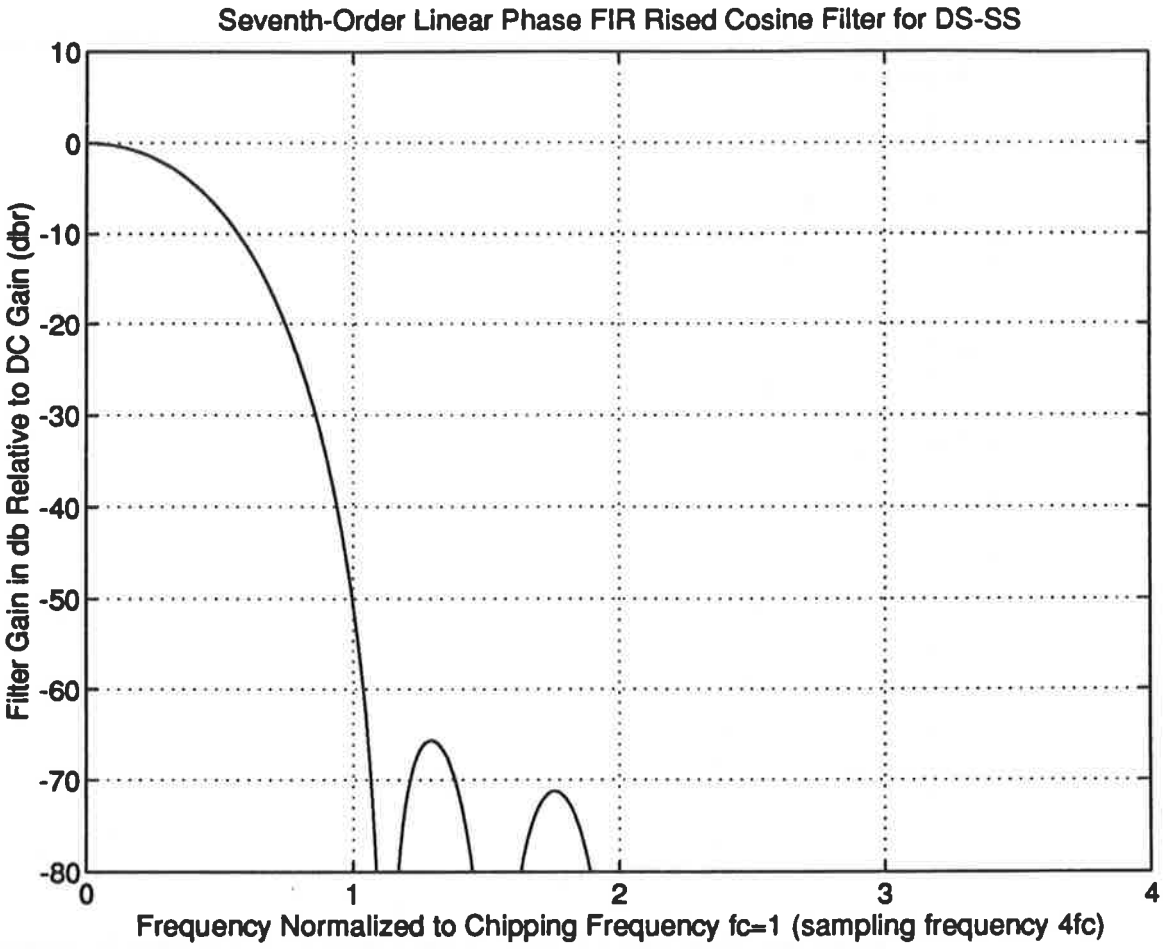

Figure 3: 7-th Order Linear Phase FIR Raised Cosine Filter ($\alpha = 1.0$) for the DS-SS Application

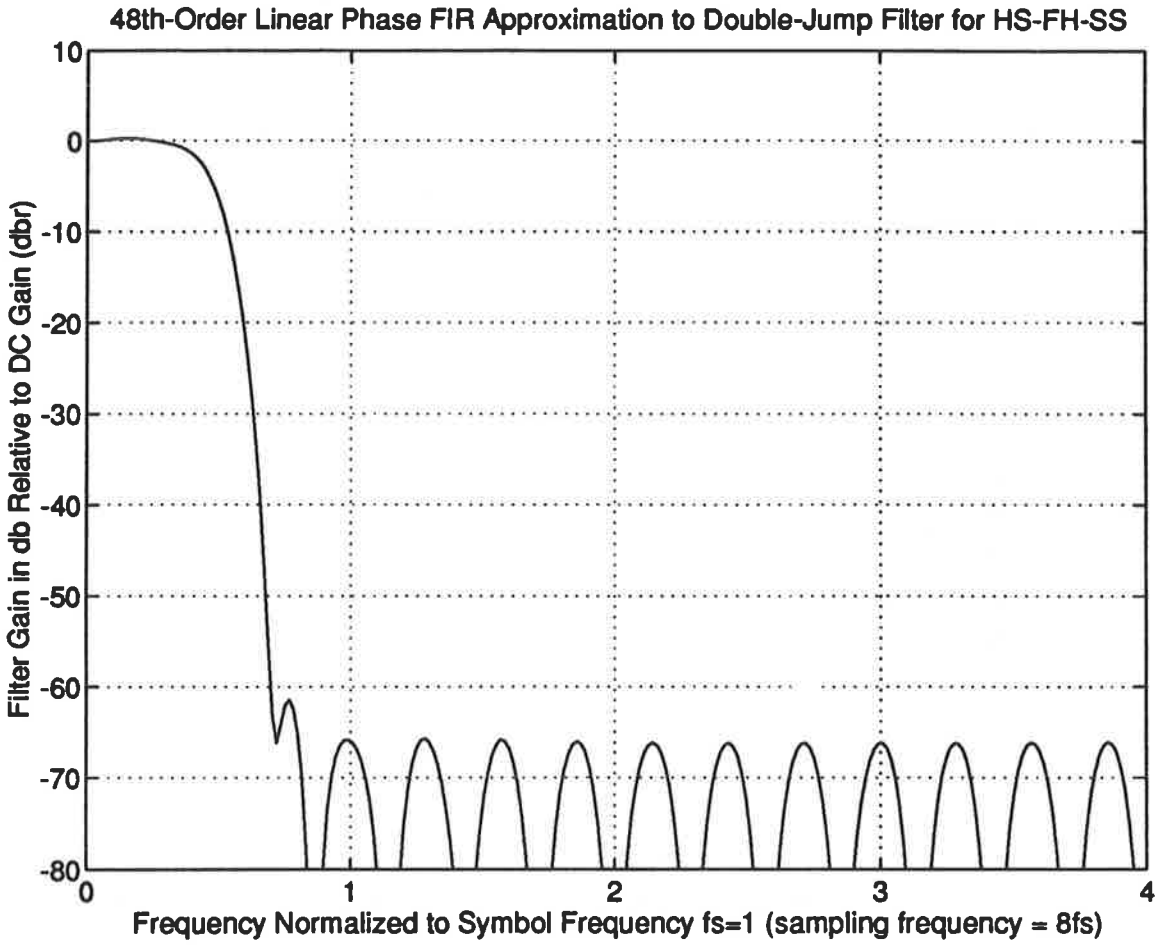

Figure 4: 48-th Order Linear Phase FIR Approximation to Double-Jump Filter ($\alpha = 0.48$) for the HS-FH-SS Application

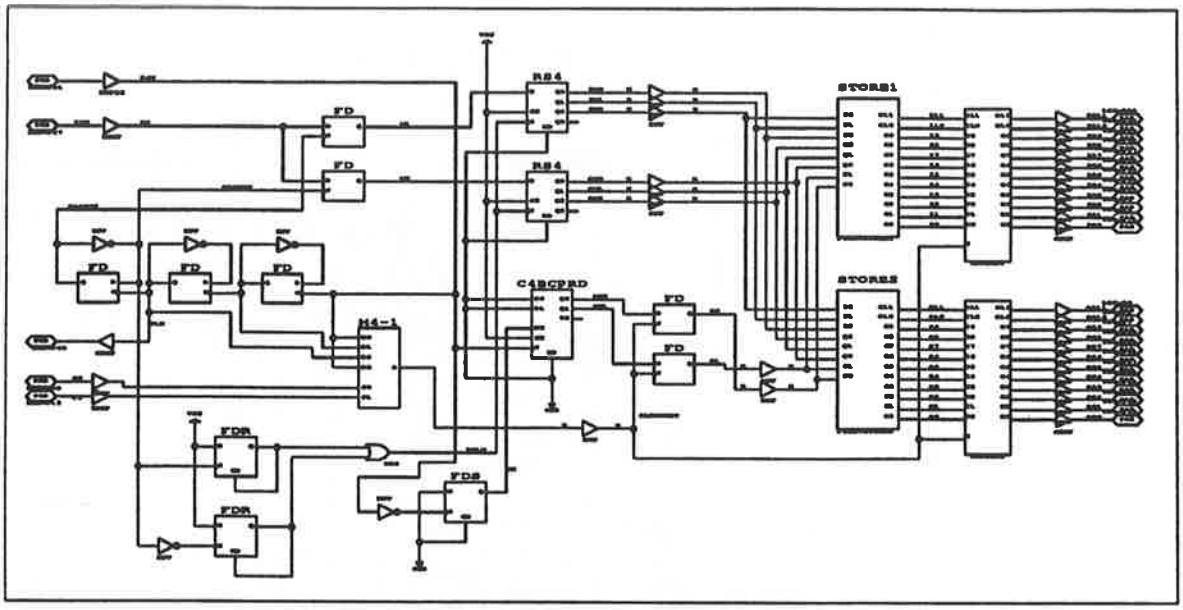

Figure 5: FQPSK-kf Cross Correlator

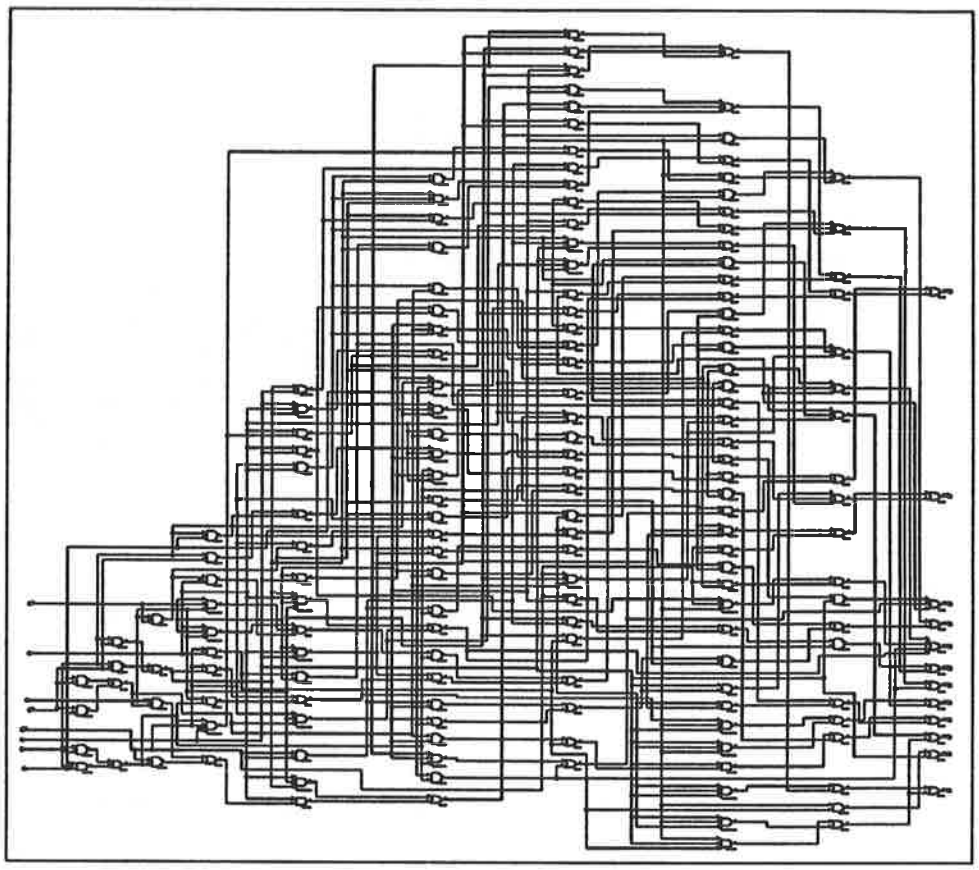

Figure 6: STORE1 Block for the FQPSK-kf Cross Correlator of Figure 5

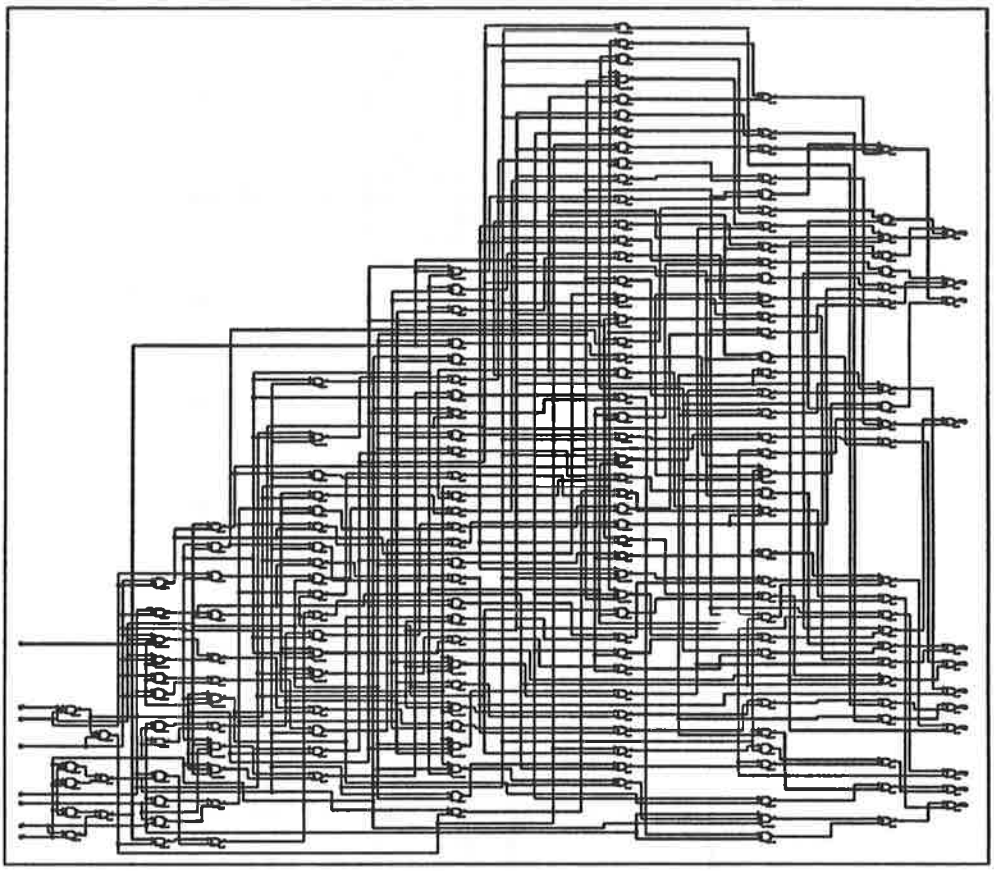

Figure 7: STORE2 for the FQPSK-kf Cross Correlator of Figure 5

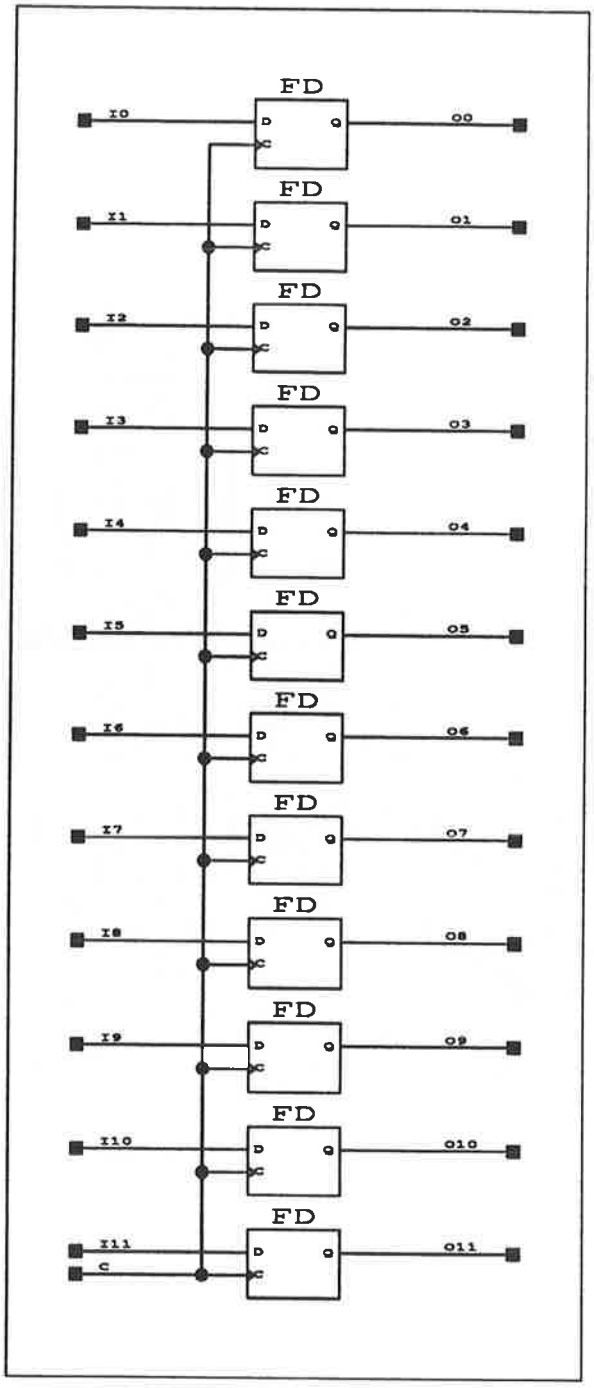

Figure 8: Output Latches for I and Q Channels of Figure 5

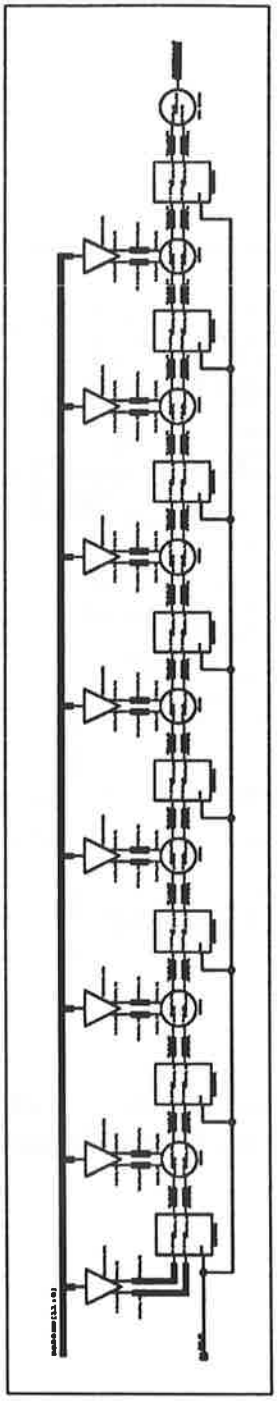

Figure 9: Eight-Weight FIR Filter Generated with FIRGEN

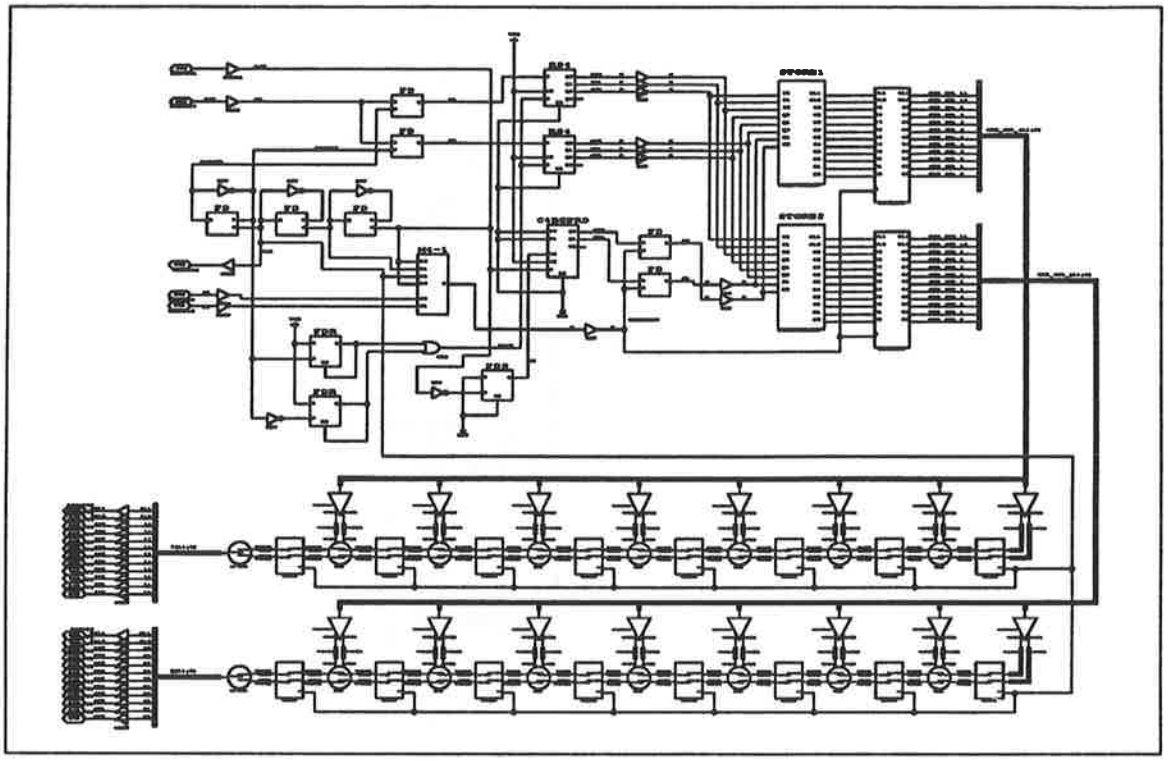

Figure 10: FQPSK-kf Cross Correlator with Two 7-th Order FIR Filters Generated by FIRGEN (Same hardware for double-jump or raised cosine filter)

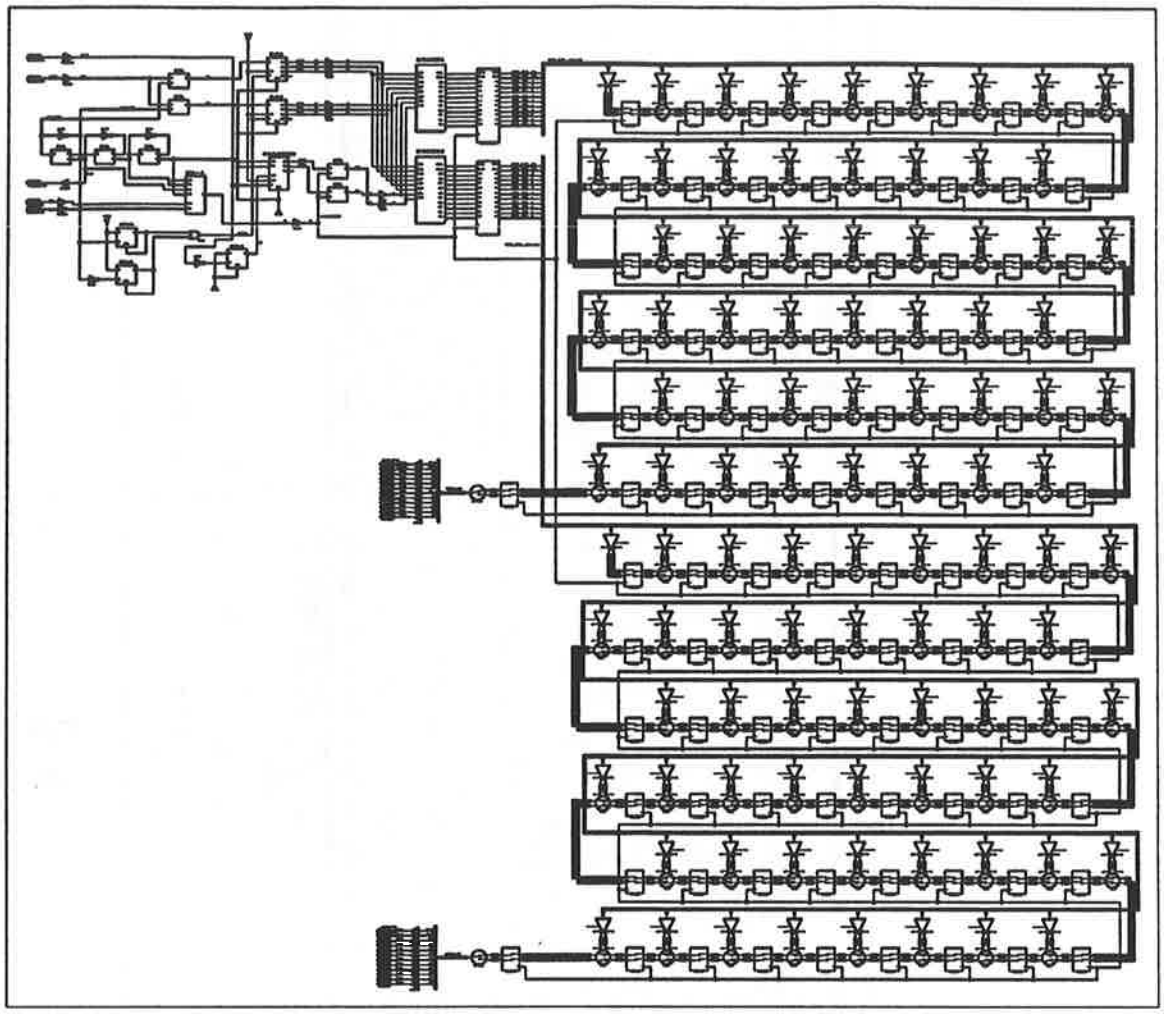

Figure 11: FQPSK-kf Cross Correlator with Two 48-th Order FIR Filters Generated by FIRGEN

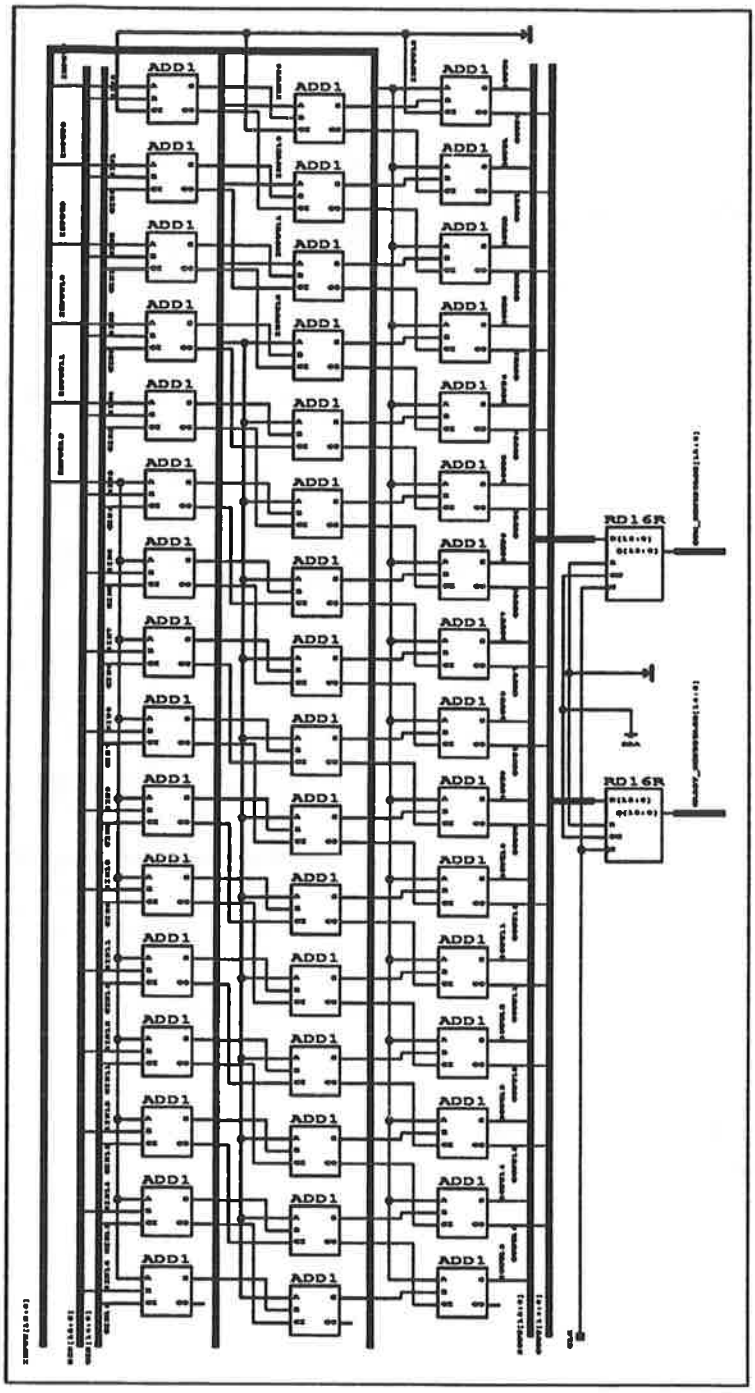

Figure 12: Example of Single Tap of FIR Filter Generated with FIRGEN

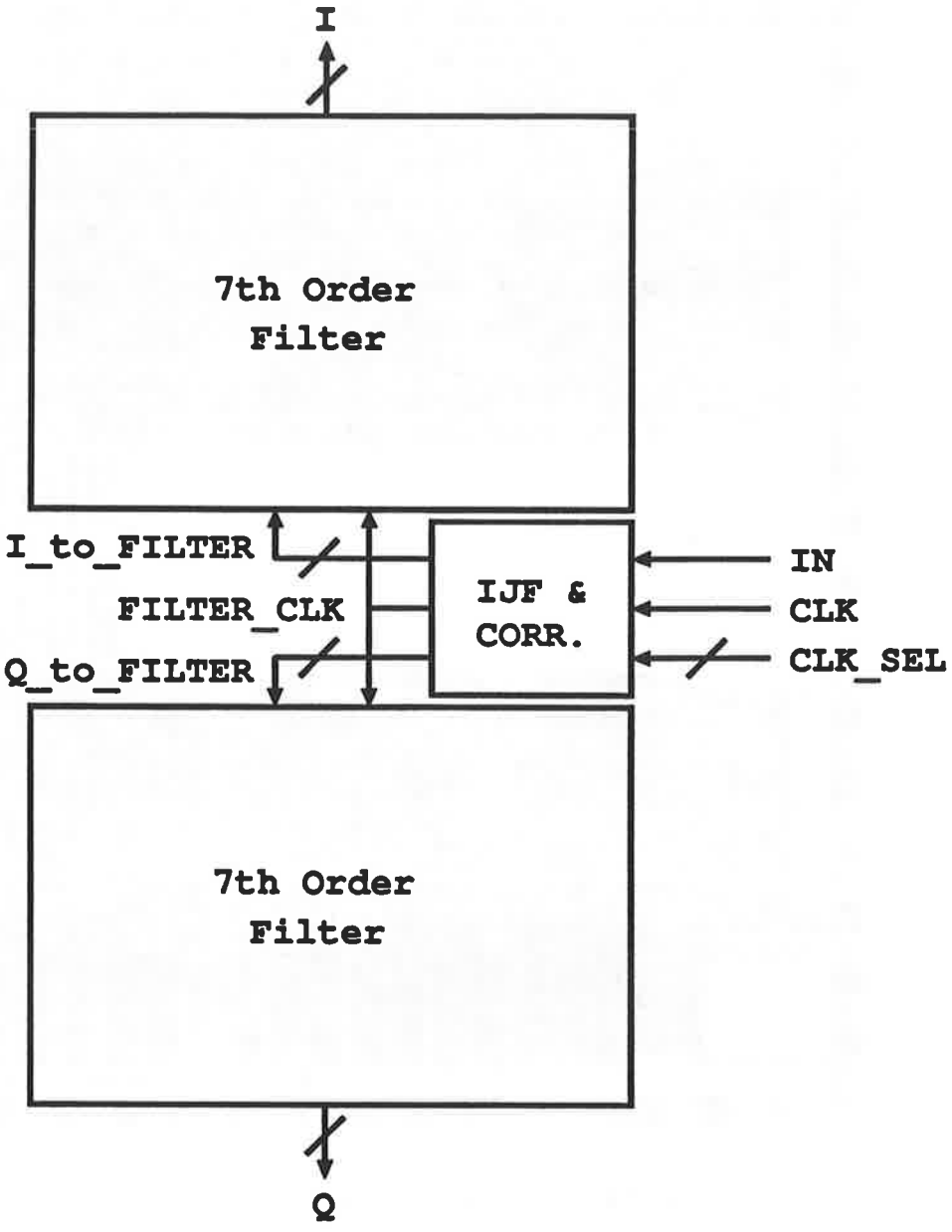

Figure 13: VLSI Chip Layout for FQPSK Baseband Modem Processor

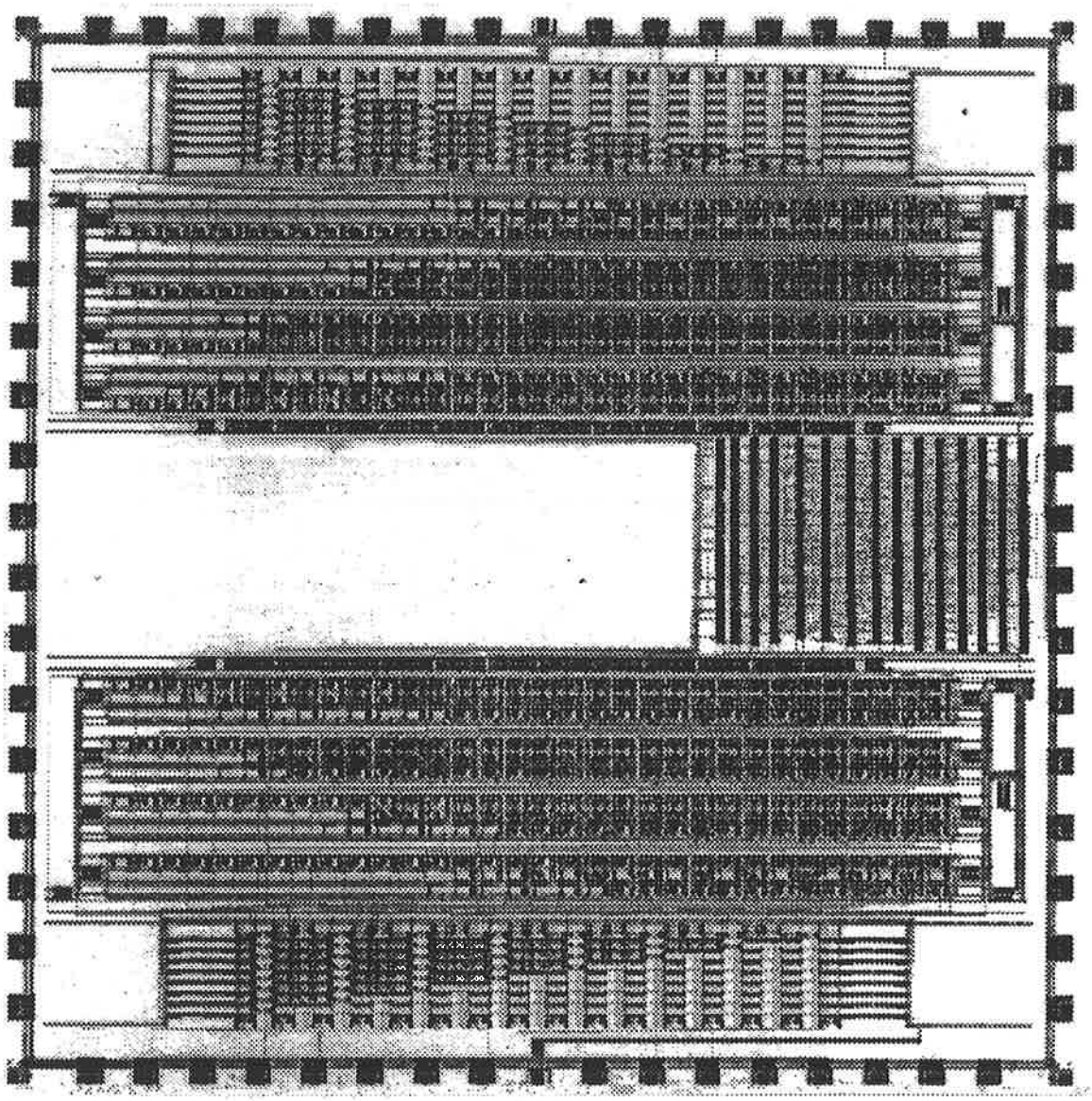

Figure 14: VLSI Chip for FQPSK Baseband Modem Processor