IEEE 802.11

WIRELESS ACCESS METHODS AND PHYSICAL LAYER SPECIFICATIONS

Title: **Clear Channel Assessment (CCA) Proposed Solution for 1 Mb/s GFSK and Higher Rate (1.4 - 2.8 Mb/s) FQPSK Systems**

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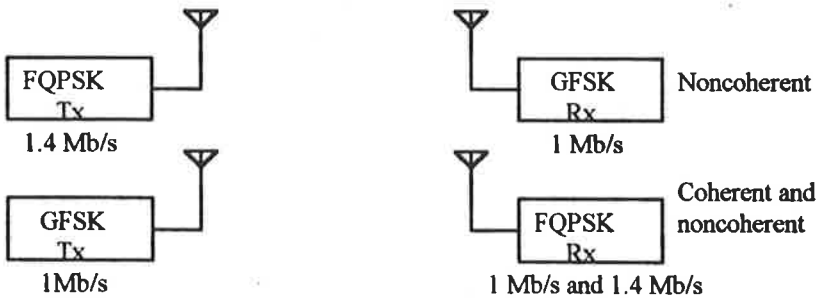
Summary

This contribution is a response to the IEEE 802.11 January 94 meeting where it was requested to submit CCA solutions. Very simple illustration solutions and concepts are described. Data clock is recovered in order for Clear Channel Assessment (CCA) decision to be made for FQPSK 1.4 Mb/s (1.5 Mb/s 2.8 Mb/s and 4.2 Mb/s) transmitted signals when operating with 1 Mb/s GFSK system. Based on the proposed methods and concepts, there is no need to change the hardware of GFSK FM discriminator. the proposed method is an illustration that CCA can be easily solved between FQPSK (at any bit rate) and GFSK . Evidently, there are many other possible solutions to CCA including pseudo error monitor method.[32]



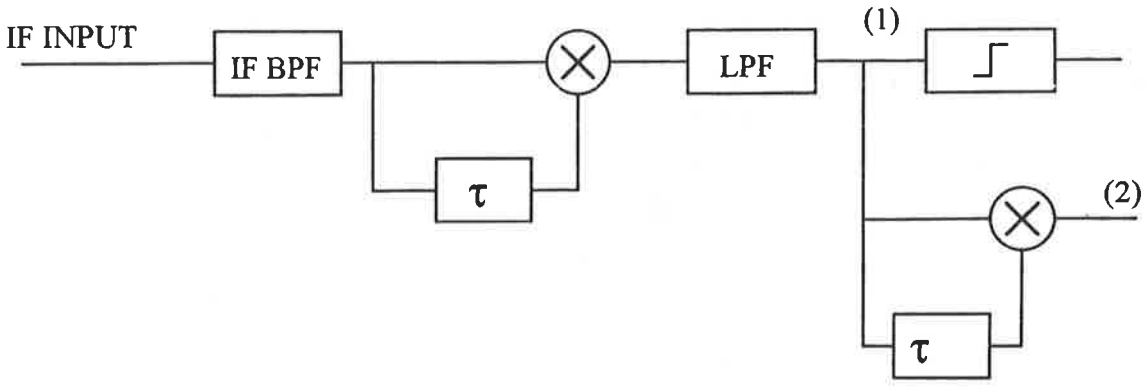


Figure 1 : Block Diagram of Discriminator Used In This Investigation.

(τ/T_b=1~2%)

The simulation and experimental results are shown in figures 2, 3 and 4.

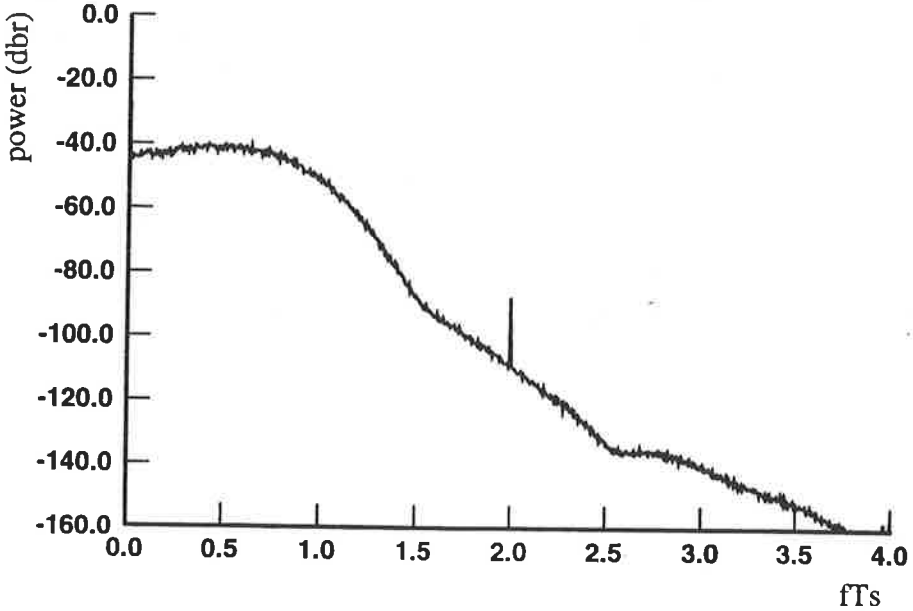


Figure 2 : Output Spectrum of Discriminator Detected FQPSK Signal at (1) in Figure 1. (Simulation)

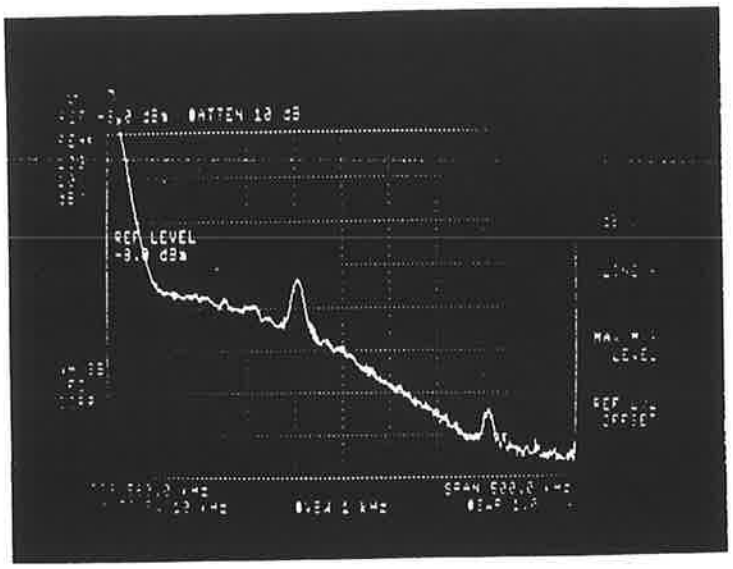


Figure 3 : Output Spectrum of Discriminator Detected FQPSK Signal at (1) in Figure 1. (Experimental)

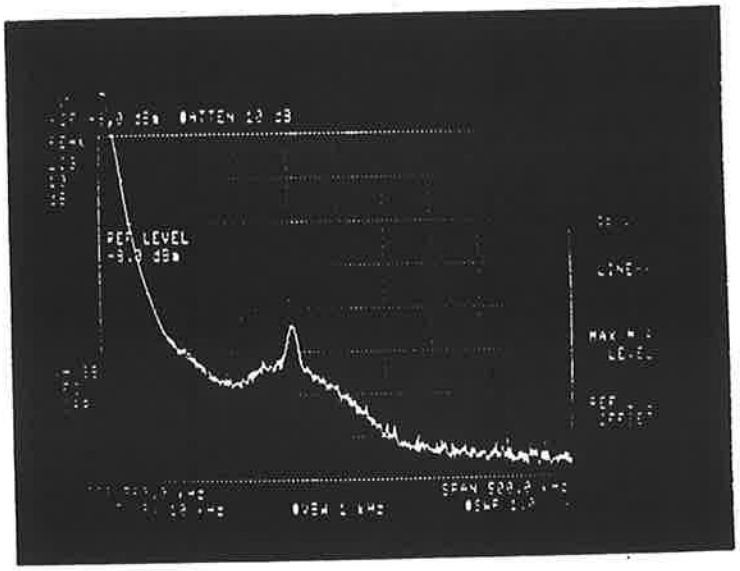


Figure 4 : Output Spectrum of Discriminator Detected FQPSK Signal at (2) in Figure 1. (Experimental)

The above figures show that the data clock can be recovered when FQPSK signal is discriminator detected.

Clock can be retrieved easily using STR :

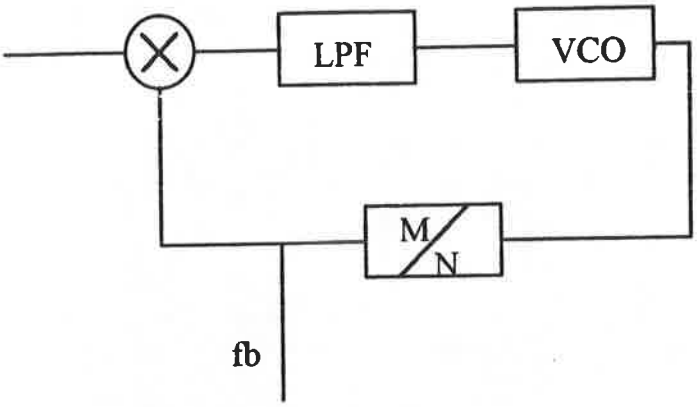
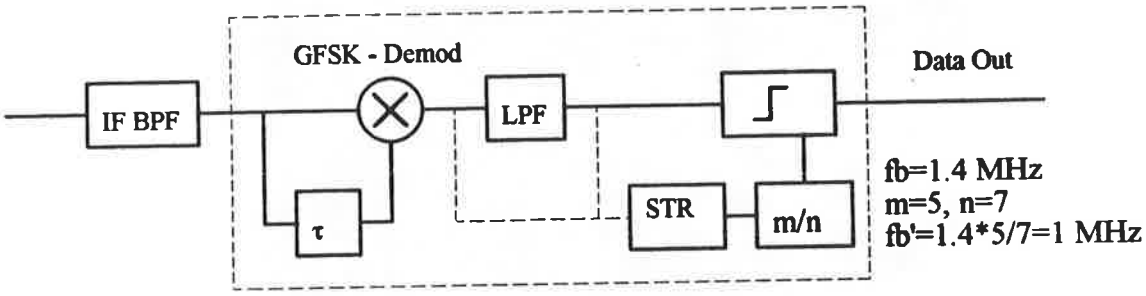


Figure 4 : Block Diagram of STR

Switching between 1 Mb/s (GFSK) and 1.4 Mb/s (FQPSK(kf,dj)) requires only interoperable simple frequency divider/multiplier.



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