IEEE 802.11
Wireless Access Methods and Physical Layer Specifications

TITLE: DC Balance and Edge Transitions
                   Their Impact on Data Recovery
                   and Overall LAN Performance

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Introduction

This paper looks at the properties of the NRZ data stream required by the physical layer to provide the proper services expected at the Physical Layer Service Access Point. These services include data recovery and more importantly, the capability of transmitting and receiving packets of every possible bit combination.

1.0   DC Balance and Edge Transitions

One of the terms commonly used to identify a property of a NRZ data stream is DC balance. This term is usually used to describe the number of 1's versus 0's which might occur in a given number of bits of data. A DC balanced NRZ stream will have a equal number of ones versus zeros. A stream with a DC balance of 60-40 indicates that the mix of ones and zeros might vary anywhere from 60% ones and 40% zeros to 60% zeros and 40% ones. The DC balance term becomes more useful to designers when the run length is also specified over which the DC balance is maintained. For example, a burst of 100 bits can have 50 ones and 50 zeros in a row, be balanced but only have one transition. This type of DC balance isn't really useful unless the system can withstand the run lengths of fifty ones and fifty zeros.

Edge transitions within the NRZ data stream are extremely important for the clock and data recovery circuit designer. Lots of transitions provide many opportunities for the clock recovery circuit to acquire the data clock and adjust and maintain the PPL. Frequent transitions also provide better insight in determining if the signal present is actually data or just noise, particularly in a wireless LAN implementation.

2.0   DC Balance and Edge Transitions in 802.11

In designing wireless LANs, our research has found that DC balance and edge transitions play an important part in the following areas:

- DC balance considerations can influence the design of the radio's transmitter and/or receiver

- Edge transitions will determine how quickly a clock and data recovery circuit can make a data or noise evaluation of a given signal

Design of either the radio transmitter or the radio receiver can be heavily dependent on the run length of ones or zeros allow within the NRZ data stream. We believe that radios can be designed to easily handle DC balances of 95-5 over a 18 bit period. This means that in any 18 bit period, a radio should be able to withstand a NRZ data run of 17 ones and 1 zero or 17 zeros and 1 one without introducing bit distortion at either the transmitting or receiving radio in a wireless LAN.

Clock recovery circuits need to see at least one transition to define a bit boundary and two or more to overcome boundary errors due to bit jitter. But more importantly, the maximum number of bits allowed between edge transitions determines how quickly the data recovery circuitry can determine if a given signal meets the requirements of the NRZ data stream or is simply just noise. The following equation describes the maximum time required to determine if a signal is noise or data:

2 x (max run length) + 1

This equation is derived using the following worst case scenario for a max run length of 17 bits:

1111111111111111110000000000000000001

In this example, clock and data recovery begins at the start of a run of 17 ones which end in a single transition to another run of 17 zeros. The seventeen zeros then terminate with a transition back to a one. This pattern meets the run length restrictions place on the NRZ data thus the signal should be evaluated as legitimate NRZ data. This example also shows that this determination must wait until the thirty fifth bit before being completed.

3.0   Meeting DC Balance and Edge Transition Requirements

Unfortunately, there is no good way to control DC balance or the minimum number transitions within a random NRZ data stream unless some type of operation is performed on the data. In the physical layer subworking group, two approach have been discussed and several more exist. The following summarizes the approaches:

- Scrambling   Apple presented papers (1)
- Block Coding
- Alternative coding schemes
- Fixed rate bit stuffing   Apple presented papers (2)

3.1 Scrambling. Several methods of scrambling have been previously discussed (1) which include the many advantages and disadvantages of scrambling. But no scrambling technique can guarantee that maximum run length or minimum edge transition requirements will always be meet for every random bit pattern of NRZ data. Most data transport systems which use scrambling do so knowing that a given pattern of data more often appears in the media than others and design scramblers to break up these patterns. For example, ATM uses a scrambler to break up the longs runs of zeros which makeup null cells. This long string of zeros can fool the cell delineation system at startup and whenever cell delineation is lost during normal operation. But clock recovery and signal determination are not based upon the impact of the scrambler on the data stream.

For the most part, scrambling moves the run length problem from one set of bits to another set of bits. This is a somewhat a win if there is a likelihood that one pattern appears much more often then another but it doesn't address the case when that pattern does occur. In other words, how do you get a data pattern through the system which violates the DC balance properties of your transmitter or receiver?
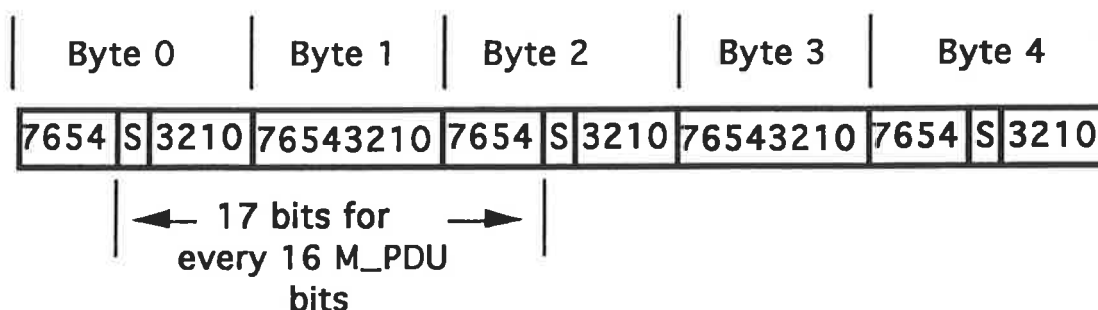
3.2 Block Coding. One method which can guarantee compliance of run length and edge transition requirements is block coding. Two popular blocking coding schemes are 4B5B and 8B10B. In the 8B10B block coding scheme, a byte of data is represented by a 10 bit code when transmitted over the media. Block codes have many advantages along with several disadvantages. Some of these advantages and disadvantages are as follows:

Advantages	Disadvantages
Single bit error detection	Data expansion of 25%
Small maximum run lengths	Error aliasing
Code point distances of 2 or more	Error multiplication
High transition densities	Large Coding tables
Predictable DC balance properties	

3.3 Alternative Coding Schemes. Another solution to the problem might be to move from NRZ toward other coding schemes such as Manchester, etc. The problem with many of these other coding schemes is that nothing comes for free. Each scheme has a penalty in terms of bandwidth, sensitivity, error multiplication, etc., much like the table listed in 3.2.

3.4 Fixed Rate Bit Stuffing. Fixed rate bit stuffing as discussed in a previous paper by Apple is a way of guaranteeing transitions and run lengths by adding a 17th bit to every sixteen bits of data which is the inverted sense of the bit preceding it. Apple originally proposed a 32 bit / 33 bit fixed bit stuffing system which most felt was a little too long for most radio designs. A 16 bit / 17 bit fixed stuffing rate proposal makes more sense when considering the effect run lengths have on the time required to do signal assessment of data versus noise.

3.4.1 Fixed Rate Stuffing Proposal. I believe that the solution to guarantee any DC balance and edge transition requirements is to use fixed rate bit stuffing. The proposed scheme as shown in figure 1 uses a 16 /17 bit fixed rate bit stuffing approach. This scheme inserts a bit, starting after bit 4 in byte 0 of the MPDU, which is the inversion of bit 4, in every other byte in the data stream.

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4

| 7654 | S | 3210 | 76543210 | 7654 | S | 3210 | 76543210 | 7654 | S | 3210 |

◄── 17 bits for ──►
every 16 M_PDU
bits

S = ~bit 4 of every n*2 bytes

16 Bit / 17 Bit Fixed Bit Stuffing
Figure 1

The results of this bit stuffing is a worst case pattern as follows :

- 011111111111111111000000000000000001

This pattern represents the lowest frequency (least transitions) which could occur in the NRZ data stream. It also represents the longest run length of zeros and ones. In addition, this example shows the worst case dc balance over 18 bits to be 17 and 1 or about 94-6. Using the equation developed in section 2.0, the maximum time required to do a signal assessment of noise versus data is 35 bit times or 35 usec in using a 1.0 MHz bit clock.

1. IEEE Doc 802.11-94/018, "Proposals for a Burst Protocol to be Used in Various Wireless Data Transport Protocols", Ed Geiger.

2. IEEE Doc 802.11-93/216, " A Look at Some Scrambling Techniques Used in Various Data Transport Protocols", Ed Geiger