# IEEE 802.11
## Wireless Access Method and Physical Specification

Title: **Low Power Implementation of FQPSK Chip for Infrared and other Wireless Systems**

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**Abstract**

A low power, single chip implementation and experimental results of a FQPSK baseband modem processor suitable for the proposed 1 Mb/s to 10 Mb/s EXIRLAN (**Ex**pandable **I**nfrared **L**ocal **A**rea **N**etwork) PHY specification [ref 1-7] are presented. This design features a single field programmable gate array (FPGA) solution that provides a path to practical, low cost production. The design was tested at 1 Mb/s and 4 Mb/s and consumed **less than 35 mW of active power** with a typical **standby power of less than 150 µW**. Carrier modulated test results performed at 10 MHz show high spectral efficiency in a non linear amplified (NLA) infrared channel--supporting the combined baseband and multichannel proposal [2]. The same device can also be reconfigured in-circuit via microprocessor over an IEEE 1149.1 JTAG interface to implement other modulated baseband signals and supports data rates **up to 16 Mb/s** at 8 samples/symbol. This design performs similar in function to the VLSI implementation proposed by Soderstrand [8] and provides a **practical solution for the first generation of EXIRLAN systems** when combined with a currently available, low power baseband analog ASIC [9].

## I. Introduction

The baseband and carrier modulated methods currently being standardized by the IEEE 802.11 Wireless Local Area Network committee promise lower-cost, portable communication devices. FQPSK, a constant envelope modulation technique, provides a carrier modulated signal that is free of *inter-symbol interference* (ISI) and *timing jitter*, and has been shown to provide up to 1.6 b/s/Hz spectral efficiency in a *nonlinearly amplified* (NLA) channel found in infrared systems [7]. Yet, little has been published on low power, cost effective, and practical designs. Soderstrand [8] demonstrated a VLSI implementation of a FQPSK-KF baseband modem processor and digital filter that consumes 150 mW--an impressive achievement for high volume production, but not a practical solution for prototyping first generation systems. Blomeyer [3] also reviewed implementation of EXIRLAN systems. Neither solution provides the combination of both low power and practical packaging, with the added flexibility of in circuit reconfiguration that is offered by SRAM based field programmable gate array (FPGA) technology--a desirable trait for prototyping new designs and reducing the time-to-market.

This report presents a low power, single-chip FPGA hardware implementation and experimental measured performance of a differential encoded FQPSK-1 baseband modem processor in a nonlinearly amplified infrared communications channel. It shows a technique, using currently available FPGA technology, that can implement a variety of modulation schemes up to 16 Mb/s with a power consumption of less than 35 mW at 1Mb/s and typical standby power of 150 μW.

## II. FQPSK-1 Baseband Processor

Figure 1 shows the block diagram of a FQPSK carrier modulated system.

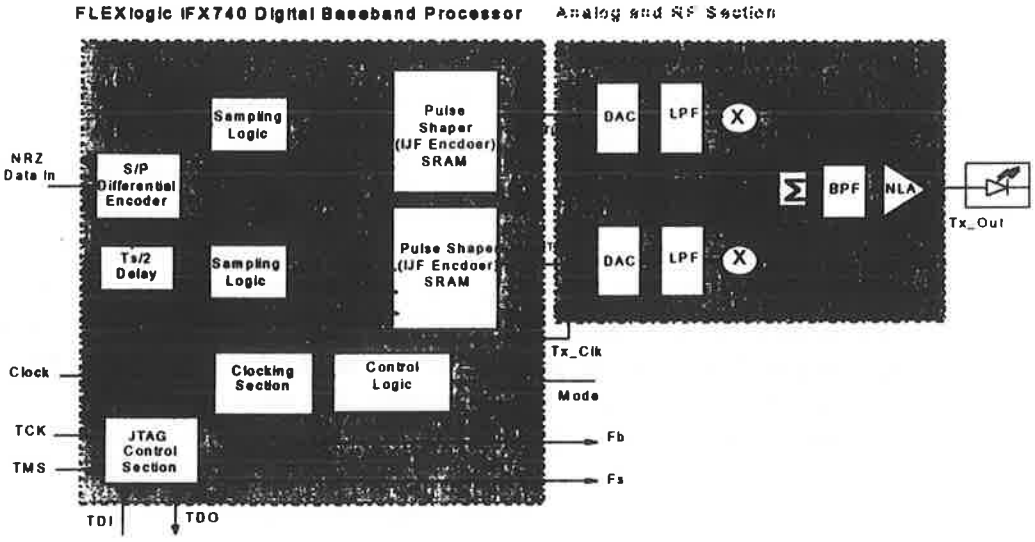


Fig 1. FQPSK Modulator Block Diagram

The non-return to zero (NRZ) binary input data stream is converted into independent I and Q channel digital signals known as symbols with a rate equal to one half the NRZ data rate ($T_s=2T_b=2/f_b$). Following this serial to parallel conversion, the digital symbols are differentially encoded to accommodate demodulation by conventional carrier recovery free offset-QPSK (OQPSK) receivers. The I and Q channel signals are then processed by the FQPSK pulse shaping filter.

The FQPSK pulse shaping has been shown to be free of ISI interference and timing jitter [10] and is often referred to as inter-symbol interference jitter free (IJF) encoding. The IJF encoding is achieved by means of a look-up table in memory according to the present and past state of the I/Q channel. Each symbol is quantized into a digital representation of a half cosine wave. Table 1 shows the look-up table function for generating the baseband FQPSK-1 signal.

| NRZ Input Data | | Output Signal (pulse shape function) |
|---|---|---|
| Past I/Q State | Present I/Q State | FQPSK-1 |
| -1 | -1 | $y_1(t) = 0$ |
| -1 | 1 | $y_2(t) = -\cos(\pi t/Ts)$ |
| 1 | -1 | $y_3(t) = \cos(\pi t/Ts)$ |
| 1 | 1 | $y_4(t) = 1$ |

Table 1. Baseband Signal Look-Up Table

By changing the pulse shaping function it is easy to implement various other quadrature modulation schemes; some of which include MSK, SQAM, OQPSK, and TSI. Various other baseband modulation techniques can also be supported by reconfiguring the FPGA logic in-circuit via a four wire JTAG interface--more on this latter.

The amount of memory required to hold the pulse shape function depends on the number of samples/symbol and digital quantization levels.

## III. Baseband Quantization

### A. Quantization Levels and Sampling Rate

Quantizing is the process of representing the continuous analog baseband signal with a set of discrete states [or levels]. The *resolution* of the quantizer is the number of states expressed in bits. The number of states for binary coding is $2^n$, where n is the number of bits [or steps]. The *sampling rate* ($S_r$) is the number of times the signal is sampled (or converted) in a time period equal to the symbol rate. Therefore, 10-bit quantization with 16 samples/symbol has 1024 states ($2^{10}$) and requires memory storage for the four 16 x 10 bit pulse shapes, or 64 x 10 bits.

**NOTE: Less memory storage can be achieved using up/down counters as suggested by Soderstrand [8], but this requires additional logic that consumes power. The chose depends on the target FPGA or ASIC architecture.**

Consider the specific case of a 11001100... NRZ data input data stream to a FQPSK modulator. The quantized baseband signal is a "stair-case" sinusoidal signal with a period equal to twice the symbol period (Figure 2). It should be noted that 11001100... is the worst case condition for a FQPSK quantizer and not 101010... which generates a steady state high- or low-level baseband signal.

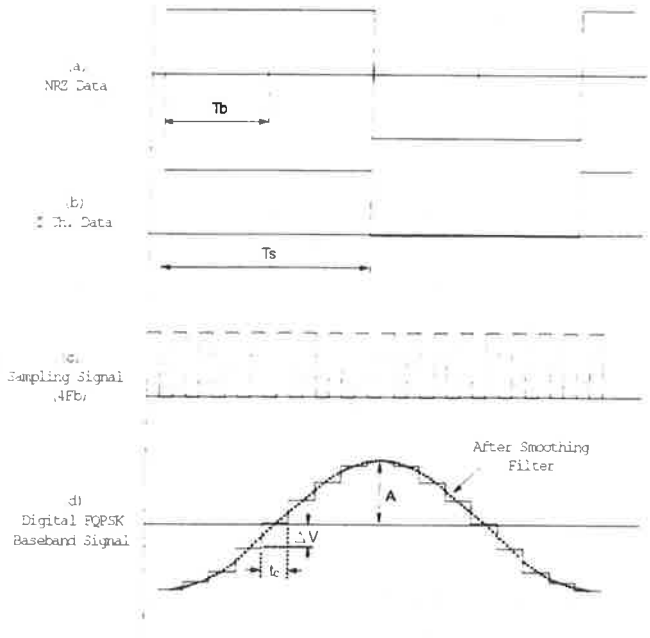


Fig 2. Sampled Baseband Signal

After a proper smoothing filter (LPF) this "stair-step" error is effectively eliminated.

Soderstrand [8] used a 16-sample, 12-bit resolution to represent the FQPSK signal. The constant level baseband waveforms, $y_1(t)$ and $y_4(t)$, allow FQPSK to achieve low quantization error with fewer quantization levels--reducing power consumption and gate count, while maintaining the highest possible data rate.

## B. Performance in a Non Linearly Amplified Infrared Wireless Channel

Figure 3 shows the out-of-band power spectrum for FQPSK-1 in a hard limited channel sampled 8 times per symbol period with various resolutions. Identical spectral performance is achieved better than -55 dB relative to the carrier frequency power when using 8-sample, 8-bit resolution when compared with higher resolution (10- or 12-bit) and satisfy the proposed spectral template and *adjacent channel interference* (ACI) requirements [5]. For this design 8-sample, 8-bit resolution was implemented and tested using the Intel iFX740 field programmable gate array technology.

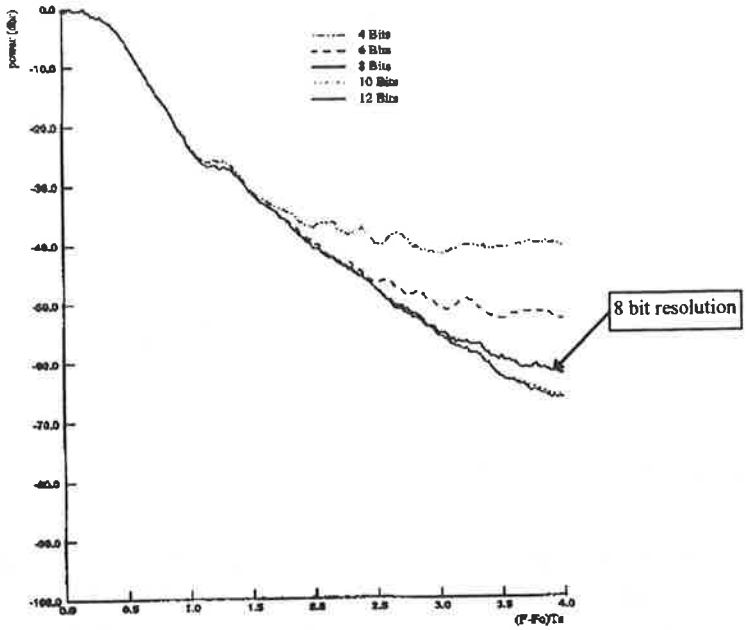


Fig 3. Quantized FQPSK NLA Out-of-Band Power Spectrum, 8 samples/symbol
[8-bit resolution provides identical performance as 10- or 12- bit system to within -55 dB rel]

## C. Bit Error Rate Performance

Figure 4 shows the simulated bit error rate (BER) performance for FQPSK sampled 8 times per symbol period with various resolutions. As expected, the resolution does not effect BER performance. The results are within 0.5 dB of theory--providing a robust transmission medium

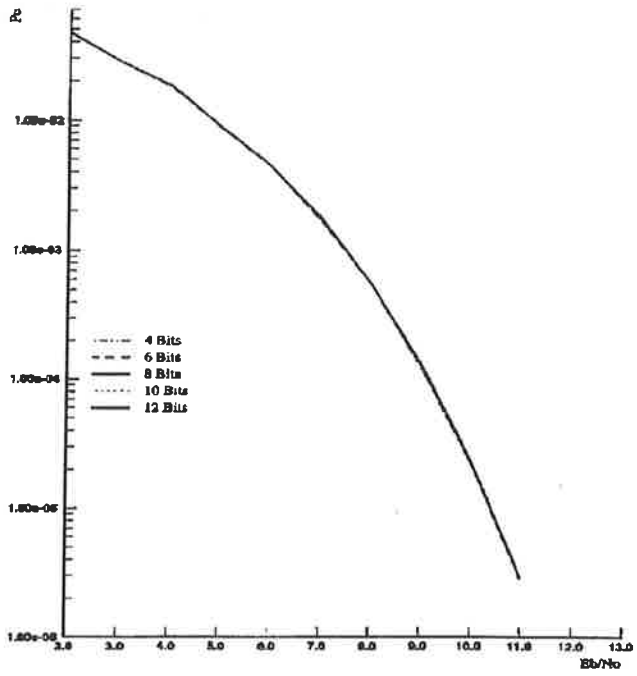


Fig 4. Quantized FQPSK BER Performance
(4th order Butterworth Rcv. Filter with $Bt_b$=0.55)

## IV. FQPSK Modem Implementation

Figure 5 shows the block diagram of the FQPSK Modulator. A master oscillator, with a clock frequency equal to four times the input date rate (4 MHz for a 1Mb/s input data stream), provides synchronization for the *pseudo random binary sequencer* (PRBS) and baseband processor.

A *phase lock loop* (PLL) provides a phase lock between the data source and PRBS generator. The PRBS encoding eliminates DC components and discrete spectral lines in the spectrum. The PRBS clock equals the data rate (1MHz) and is generated by a clock divider network located in the baseband processor.

Using the IEEE 1149.1 JTAG interface, the baseband processor, implemented in a FPGA, is reconfigured in-circuit for various modulation schemes, encoding techniques, and quantization levels. The digital baseband signals are then converted to an analog waveform by the DAC, passed through a smoothing low-pass filter and quadrature modulated at a carrier frequency of 10 MHz.

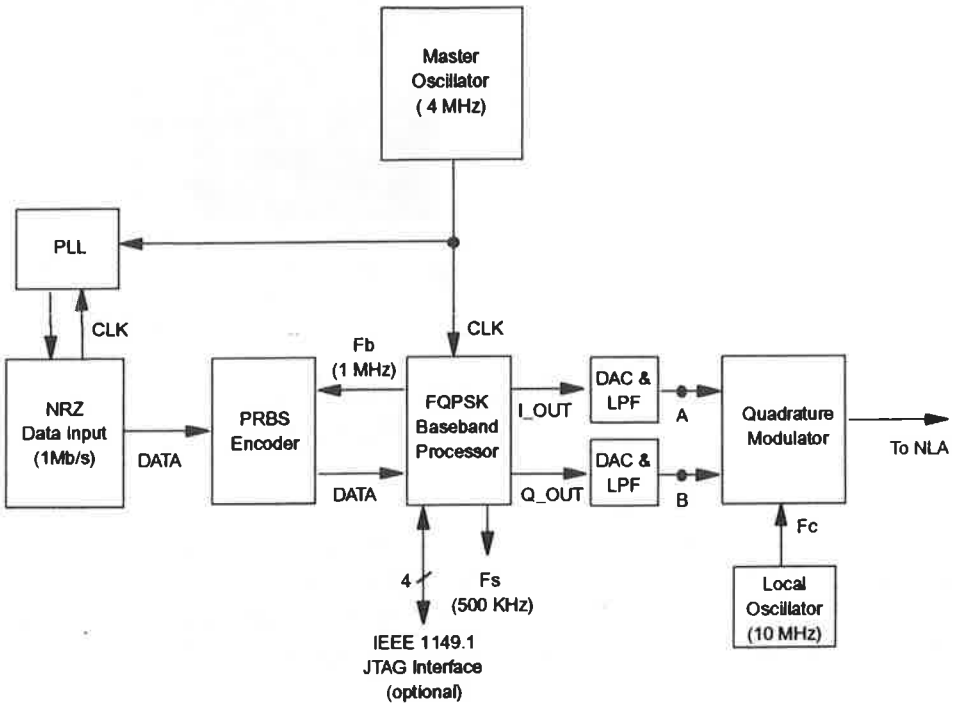


Fig. 5. FQPSK Modualator Block Diagram Design

The baseband processor consists of a serial-to-parallel converter, differential encoder, clock divider, address counter, and SRAM (ROM) look-up table.

**B. FPGA Design Details**

The complete digital baseband processor for FQPSK, MSK, SQAM and OQPSK was implemented in a single Intel iFX740 FPGA chip (Figure 6). The iFX740 is based on an Intel 0.8µ CHMOS EPROM/SRAM technology--providing 80 Mhz external clock rates and high speed 10 nS pin-to-pin delays. The iFX740 was chosen because of its ready availability, reasonable cost, low power and flexible on-chip SRAM.

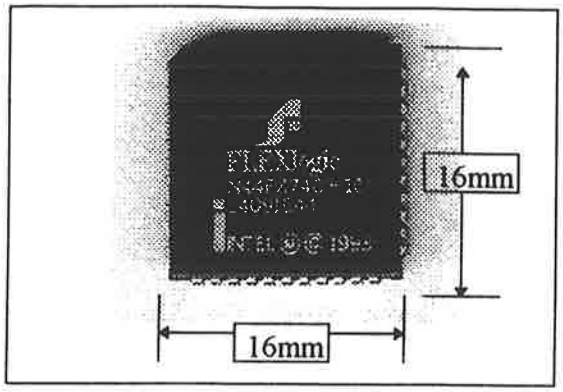


Fig 6. Intel iFX740 FPGA Chip
(44-pin PLCC Package)

Figure 7 shows the block diagram of the iFX740 FPGA. The device consists of configurable function blocks (CFBs) interconnected by a global matrix. Each CFB can be defined as a 24V10 block of digital logic or a block of 128 x 10 SRAM--ideal for the pulse shaping function. Each CFB provides 10 macrocells [D registers with AND-OR logic] for a total of 40 macrocells providing approximately 1,700 gates of logic [11].

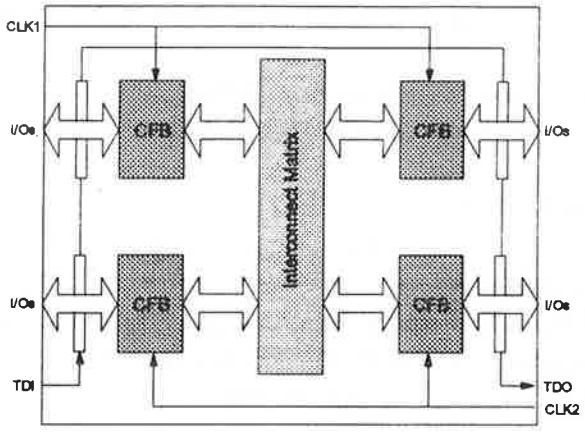


Fig 7. iFX740 Architecture
**(Configurable Function Blocks with Interconnect Matrix)**

The design uses 33 macrocells for logic and SRAM, consuming 63% of the device resources, and dissipating less than 35 mW power at a 1 Mb/s data rate.

The design employed a standard design process. The Viewlogic™ PRO Series [12], a Windows™ based software package, was used for schematic capture and timing simulation. The design was fit into the FPGA using the Intel FLEXlogic Fitter integrated into the Viewlogic™ tool.

Figure 8 (page 16) shows the schematic design of the digital baseband processor generated by the Viewlogic™ tool.

There are three inputs (appearing on the left side of the schematic):

1. **DATA_IN** - The NRZ data input signal,
2. **CLK_IN** - The master oscillator clock equal to four times the data input bit rate, and
3. **MODE[2:1]** - The two bit mode signal that selects the modulation technique.

There are also four outputs (appearing on the right side):

1. **FS_OUT** - The symbol rate output clock signal--to synchronize test equipment for eye-diagram measurements.
2. **FB_OUT** - The bit rate output clock signal--to synchronize the PRBS data generator,
3. **I_OUT[7:0]** - The eight bit I channel output, and
4. **Q_OUT[7:0]** - The eight bit Q channel output.

The functions of the baseband processor include clock division, serial-to-parallel conversion, differential encoding, Ts/2 data offset, and addressing of the SRAM look-up table. The clock divider consists of a series of D-type registers, each driven by their respective inverted outputs (see Figure 8). The master oscillator frequency is divided four times to produces the necessary *bit rate clock*, *Fb*, and *symbol rate clock*, *Fs*.

The NRZ input data is converted into the I and Q channels and differentially encoded. The *Ts*/2 data offset is achieved by clocking the Q channel register by the inverted symbol rate clock.

The I and Q channel signals drive two separate Pulse Shaper circuits shown in Figure 9 (page 17). The pulse shaper consists of 128 x 10 bit SRAM, state latch register, and 3-bit synchronous counter.

The SRAM is configured using one of the FPGA configurable function blocks (CFBs). The size was chosen because of the default SRAM size implemented in this FPGA and the desire to store four 32-byte pulse shapes--allowing four different quadrature modulation techniques to be tested

**NOTE: Only 32 x 8 SRAM is needed to support FQPSK-1 using 8-bit resolution and 8 samples/symbol.**

The MODE[2:1] signal drives the two most significant bits of the SRAM (A[6:5]) and is used to select the pulse shaping function, 32-bit memory bank.

To generate the digital 8-bit I and Q channel baseband signals, the equations listed in Table 1 are converted to 8 bit HEX values that are programmed into the on-chip PROM that preloads the SRAM cells upon power-up. The past and present state of the I/Q channel drive the A[4:3] address bits that select one of the four waveshapes, $y_1(t)..y_4(t)$. Once selected, the synchronous counter drives the three low significant bits (A[2:0]) and counts through the 8-step quantization samples. The output of the SRAM is latched and held for the transparent D/A converter. The conversion occurs eight times per symbol period.

The maximum data rate supported by the FPGA is given by

$$Fb_{\max} = 2Fs_{\max} = 2 / S_r t_{RC} \quad (1)$$

where $t_{RC}$ is the *read cycle time* of the SRAM. For the iFX740-10 FPGA the on-chip SRAM $t_{RC}$ is 15nS. At a sample rate $S_r$ = 8 samples/symbol, $fb_{\max}$ is 16.67Mb/s.

The output of the I/Q DAC is feed through a first order smoothing low pass filter, see Figure 1. The modulated signal is mixed with a 10 MHz carrier and amplified by the NLA.

Non Linear Amplification is achieved by driving the RF amplifier into saturation. Often referred to as Class-C operation, this method achieves improved power efficiency--providing longer battery life for portable systems.

**NOTE: Non Linear Amplification causes spectral regrowth and requires a constant envelope modulation technique like FQPSK.**

### C. FQPSK Receiver/Demodulator

Figure 10 shows the block diagram of a FQPSK receiver. The receiver is divided into an analog and RF section and digital baseband demodulator. For test purposes the receiver was constructed using existing discrete components. A post low pass filter (LPF) threshold detection technique decodes the demodulated signal to recreate the encoded baseband signals.

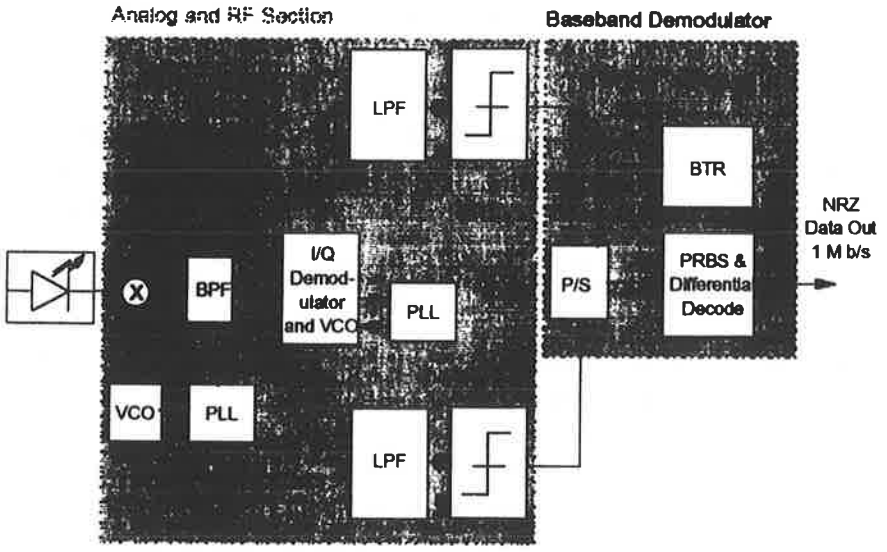


Fig 10. Receiver Block Diagram

### D. Low-Power Analog ASIC Designs

Blomeyer presented an FQPSK transmitter/receiver design using existing commodity components [3]. This provides a practical prototyping solution, but modulated carrier EXIRLAN systems will require low power analog and RF components. Such requirements have been addressed by ASIC designs such as the Qualcomm Analog and RF ASIC [9] that is used in portable cellular designs today. Figure 11 shows the block diagram of this ASIC.

This part replaces several discrete components--saving board space and reducing power. The Qualcomm ASIC was designed on a 1μ bipolar process. Offered in a 64 pin Thin Quad Flat Package (TQFP), the part consumes 385 mW at 5 volts in full transmit and receive operation [9].

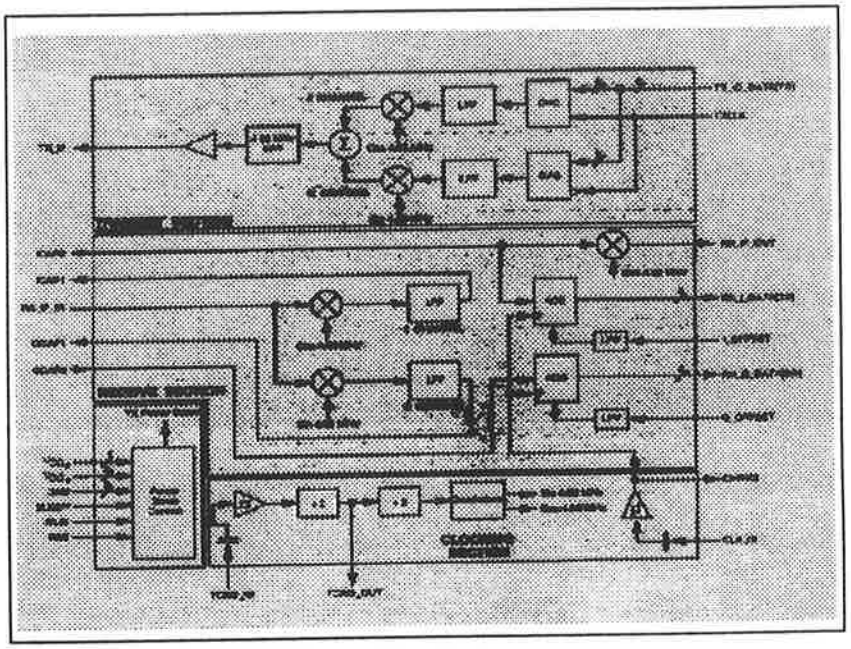

Fig 11. Analog and RF ASIC

## V. In-Circuit Reconfiguration

The iFX740 FPGA utilizes the IEEE 1149.1 JTAG interface to support boundary scan and in-circuit reconfiguration and programming. The most common application of boundary scan is for identification of assembly errors during manufacturing. Another benefit of JTAG is to reduce prototype time and improve the overall time to market [13].

The JTAG interface consists of a four signal, serial interface:

1. **TDI** - The Testability Data Input used to shift instructions and data into the FPGA.
2. **TDO** - The Testability Data Output is the serial instruction and data output from the FPGA
3. **TCK** - The Testability Clock input used to clock the instructions and data into and out of the FPGA.
4. **TMS** - The Testability Control Input used to select the test mode.

Through the JTAG interface, data is shifted into instruction registers in the FPGA. Based on the instruction and data loaded, the FPGA logic may be reconfigured in-circuit.

In designing and developing the modem described in this paper, JTAG was used to reconfigure the FPGA numerous times--eliminating the need for a device programmer and greatly reducing the development time.

The method used was a prototyping cable connected between a standard IBM compatible PC parallel port and the system board. The PC acts as a JTAG Test Access Port (TAP) controller and drives the JTAG interface. Using the prototyping cable and the PENGN program [11] design changes where recompiled and shifted down the cable--reconfiguring the device in a matter of minutes.

This technique also allows for other modulation schemes, such as $\pi/4$DQPSK and FQPSK-KF, to be quickly implemented and tested.

## VI. Experimental Results

### A. Baseband Eye Diagram

Measured I and Q channel baseband signals at the transmitter (test points A & B in Figure 5) are shown in Figure 12. The differential encoded data rate is 1 Mb/s. The resulting FQPSK signal contained neither ISI nor timing jitter.

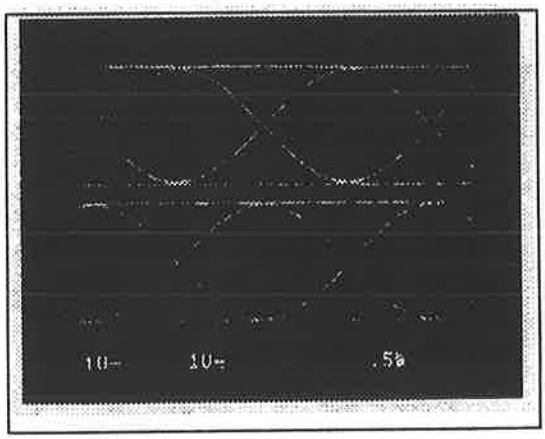

Fig 12. FQPSK-1 Eye Diagrams Measured at the Transmitter
(Fb=1 Mb/s, no ISI nor jitter)

**B. Constellation Diagrams**

The space constellation diagrams (Figure 13) shows reduced envelope fluctuation for FQPSK.

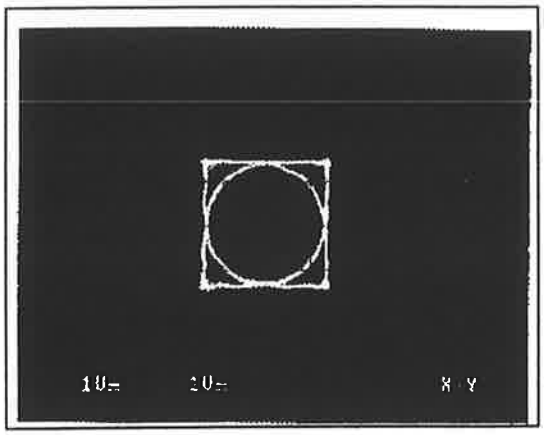

Fig 13. Space Constellation Diagram Measured at Transmitter
(1 Mb/s, Measured at Points A & B in Figure 5)

**C. Power Spectrum**

Figure 14 shows the power spectrum of FQPSK-1 carrier modulated signal, measured at the output of the NLA. FQPSK showed the least spectral regrowth when compared to other carrier modulated techniques, such as OQPSK and MSK which caused interference to adjacent channels.

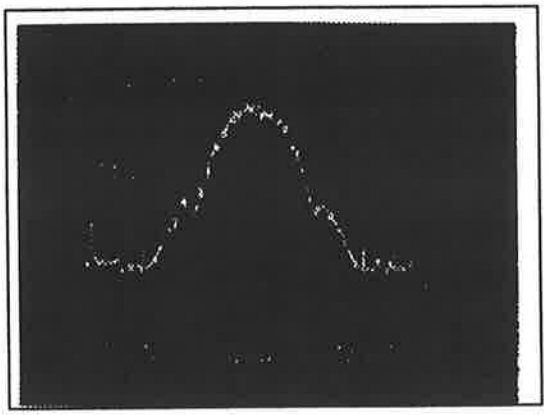

Fig 14. FQPSK Out-of-Band Power Spectrum
(Fb = 1 Mb/s, Fc = 10 Mhz, Span = 3Mhz, RBW=3kHz)

**D. Demodulated Eye Diagram**

Figure 15 shows the demodulated FQPSK eye diagram measured at the input of the threshold detectors in a hard wired channel with fourth order Butterworth LPF in the receiver.

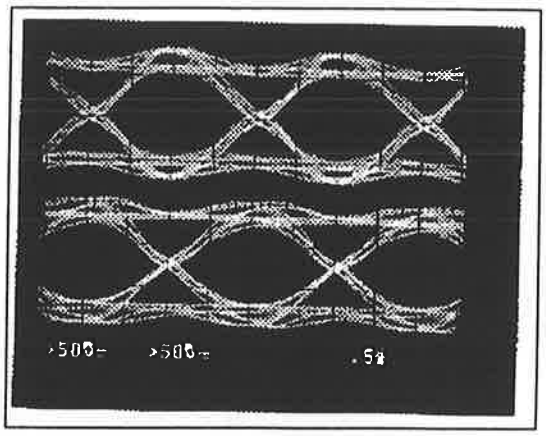

Fig. 15. Demodulated FQPSK Eye Diagram
(Fb = 1 Mb/s, 4th Order Butterworth LPF with BT = 0.55 (270kHz))

**E. Power Consumption**

The CMOS based iFX740 is well suited for low power applications. The on-board PROM memory (containing the system configuration and table look-up contents) is loaded into SRAM configuration cells during the power-up cycle that completes by the time Vcc = 4.75V for a monotonic Vcc rise (slew rate > 1V/mS). Once the configuration is loaded, the PROM is turned off--providing low power, fast logic with SRAM look-up.

The baseband processor was found to consume from 35- to 145-μW during standby (7- to 30-μA at 5V with 0 MHz data input). This is well within the maximum specified value for the device and exceptional for portable applications.

Table 2 shows the power consumption of the active baseband processor measured on two iFX740 parts from different manufacturing lots. At 1 Mb/s the power consumption of was found to be less than 35 mW.

| | | Power Consumption | |
|---|---|---|---|
| **Data Rate (Mb/s)** | **Master Oscillator (MHz)** | **Lot # V3471001 Nov. '93** | **Lot # L4091644 Feb '94** |
| standby | 0 | 35μW | 145μW |
| 0.1 | 0.4 | 4.0mW | 12.0mW |
| 0.25 | 1.0 | 9.0mW | 17.5mW |
| 0.5 | 2.0 | 17.5mW | 19.5mW |
| **1.0** | **4.0** | **34.0mW** | **24.0mW** |
| 2.0 | 8.0 | 60.0mW | 29.5mW |
| 4.0 | 16.0 | 132mW | 46mW |
| 5.0 | 20.0 | 176mW | 57mW |
| 10.0 | 40.0 | n/a | 103mW |

Table 2. Active Power Consumption
(Vcc = 5.0V at room temperature, Measured Icc + Icco)

The iFX740 also supports 3.3V programmable I/O that is well-suited for mixed voltage designs and provides reduced power consumption.

## VII. Conclusions

FPGA technology provides a low-power, flexible means to implement FQPSK for the proposed EXIRLAN Wireless Local Area Network. An 8-sample quantization of the baseband signal with 8-bit resolution was found to provide nearly equal power spectrum and equal BER performance as achieved by higher resolution techniques. The reduction in quantization levels reduces the amount of digital logic and conserves power--allowing implementation in a smaller FPGA device.

Experimentally measured eye diagrams show IJF modulation was achieved. In a NLA channel the 8-bit resolution FQPSK baseband processor, consumed less than 35 mW at 1 Mb/s, showed spectral compactness, reduced spectral regrowth, and supported data rates greater than 10 Mb/s.

The results also show the ability to quickly and easily implement various other modulation techniques by reconfiguring the FPGA in-circuit through the IEEE 1149.1 JTAG interface. A technique that can support remote field service.

In conclusion, this paper demonstrates a low power consuming, high-speed, and flexible FQPSK baseband processor that provides a **practical solution for the first generation of EXIRLAN systems**.

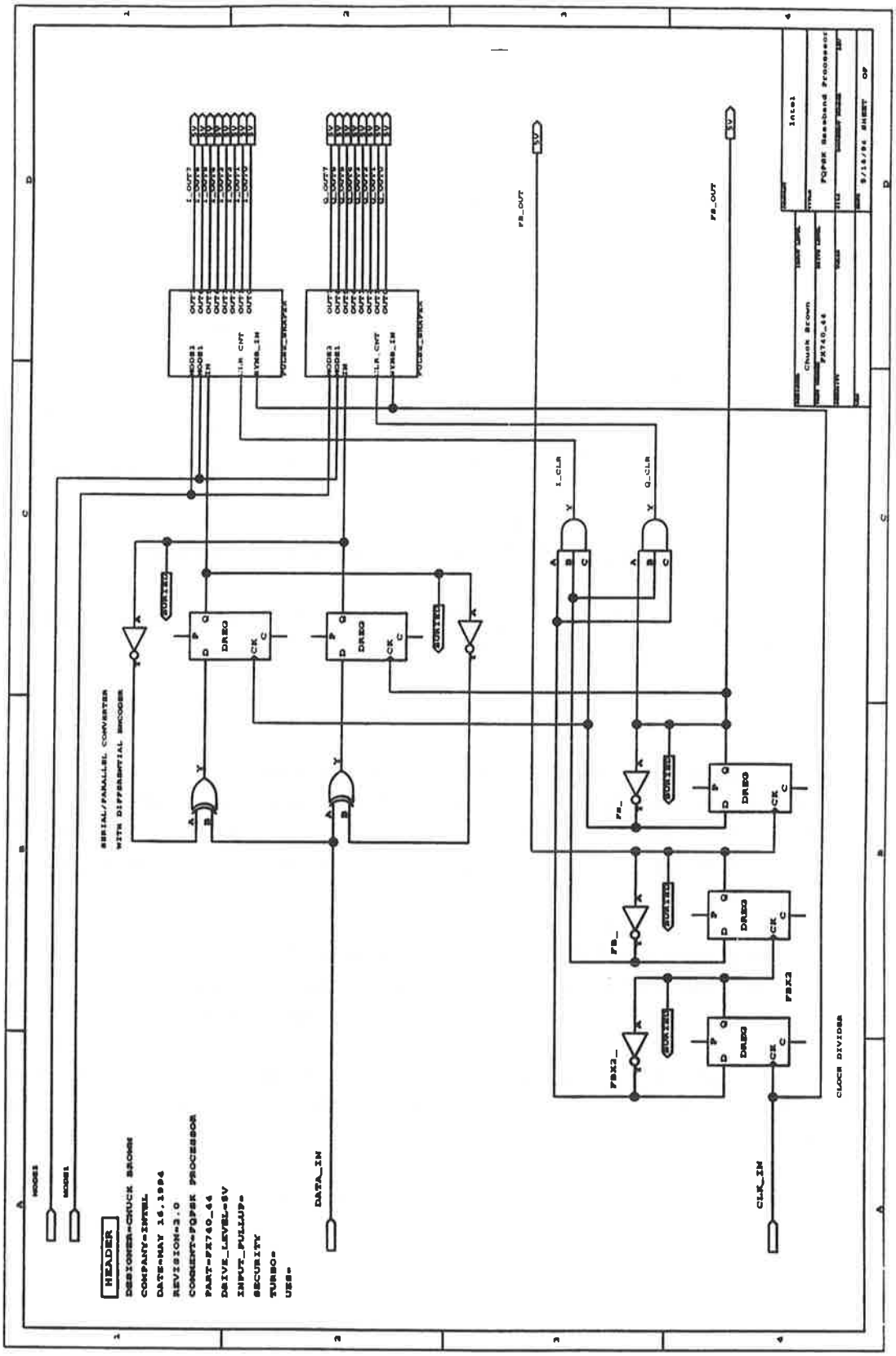


Fig 8. Digital Baseband Processor

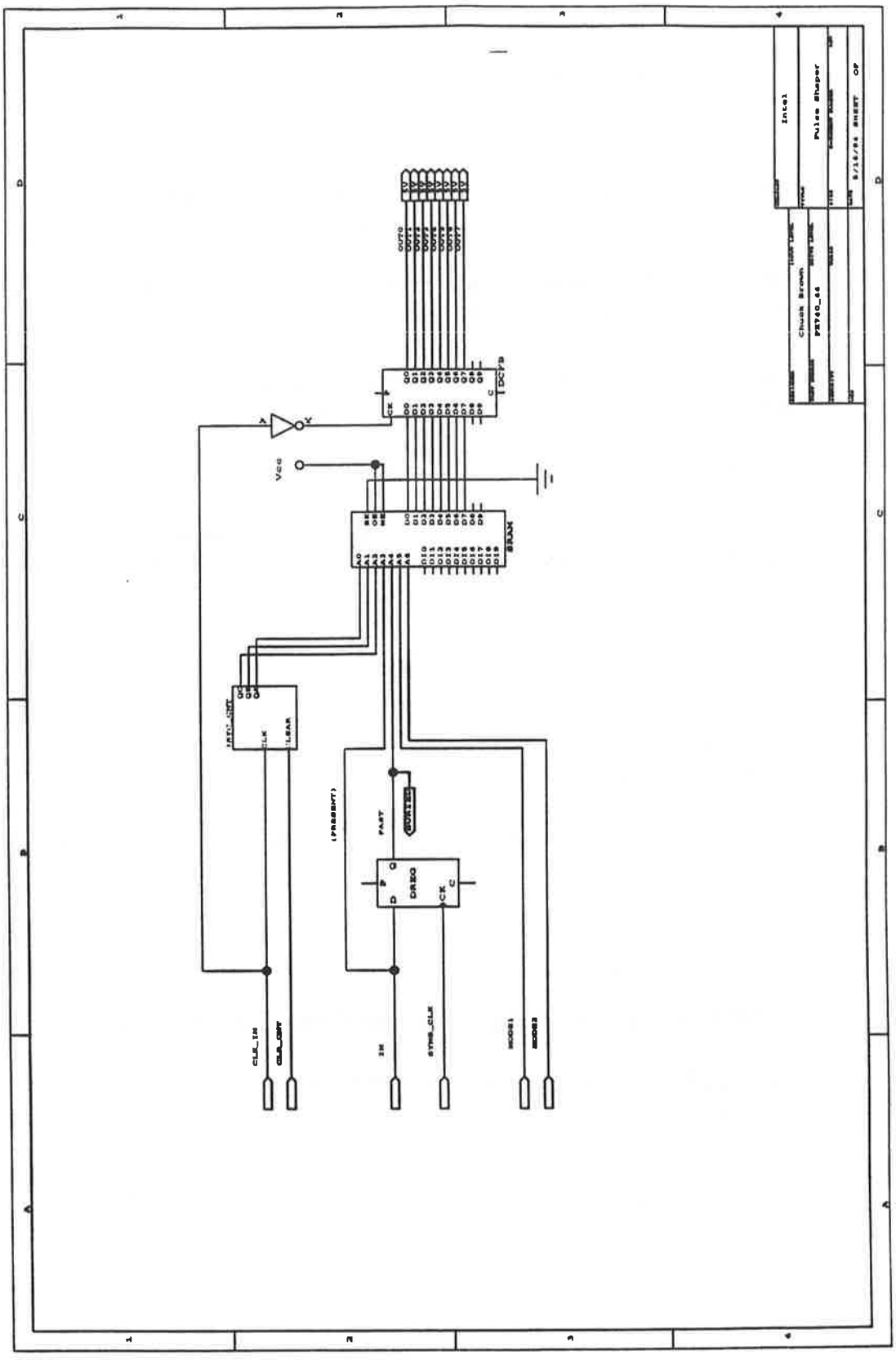


Fig 9. Pulse Shaper

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