IEEE 802.11 Wireless Access Method and Physical Specification

Title:

Proposed Revision to 94/068

Section 4: FHSS PMD Sublayer

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ABSTRACT:

This submission contains a proposed revision of section 4 of the FH PHY working draft standard as represented by document 94/068. Every attempt has been made to keep the proposed changes in this submission non-controversional.

All text additions are based from 93/083. Certain headings which are stated as OPEN have additional text and figures associated with it; the objective of the text and figure is to provide an explanation of the proposed specification heading. Note that even if the proposed revisions are adapted to replace those counterparts in section 4 of 94/068, the modifications are still subject to detailed review and section-by-section voting by the FH PHY subgroup before presenting to the PHY group and the full 802.11 plenery.

Additions are identified by underlines; deletions by strike-thrus. Paragraph numbering changes are not marked. All other corrections are presented by a combination of deletions and additions.

Modification 1: Rewording Section 4.7.4

4.7.4 Occupied Channel Bandwidth (CLOSED per A.3) The occupied channel bandwidth for the PMD is 1.0 MHz wide as specified at the -20 dB points of the associated signal spectrum. This 1.0 MHz envelope must contain 99% of the emitted energy as channel is measured at the +/- 500 kHz frequency limits from the specified operating center frequency listed in section 4.7.3. The following diagram illustrates the relationship of the operating channel center frequency (defined as F_C) to the occupied channel bandwidth.

Modification 2: Additional PMD Operating Specifications General Headings Based on 93/068

4.7.11 Channel Switching/Settle Time (OPEN) The time to change from one operating channel frequency, as specified in section 4.7.3, is defined as TBD microseconds. A conformant PMD is said to meet this switching time specification when the desired final operating channel center frequency hs settled to within +/- TBD kHz of the operating channel center frequency as outlined in section 4.7.3.

(NOTE: To add more verbage to specify the conditions for switching. Maybe add a graph to clarify)

4.7.12 Transmit to Receive Switching Time (OPEN)

To add verbage once closed.

4.7.13 Receive to Transmit Switching Time (OPEN)

To add verbage once closed.

4.7.14 Operating Channel Availability (Closed per PAR) A conformant PMD must provide availability to each operating channel center frequency at least 99.5% of the time with no interference present in the occupied operating channel bandwidth.

4.7.15 Antenna Port Impedance/VSWR (Open)

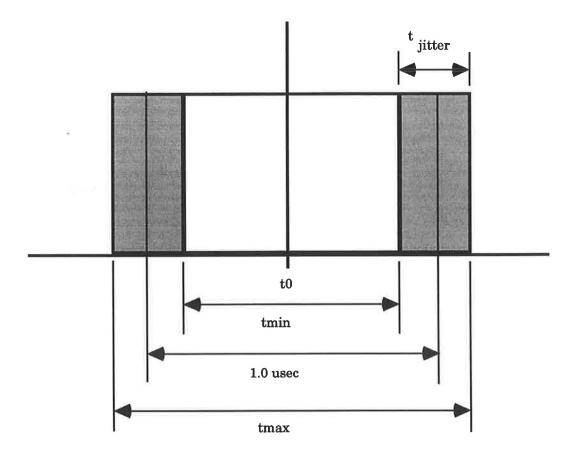
Modification 3: Additional PMD Transmitter Specifications Headings Based on 93/068

4.8.5 Amplitude Envelope Window (Closed November 1993)

Add verbage.

Modification 4: Additional PMD Receiver Specifications Headings Based on 93/068

4.9.7 Receiver Data Jitter Tolerance (OPEN) A conformant PMD implementation must be capable of providing to the PLCP the following bit width restrictions as applied to a single logical "one" or logical "zero" data bit that meets the maximum run length and dc balance as specified in sections 4.9.x and 4.9.y. The jitter associated with each individual data bi, as referenced from the center of a nominal dat bit period of 1.0 microsecond is outlined in Figure 4.6.



where t0 is the nominal center of a logical data bit

FIGURE 4.6: Data Jitter Tolerance

4.9.8 Preamble Definition

4.9.8.1 Ramp Up Period (CLOSED per A19) The purpose of a conformant PMD Ramp Up Time Period is to control the rate of change of the amplitude of the transmit signal durign its transition to the desired steady state transmit output level. The ramp-up period is defined as a window consisting of 8-bit periods and is governed by the mask of Figure 4.7.

The following states are defined by the mask of diagram Figure 4.7. The transmitter is considered "off" (i.e. less than -50 dBm EIRP) at the start of the first bit period and is less than 0 dBm at the end of the first bit period. The output level at the end of the seventh bit period is within 3 dB of the desired steady state transmit power level and within 1 dB at the end of the eighth bit period. The maximum magnitude of the rate of change of the output power level should be one volt per microsecond as measured by a wideband detector based on the RMS output voltage into a 50-ohm load of the conformant PMD.

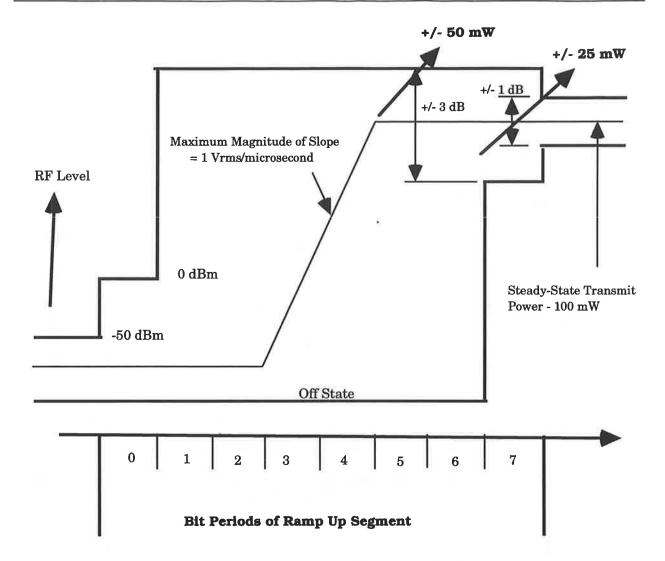


Figure 4.7: Ramp-Up

4.9.8.2 Ramp Down (CLOSED per A19) The purpose of a conformant PMD Ramp Down Time Period is to control the rate of change of the amplitude of the transmit signal durign its transition to the desired steady state transmit output level. The ramp-down period is defined as a window consisting of 8-bit periods and is governed by the mask of Figure 4.8.

The following states are defined by the mask of Figure 4.8. The transmitter is considered "off" (i.e. less than -50 dBm EIRP) at the start of the first bit period and is less than 0 dBm at the end of the first bit period. The output level at the end of the seventh bit period is within 3 dB of the desired steady state transmit power level and within 1 dB at the end of the eighth bit period. The maximum magnitude of the rate of change of the output power level should be one volt per microsecond as measured by a wideband detector based on the RMS output voltage into a 50-ohm load of the conformant PMD.

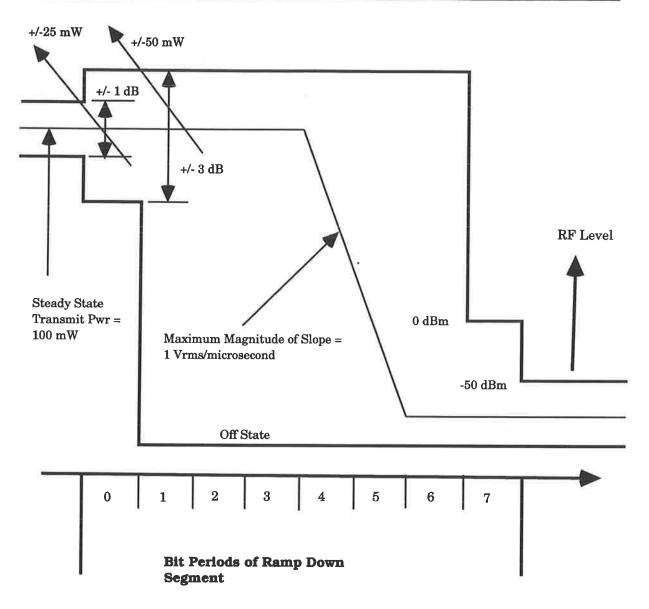


Figure 4.8: Ramp-Down

4.9.9 Received Data DC Offset (OPEN)

4.9.10 Received Data Maximum Run Length (DC Balance) (OPEN)

MOTION: Replace section 4.x (FHSS PMD Sublayer) of the FH PHY working draft standard 94/068 with the contents in this submission.