IEEE 802.11
Wireless Access Method and Physical Specification

Title: **FH PHY Bias Suppression Encoding Block Size**

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Summary

The Bias Suppression Encoding (BSE) discussed in submissions 94/69, 94/104, and 94/129 was adopted by the FH PHY ad hoc group to constrain data DC offset prior to modulation. The block sizes (unencoded/encoded) that have been proposed to date range from 8/9 to 64/65 bits with 16/17 and 32/33 as the primary candidates. Smaller block sizes results in less degradation while larger block sizes result in lower overhead on the raw data rate. The question that must be answered to select the block size for the 802.11 FH standard is: how much degradation?

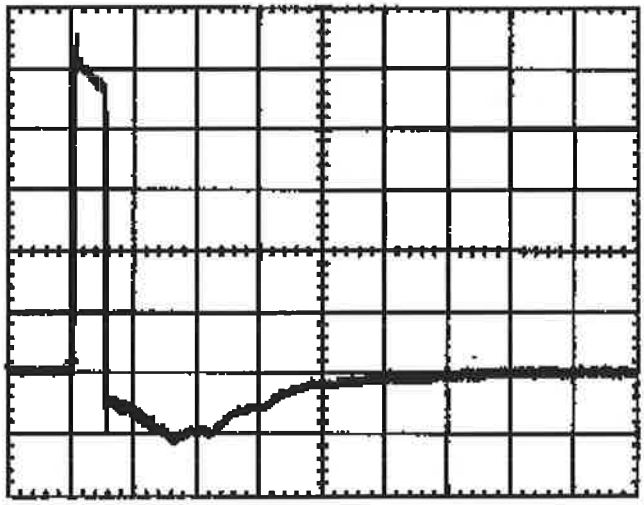
Degradation in this case must be analyzed in two parts: a statistical measure in the form of Eb/No degradation to achieve 10^{-5} BER, and a worst case degradation for degenerate data patterns. Hardware measurements and analysis were performed to estimate the degradation for 16/17 and 32/33 block sizes. The results indicate that for 1 KHz modulation loop bandwidths, either 16/17 or 32/33 would provide adequate performance and reasonable overhead.

To provide design flexibility for using faster modulation loops and higher data rates, the 16/17 BSE block size would be preferable. Faster loops would improve battery conservation but would result in higher signal distortion due to data bias. The 4GFSK modulation selected for the 2 Mbps option is much more sensitive to signal distortions. Both of these options would benefit from a smaller block size.

Worst Case Performance Degradation

We will look at the worst case first. Figures 1 and 2 show hardware measurement plots of the closed loop response to a block of biased (single valued) data followed by a tri-state condition. This would be representative of a string of ones or zeros followed by an unbiased 0101... pattern. The loop bandwidth is approximately 1 KHz. The curves are consistent with the simulation plots shown in 94/69.

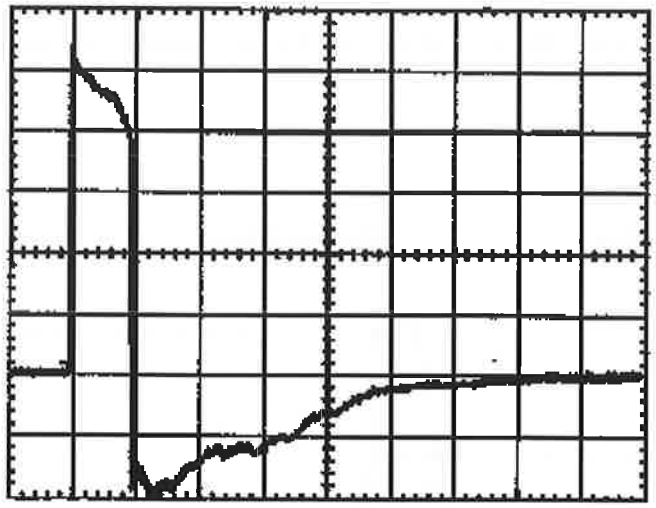
Figure 1 shows a string of 25 ones which is the worst case possible for 16/17 BSE block size. The dip following the block is approximately 20% of full voltage, producing a 1.9 dB signal reduction of any following ones. Thus, with the worst case pattern, the bias tracking effects will reduce the effective Eb/No by 1.9 dB for a portion of the data sequence.



50 μs/div

Figure 1. Hardware measurements of closed loop response to 25 ones

Figure 2 shows a string of 49 ones which is the worst case for 32/33 BSE block size. In this case, the dip is approximately 40% of full voltage which produces a 4.4 dB reduction in effective Eb/No for a portion of the data sequence.



50 μs/div

Figure 2. Hardware measurements of closed loop response to 49 ones

You could extrapolate these results to show the worst case for 64/65 BSE block size would produce effective reduction in Eb/No in excess of 12 dB. Although the probability of occurrence is very low, the number of times which the packet must be re-transmitted would be excessive. Also, the deterministic method in which the packet is scrambled and bias suppression encoded means that the degenerate pattern will remain until it is successfully transferred or is aborted.

Statistical Performance Degradation

We will now evaluate the statistical performance degradation of the bias. Figure 3 shows the probability density functions and standard deviation of the data bias in bits for various BSE block sizes. These statistics were generated from simulations of 1000 packets with length of 1500 bytes using the BSE formatting. The bias after each bit transmitted was accumulated into these statistics.

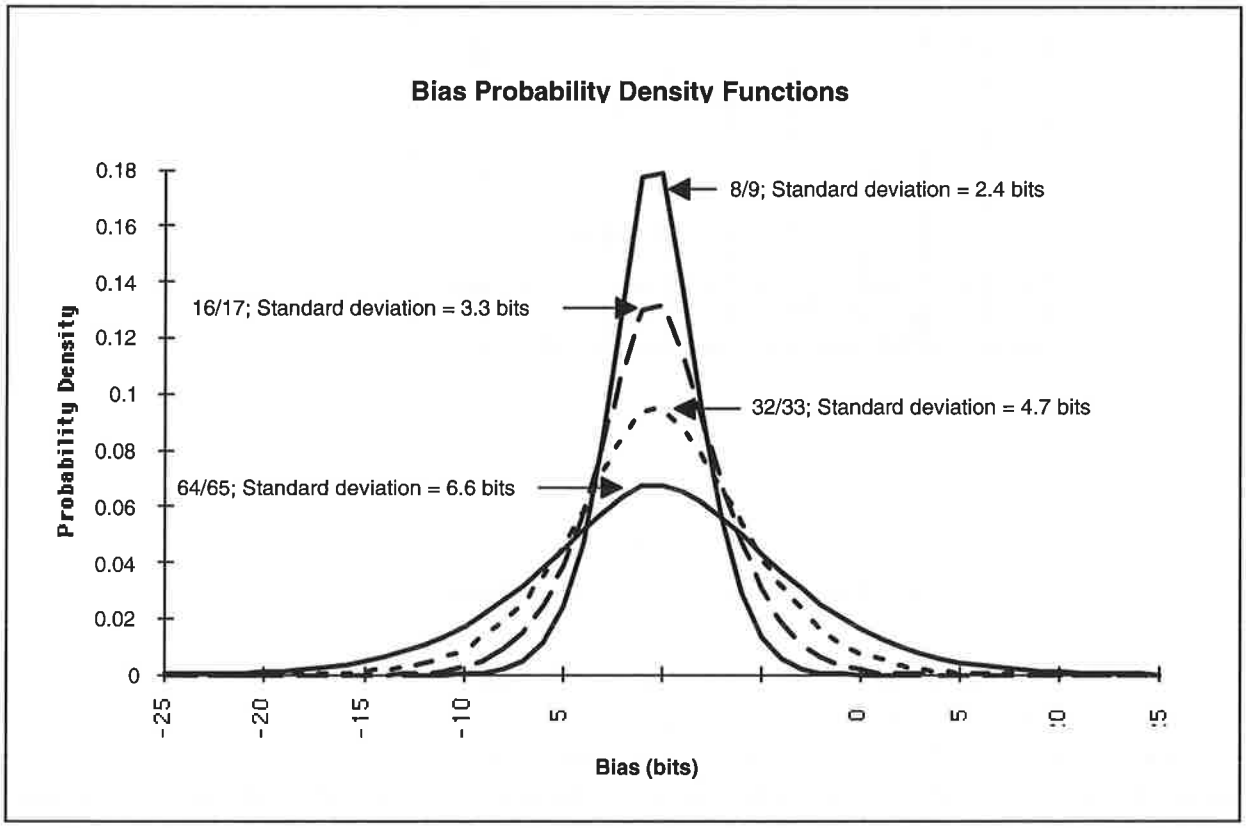


Figure 3. PDFs and standard deviations of bias for various BSE block sizes

Using Figures 1 and 2 to approximate a linear relationship between data bias in bits to signal distortion, we have an approximate signal distortion translation factor of 0.8%/bit of bias. The standard deviation translated to signal distortion is

16/17: $\sigma_{16/17} = 0.8\% * 3.3 = 2.6\ \%$

32/33: $\sigma_{32/33} = 0.8\% * 4.7 = 3.8\ \%$

Although the bias distributions are not exactly Gaussian, we can get a rough estimate of the degradation to Eb/No by RSS'ing the standard deviations of the noise and bias signal distortion. This estimate will be slightly pessimistic because it doesn't take into account the improved performance of opposite valued bits, e.g. zeros in our examples above. The standard deviation of Gaussian noise at 10^{-5} BER is about 23%. The RSS total of noise and bias distortion is

16/17: $\sigma_{noise+16/17} = (0.026^2 + 0.23^2)^{1/2} = 23.15\%$

32/33: $\sigma_{noise+32/33} = (0.038^2 + 0.23^2)^{1/2} = 23.3\%$

which corresponds to 0.06 and 0.11 dB degradation, respectively. Thus, statistically, either 16/17 or 32/33 will provide adequate performance.

Other Considerations

These performance numbers were measured and analyzed using a typical modulation loop bandwidth of 1 KHz. If the design utilized a higher bandwidth to conserve battery power by minimizing settling time on power up, the signal distortions would increase by a proportional amount.

The 4GFSK modulation selected for the 2 Mbps option of the 802.11 FH PHY is much more sensitive to signal distortions such as bias. The BSE algorithm can be applied independently to the MSB and LSB bit streams of the modulator (assuming Gray code encoding). The overall bias will be 1.33 times the bias of just the MSB stream alone. In addition, the thresholds are one third the distance of the maximum amplitude symbol. Thus, it will require either much slower modulation loop bandwidth or more expensive DC coupled modulators. Smaller BSE block sizes could significantly improve the high data rate performance in both the modulator and demodulator. Different block size could be used for 1 and 2 Mbps data rate, but it would increase the complexity of the hardware and the duration calculation in the MAC.