Direct Sequence Spread Spectrum
Physical Layer Specification
IEEE 802.11

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What is DSSS?

- Signal symbol is spreaded with a sequence

- Wider Bandwidth
- Less power density
11 chip BARKER sequence

- Good autocorrelation properties
- Minimal sequence allowed by FCC
- Coding gain 10.4 dB

DSSS benefits

- 10 dB coding gain:
  - Robust against interferers and noise (10 dB suppression)
- Robust against time delay spread
  - Resolution of echoes
IEEE 802.11 DSSS PHY characteristics

- 2.4 GHz ISM band (FCC 15.247)
- 1 and 2 Mb/s datarate (DBPSK and DQPSK modulation)
- Symbol rate 1 MHz
- Chipping rate 11 MHz with 11 chip Barker sequence
- Multiple channels in 2.4 to 2.4835 GHz band

PLCP Frame Format

Preamble and Header always at 1Mb/s DBPSK
PLCP synchronization

- 128 scrambled 1 bits
- needed for o.a.
  - gain setting
  - energy detection
  - antenna selection
  - frequency offset compensation

Start Frame Delimiter

- 16 bit field (hF3A0)
- used for
  - bit synchronization
**Signal Field**

- Rate indication
  - h0A 1Mb/s DBPSK
  - h14 2Mb/s DQPSK
- Other values reserved for future use (100 kb/s quantities)

**Service Field**

- Reserved for future use
- h00 signifies 802.11 compliant
Length Field

- Indicates number of octets to be transmitted in MPDU
- Used for
  - End of frame detection
  - MPDU CRC sync

CRC field

- CCITT CRC-16
- Protects Signal, Service and Length Field
Data Scrambler

Scrambler Polynomial: \( G(z) = z^4 + z^3 - 4z + 1 \)

- ALL bits transmitted by the DSSS Phy are scrambled
- Purpose
   - Whitening the spectrum
   - DC blocking (Barker sequence is asymmetric)

DBPSK Modulation

<table>
<thead>
<tr>
<th>Bit Input</th>
<th>Phase Change (( \pm \pi/2 ))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>( \pi )</td>
</tr>
</tbody>
</table>

Table 1, 1 Mb/s DBPSK Encoding Table.
DQPSK Modulation

<table>
<thead>
<tr>
<th>Dibit pattern (d0,d1)</th>
<th>Phase Change ($\pm \phi$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>0</td>
</tr>
<tr>
<td>01</td>
<td>$\pm \pi$</td>
</tr>
<tr>
<td>11</td>
<td>$\pm 3\pi/2$ ($\mp 3\pi/2$)</td>
</tr>
<tr>
<td>10</td>
<td>$\pm \pi/2$ ($\mp \pi/2$)</td>
</tr>
</tbody>
</table>

Table 1, 2 Mb/s DQPSK Encoding Table

Transmit Spectrum Mask

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### DSSS Channels

<table>
<thead>
<tr>
<th>CHNL_ID</th>
<th>FCC Channel Frequencies</th>
<th>ETSI Channel Frequencies</th>
<th>Japan Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2412 MHz</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>2417 MHz</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>3</td>
<td>2422 MHz</td>
<td>2422 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>2427 MHz</td>
<td>2427 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>5</td>
<td>2432 MHz</td>
<td>2432 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>6</td>
<td>2437 MHz</td>
<td>2437 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>7</td>
<td>2442 MHz</td>
<td>2442 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>8</td>
<td>2447 MHz</td>
<td>2447 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>9</td>
<td>2452 MHz</td>
<td>2452 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>10</td>
<td>2457 MHz</td>
<td>2457 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>11</td>
<td>2462 MHz</td>
<td>2462 MHz</td>
<td>N/A</td>
</tr>
<tr>
<td>12</td>
<td>N/A</td>
<td>N/A</td>
<td>2484 MHz</td>
</tr>
</tbody>
</table>

Table 1, DSSS PHY Frequency Channel Plan

### Clear Channel Assessment

- **Three methods:**
  - CCA mode 1: Energy above threshold
  - CCA mode 2: Carrier sense only
  - CCA mode 3: Carrier sense with energy above threshold
- **Energy detection function of TX power**
  - Tx power > 100 mW: -80 dBm
  - Tx power > 50mW : -76 dBm
  - Tx power <= 50mW: -70 dBm
- **Energy detect time**: 15 µs
- Correct PLCP header --> CCA busy for full (intended) duration of frame as indicated by PLCP Length field
DSSS Specification Summary

- Slottime: 20 μs
- TX to Rx turnaround time: 10 μs
- Rx to Tx turnaround time: 5 μs
- Operating temperature range:
  - type 1: 0 - 40 °C
  - type 2: -30 - 70 °C
- Tx Power Levels:
  - 1000 mW USA
  - 100 mW Europe
  - 10 mW/MHz Japan
- Minimum Transmitted Power: 1 mW
- Tx power level control: required above 100 mW

DSSS Specification Summary (cont)

- Tx Center Frequency Tolerance: +/- 25 ppm
- Chip Clock Frequency Tolerance: +/- 25 ppm
- Tx Power On Ramp: 2 μs
- Tx Power Down Ramp: 2 μs
- RF Carrier suppression: 15 dB
- Transmit modulation accuracy: test procedure
- Rx sensitivity: -80 dB @ 0.08FER (1024 Bytes)
- Rx max input level: -4 dB
- Rx adjacent channel rejection: >35 dB @ > 30 MHz separation

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PLCP Transmit Procedure

PLCP Receive Procedure