NTT Wireless Systems Laboratories

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Background

To realize high data rate (≥ 20Mbit/s) wireless LAN modem...

Higher symbol rate \( \rightarrow \) larger degradation by multipath delay

Multipath countermeasure

- Equalizer
  - Large circuit scale
  - (trade-off with performance)
  - \( \times \)
- Sector antenna
  - Large antenna size
  - \( \times \)
- OFDM modulation
  - Hardware size?
  - Power Consumption?
Number of butterfly operations

<table>
<thead>
<tr>
<th>FFT points</th>
<th>radix - 2</th>
<th>radix - 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>r</td>
<td>m</td>
</tr>
<tr>
<td>8</td>
<td>3</td>
<td>12</td>
</tr>
<tr>
<td>16</td>
<td>4</td>
<td>32</td>
</tr>
<tr>
<td>32</td>
<td>5</td>
<td>80</td>
</tr>
<tr>
<td>64</td>
<td>6</td>
<td>192</td>
</tr>
<tr>
<td>128</td>
<td>7</td>
<td>448</td>
</tr>
<tr>
<td>256</td>
<td>8</td>
<td>1024</td>
</tr>
</tbody>
</table>

radix - 2
m = \frac{N \log_2 N}{2}

radix - 4
m = \frac{N \log_4 N}{4}

Basic (parallel) type FFT circuit

FFT circuit structure

Hardware size
Loop type < Pipeline type < parallel type

Power Consumption
Loop type ? Pipeline type

Basic (parallel) type FFT circuit

Loop type FFT circuit
<table>
<thead>
<tr>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data rate</strong></td>
</tr>
<tr>
<td><strong>Modulation scheme</strong></td>
</tr>
<tr>
<td><strong>FFT point</strong></td>
</tr>
<tr>
<td><strong>Technology</strong></td>
</tr>
</tbody>
</table>

**Pipelined FFT circuit (radix-4)**

```
input formatter

butterfly circuit

k = \frac{N}{4^r+1}

matrix switch

output formatter
```
### Hardware size and power consumption of pipelined FFT circuits

**3 quantization bits : 12 bit**

<table>
<thead>
<tr>
<th>Circuit Block</th>
<th>Power Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 butterfly circuit</td>
<td>90.7 kG (58.6%)</td>
</tr>
<tr>
<td>1 butterfly circuit</td>
<td>30.2 kG</td>
</tr>
<tr>
<td>delay line (D)</td>
<td>28.2 kG (16.9%)</td>
</tr>
<tr>
<td>coefficient ROM</td>
<td>3.5 kG (2.3%)</td>
</tr>
<tr>
<td>matrix switch</td>
<td>1.8 kG (1.2%)</td>
</tr>
<tr>
<td>bit arrangement</td>
<td>18 kG (11.6%)</td>
</tr>
<tr>
<td></td>
<td><strong>88.6 mW (100%)</strong></td>
</tr>
</tbody>
</table>

**Power Consumption**

- **Adder(108G)*30 + Multiplier(2250G)*12**
  - 30.2 kG

**FFT clock frequency = 6.25 MHz (radix-2 type)**

### Hardware size and power consumption of pipelined FFT circuits

![Graph showing number of gates and power consumption vs. FFT point number](image)

**Number of gate**
- 16bit
- 12bit
- 8bit

**Power Consumption (mW)**
- 16bit
- 12bit
- 8bit

**Number of FFT point N**
- 16
Parameter for gate number
Number of FFT point: 64
Number of bit: 12
Total gate size: 84kG

Hardware size and power consumption of loop-type FFT circuits
Conclusion

- 64 point FFT for 25Mbit/s QPSK-OFDM modulation
  (radix-4 type, 12 bits operation)
  - Pipelined FFT circuits: 155 kG, 89 mW
  - Loop-type FFT circuits: 84 kG, 75 mW

Items to be considered

- Frequency error sensitivity (AFC)
- Clock recovery
- Preamble length
- Guard interval (multipath delay)