

IEEE P802.11 Wireless LANs

QPSK Modulation With Anti-multipath Scheme for High Speed Wireless LAN

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Status of the Presentation

A skeleton proposal for
QPSK modulation with an anti-multipath scheme

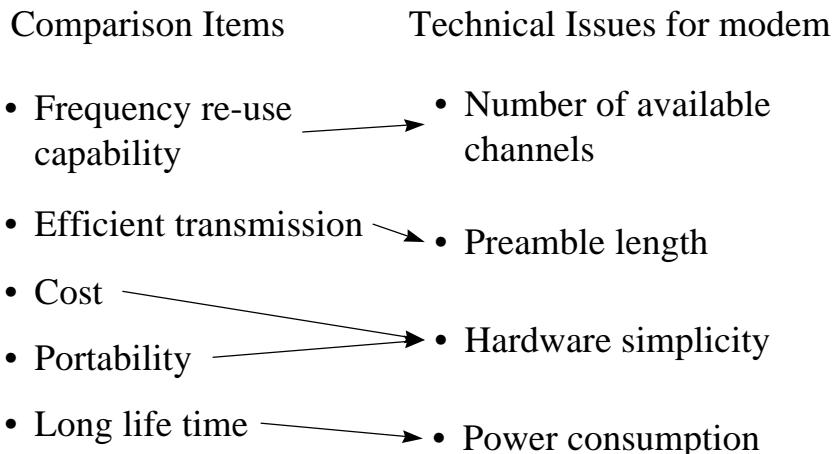


- A candidate of single carrier systems
- Possibilities to change the proposed scheme through future studies

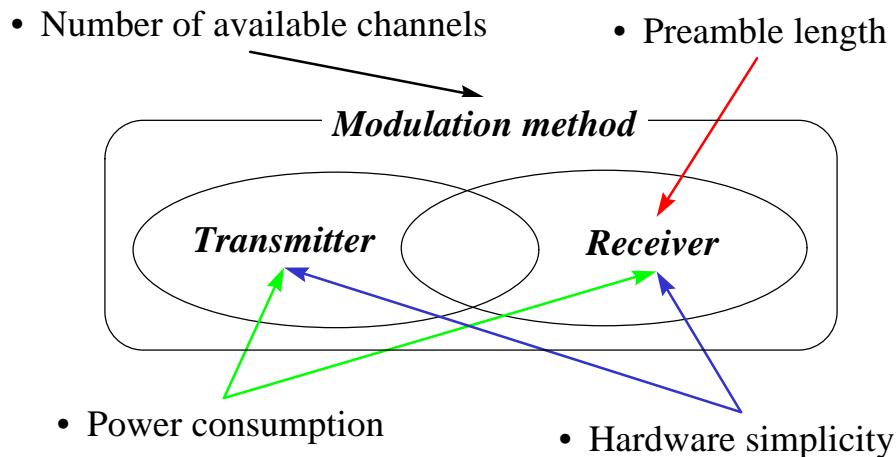
Requirements for High Speed Wireless LAN

- Requirements from System side: **Large system capacity**
 - Additional comparison items
 - Frequency re-use capability
 - Efficient transmission
- Requirements from Equipment side: **Usability for users**
 - Additional comparison items
 - Cost
 - Portability
 - Long life time

Technical issues for the comparison items



Impacts of the issues on modems



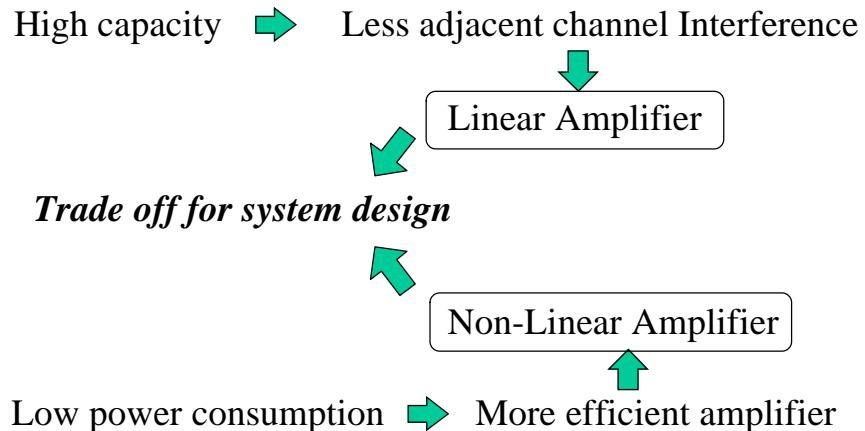
Considerations on Transmitter

Modulation method: QPSK

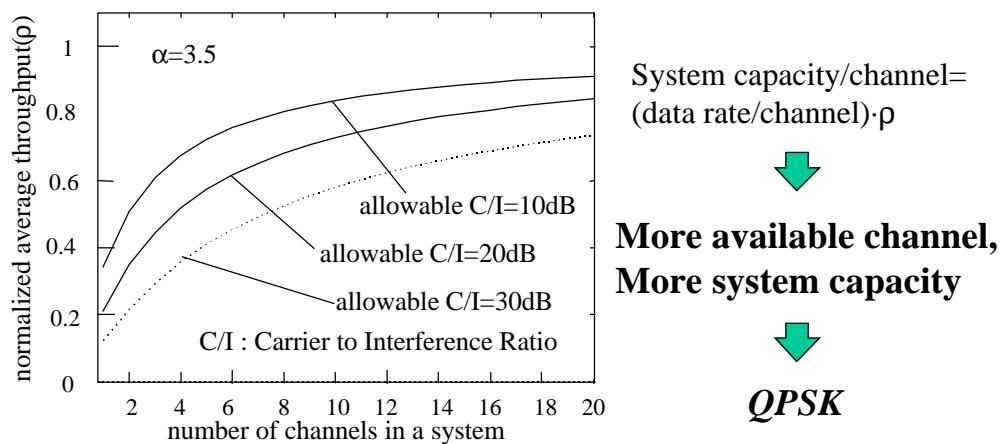


	Power Consumption	H/W Simplicity
baseband	Low (mature digital technology)	Simple
RF/IF	To be solved <i>(linear high power amplifier)</i>	To be solved

Amplifier in Transmitter



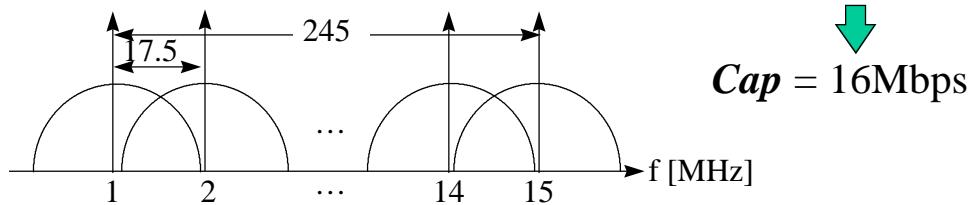
Consideration on modulation method



Estimation of System capacity/channel(*Cap*)

- Modulation: QPSK (roll-off=50%)
- Data rate: 20Mbps/channel(12.5Msymbol/sec)
- Carrier interval: $12.5[\text{MHz}] \cdot 1.4 = 17.5 [\text{MHz}]$
- System bandwidth: 300MHz

15 carriers + • Allowable C/I: 20dB $\rightarrow \rho=0.8$



Consideration on Receiver

	Power Consumption	H/W Simplicity	Preamble
baseband	Pending issue	Pending issue	Pending issue <i>(Anti-multipath scheme)</i>
RF/IF	Low	Simple	Short (conventional technologies can be applied)



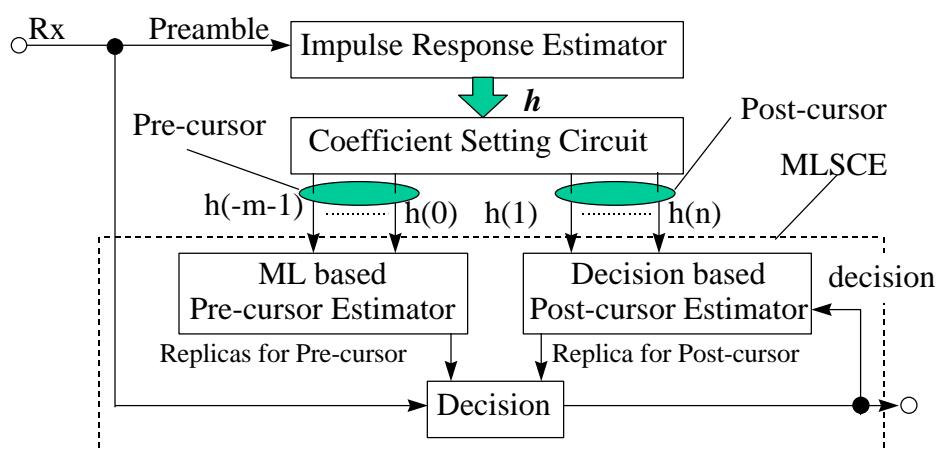
Innovative anti-multipath scheme must be proposed

Anti-multipath Scheme

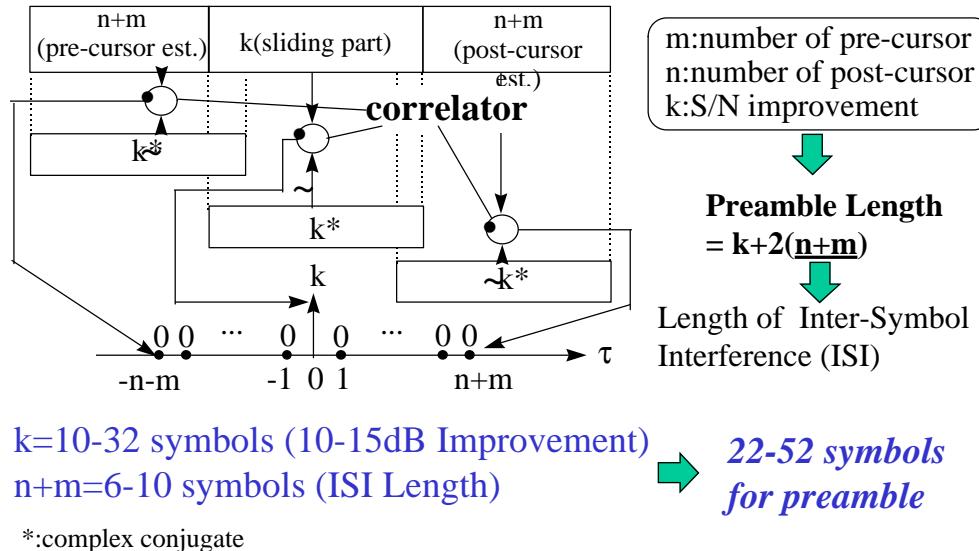
Tap Coefficient Shift MLSCE (Maximum Likelihood Symbol Candidate Estimator)

- Symbol-by-symbol base ML estimator
 - Effective usage of decision feedback loop
 - Reduction of likelihood calculation
 - Avoidance of weak point of ML estimator
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Tap Coefficient Shift MLSCE



Preamble for Tap Coefficient Shift MLSCE



Comparison of Calculation Amount

	MLSCE	DDFSE	DFE
multiplier (complex)	0	0	m
adder	$n+m \cdot L^m$ *	$n+m \cdot L^m$ *	$n+m$
Viterbi	None	Required	None

* $m \cdot L^m$: one time per packet

m: tap number of Pre-cursor Estimator

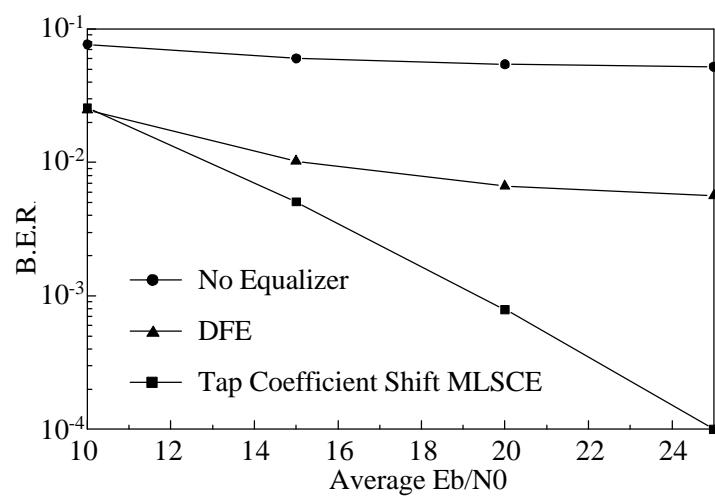
n: tap number of Post-cursor Estimator

L: phase number of Modulation

Simulation Conditions

Modulation Method	QPSK(Roll off=50%)
Symbol Rate	12.5Msymbol/s
Propagation Model	2-path Rayleigh model (1symbol delay)
tap	Pre-cursor Estimator : 2tap Post-cursor Estimator : 3tap

Simulation Results



Conclusions

QPSK + Tap Coefficient Shift MLSCE

Skeleton Proposal for single carrier system

- Large capacity: 16Mbps/channel for 300MHz bandwidth
- Transmitter: trade off for system design
- Short preamble: about 20-50 symbols for MLSCE
- Simplicity: neither Viterbi process nor complex multiplier