IEEE P802.11
Wireless LANs

Optimized Bit Order within the Interleaver

Date: February 18, 1999

Author: Tal Kaitz and Naftali Chayat
BreezeCom
Atidim Technology Park, Bldg. 1, Tel-Aviv 61131, Israel
Phone: +972-3-645-6262
Fax: +972-3-645-6290
e-mail : [talk naftalic]@breezecom.co.il

Abstract

In this submission, a modification to the interleaver structure is presented. The modification involves permuting the order of bits within the interleaver. This modification prevents the occurrence of runs of consecutive low reliability least significant bits (LSBs). This submission is a response to a comment issued by Dean Kawaguchi, during the balloting process of the 802.11a.

1 Introduction

In the January 802.11 interim meeting, a comment was made by Dean Kawaguchi, regarding the bit ordering of least and most significant bits within the interleaver/deinterleaver. During the meeting, Dean's proposed change was evaluated by Breezecom. It was revealed that there is only a minor potential for improvement.

However, a more thorough simulation effort, which included QAM64 modulation and the new scheme of un punctured pilots, revealed that the potential for improvement is considerable.

2 Problem statement

Because of the Gray coding used in the symbol mapping, the bits related to one symbol cannot be decoded with equal reliability. To demonstrate, let us consider the case of QAM16 modulation and discuss the 2 bits related to one coordinate (e.g. In-phase or Quadrature). The bit assignment is shown in table 1, where for simplicity the factor of square √10 was omitted.

Input bits b_1 b_2	I or Q out
00	-3
01	-1
11	1
10	3

Let us consider the probability of a bit error, denoted by $P_e(b_n)$. Let us assume hard decoding and equally likely bits. Let x denote the transmitted symbol and Pe denote the probability of a decoding error. We shall assume that a decoding error could lead to a neighbouring symbol only. In this case

$$P_e(b1)= 1/2*P_e* (Pr(x=-1) + Pr(x=1)) = 1/4 P_e.$$

$$P_e(b2)= 1/2*P_e* (Pr(x=-3) + Pr(x=1)+ Pr(x=1) + Pr(x=3)) = 1/2 P_e.$$

Hence $P_e(b2)=2*P_e(b1)$.

For QAM64 modulation and grey coding the bit error probabilities are given by:

$$P_e(b1)= 1/8 P_e.$$

$P_e(b2)= 1/4\ P_e.$

$P_e(b3)= 1/2\ P_e.$

Hence $P_e(b3)=2*P_e(b2)=4*P_e(b1)$.

The conclusion from both examples is that the more significant bits are more reliable than the least significant bits.

Let us now consider the operation of the deinterleaver. Let d denote the size of the interleaver. The deinterleaver is arranged as matrix of d/16 row by 16 columns. Writing into the deinterleaver is performed column-wise and reading from the deinterleaver is performed row-wise.
Let $b_n(I_k)$ and $b_n(Q_k)$ denote the n^{th} bit from the I or Q components of the k^{th} subcarrier, respectively. For QAM16 the deinterleaver contents are shown in figure 1.

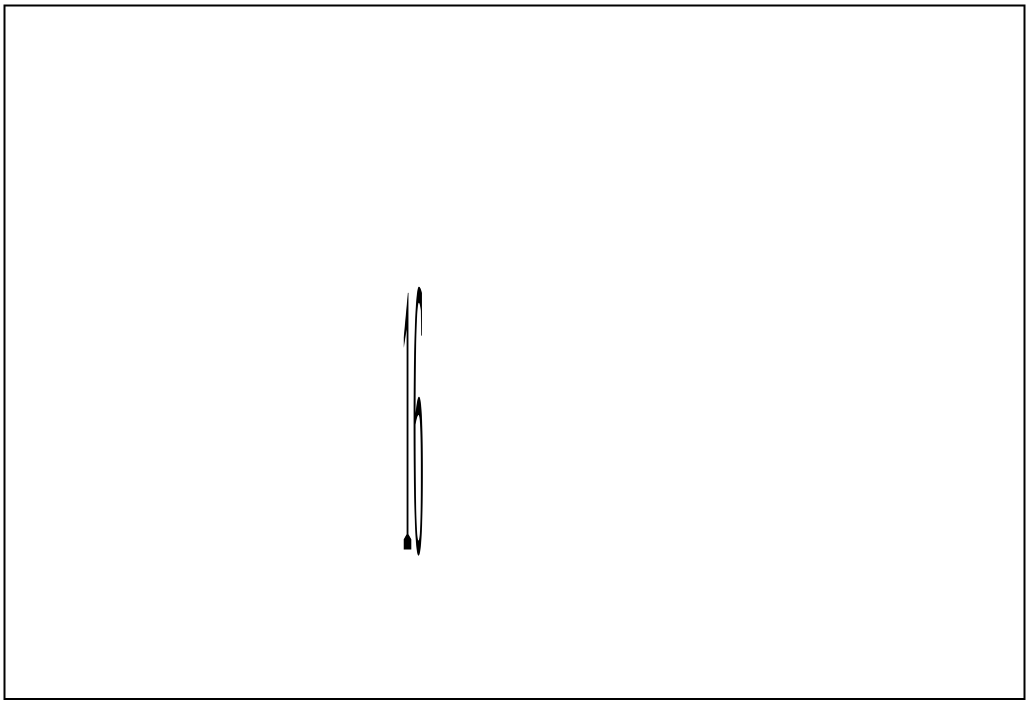

Figure 1 Current deinterleaver for QAM16

As can be seen, the bit stream leaving the deinterleaver, is composed of 16 consecutive high-reliability MSBs followed by 16 consecutive low-reliability LSBs. This may weaken the error correction capabilities of the convolutional code.

3 Proposed solution

The proposed solution is to cyclically permute all the bits that relate to the same coordinate. The contents of the deinterleaver for QAM16, under the proposed permutation is shown in figure 2.

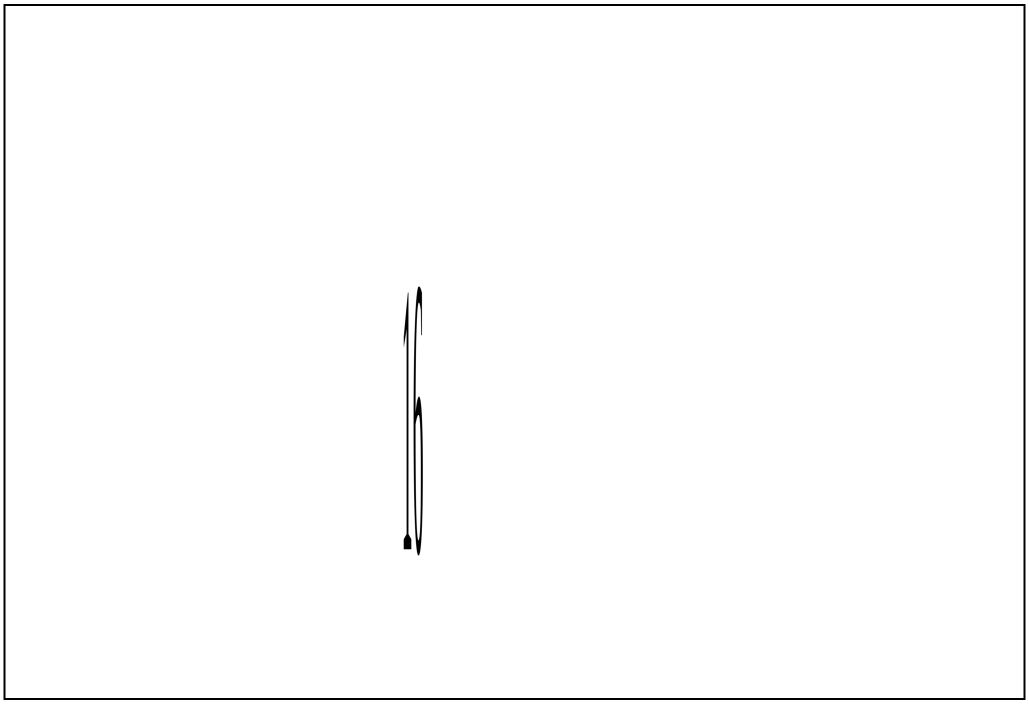

Figure 2- Modified deinterleaver for QAM16

For the QAM64 the contents of the deinterleaver are shown in figure 3.

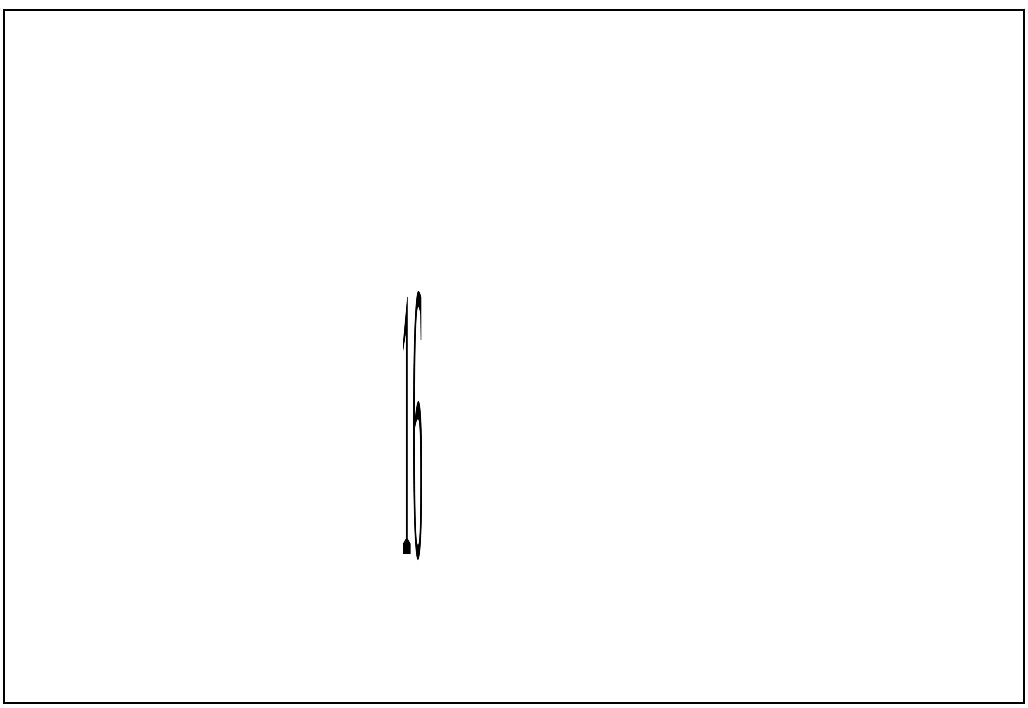

Figure 3 Modified deinterleaver for QAM64

4

Simulation results

To demonstrate the improvement of the proposed scheme, a set of simulation experiments was conducted. The results are shown below.

4.1 Performance in AWGN

4.1.1 QAM16 modulation

The results for QAM16 modulation (rate 24Mb/s and 36Mb/s) are shown in figure 4.

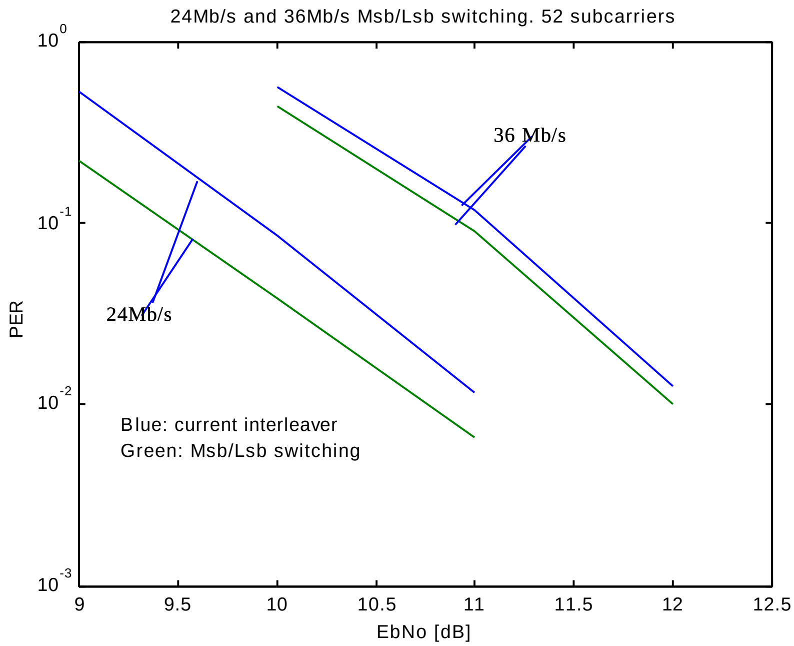

Figure 4

An improvement of about 0.5dB is evident for 24Mb/s mode.

4.1.2 QAM64 modulation

The results for QAM64 modulation (rate 48Mb/s and 54Mb/s) are shown in figure 5 and 6.

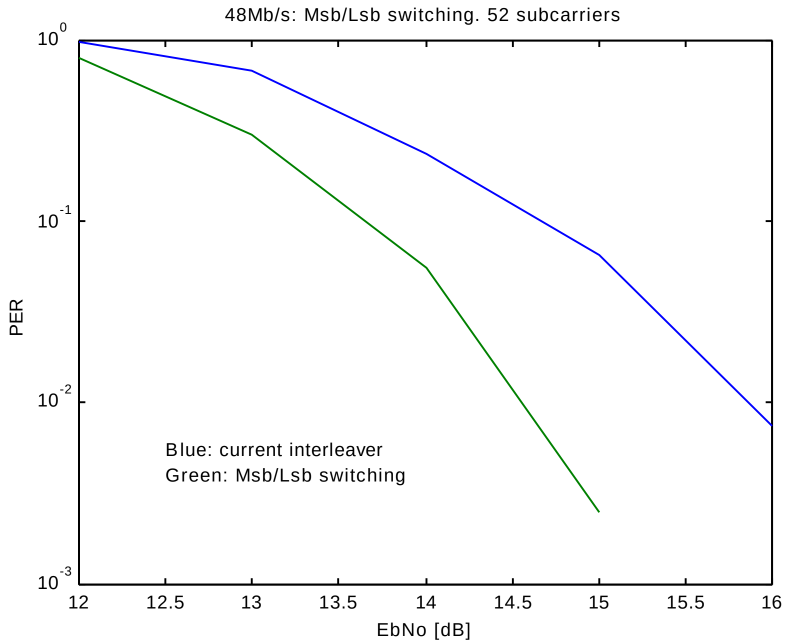

Figure 5 –48Mb/s

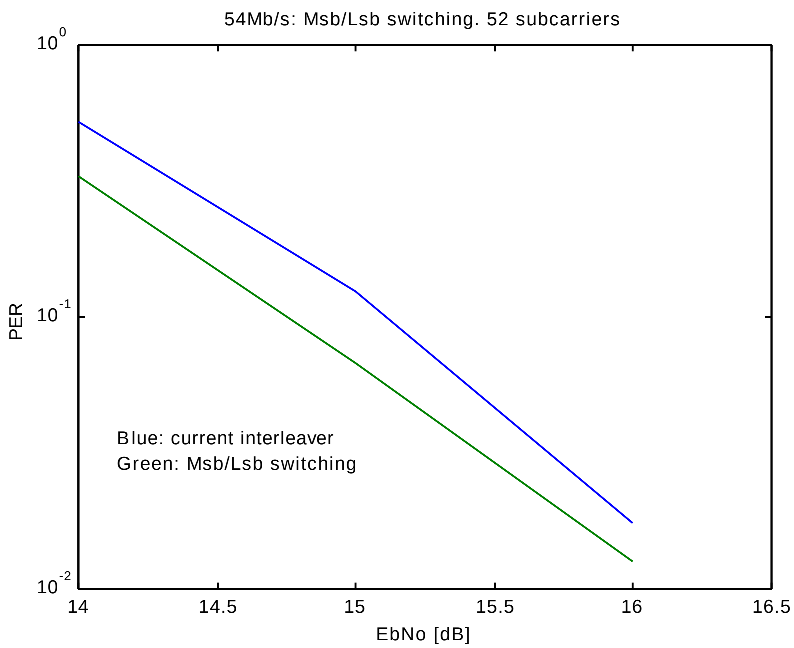

Figure 6 - 54 Mb/s modulation

An improvement of about 1dB is evident for 48Mb/s.

4.2 Performance in Multipath

4.2.1 QAM16 modulation

The results for 24Mb/s are shown in figure 7 and for 36 Mb/s in figure 8.

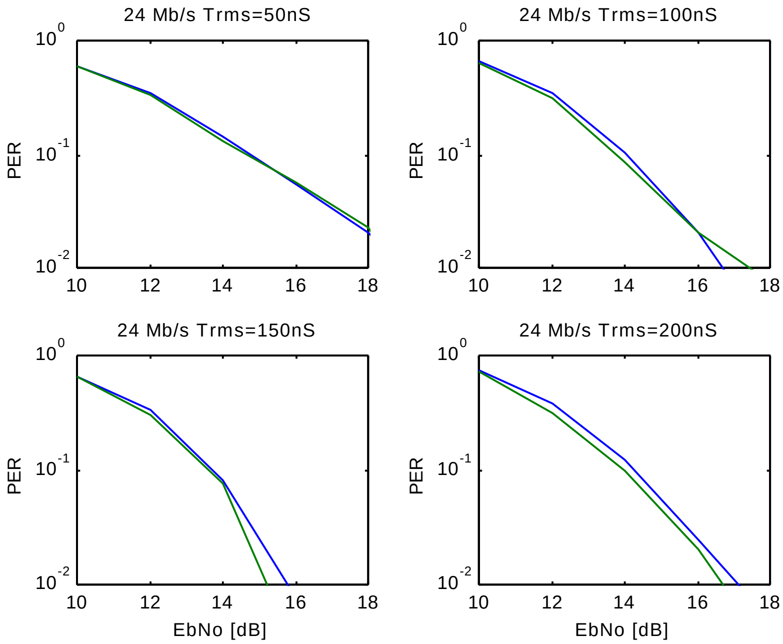

Figure 7 - Results for 24Mb/s

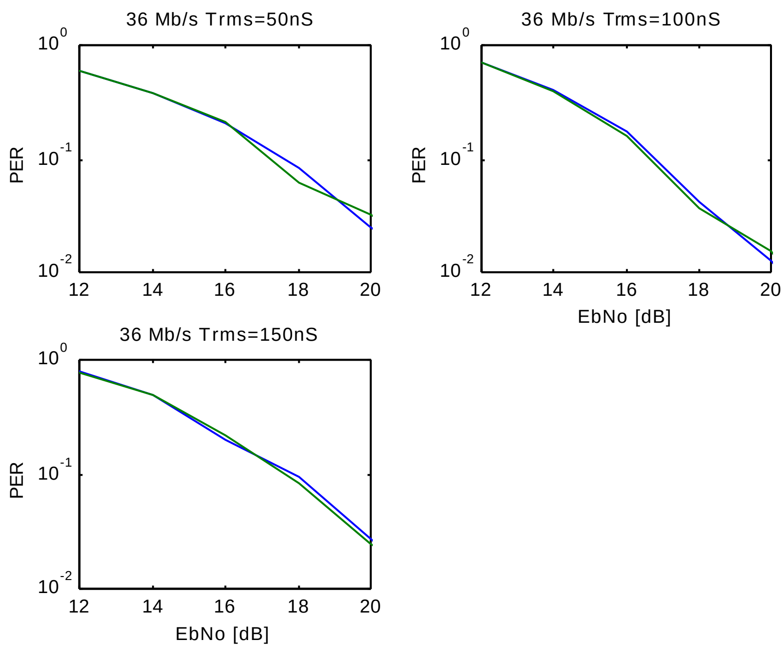

Figure 8 – Results for 36Mb/s

A slight improvement is evident.

4.2.2 QAM64 modulation

The results for 48Mb/s are shown in figure 9 and for 54Mb/s in figure 10.

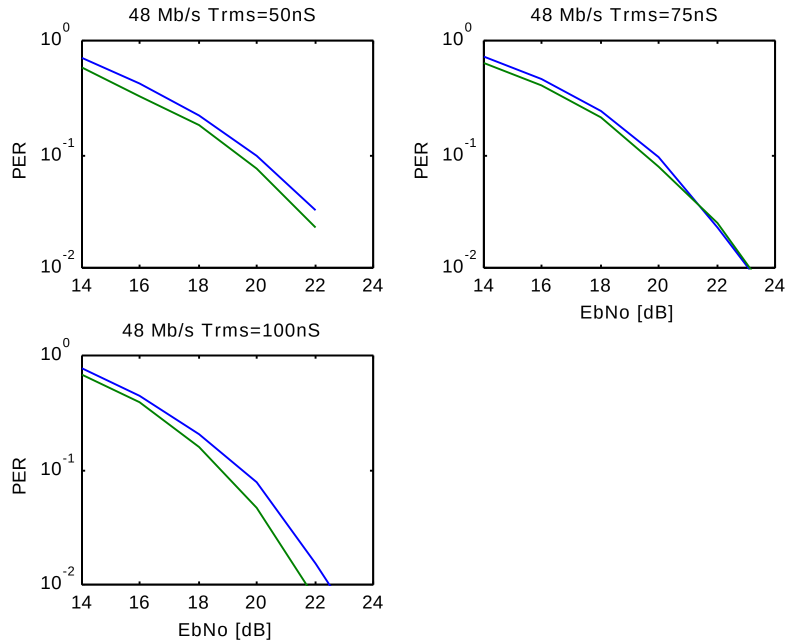

Figure 9- Results for 48Mb/s

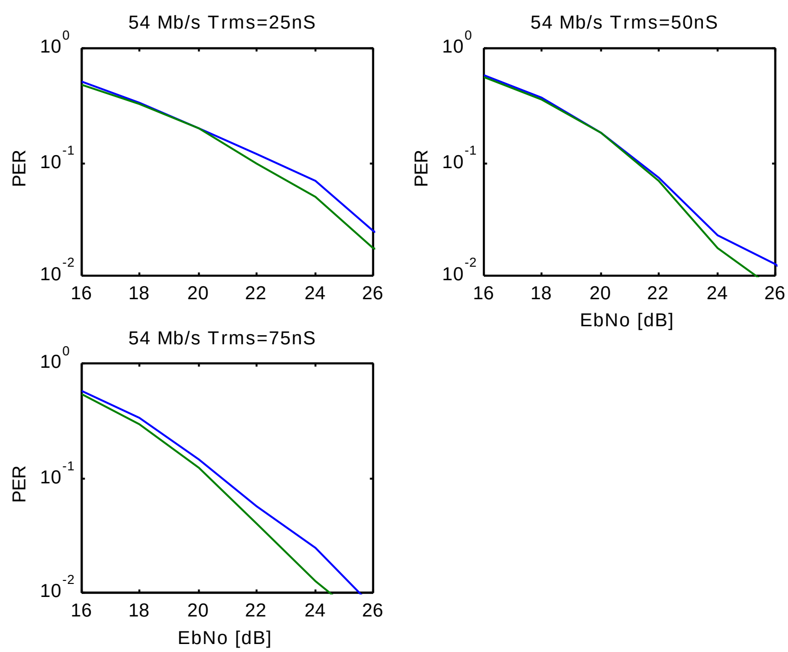

Figure 10 – Results for 54 Mb/s

An improvement of up to 1 dB for 48Mb/s is evident.

5 Formal Definition and Recommended Text Change

5.1 Preliminaries

We should note that the modification to the deinterleaver can be described as a permutation action performed prior to writing into the deinterleaver. The interleaver action, on the other hand can be described as a permutation action performed after the reading from the interleaver.

5.2 Interleaver definition:

1. Perform the interleaver defined by Eq (14)

2. Perform the permutation defined by

$j= s*floor(i/s)+ (i + N_{CBPS} - floor(16*i/N_{CPBS})\ )\ \mathbf{mod}\ s \quad i=0\ldots N_{CPBS}-1$

where : i location before permutation
j location after permutation
and :
s = max("coded bits per subcarrier/2",1)

5.3 Deinterleaver definition

1. Perform the permutation defined by:

$i= s*floor(j/s)+ (j+ floor(16*j/N_{CBPS})\ )\ \mathbf{mod}\ s \quad j=0\ldots N_{CPBS}-1$

where : j location before permutation
i location after permutation
s defined as in section 5.2

2. Perform the deinterleaver defined by equation (15)

6 Conclusions

It was shown that a simple permutation in the bit order can solve the problem of consecutive low-reliability LSBs. The proposed permutation is easy to implement, and yet it may lead to a performance improvement of up to 1 dB. The authors recommend to incorporate the proposed modification into the 802.11a standard's draft.