IEEE P802.11
Wireless LANs

Comment received on Letter Ballot 18 for 802.11a

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Tal's wording proposal is given at the end

Seq. #	Clause number	your voter's id code	Cmnt type E, e, T, t	Part of NO vote	Comment/Rationale	Recommended change	Disposition/Rebuttal
1	17.3.2.1	NC	e	N	**On page 12, line 25, replace "data bits per OFDM symbol" with N_{DBPS}.**		
2	17.3.2.4	NC	e	N	**On page 14, end of line 37, add "with" before Ck and apply an appropriate formatting to Ck**		

3	**17.3.5.7**	**NC**	**e**	**N**	**Use notation $b_0 - b_5$ coherently throughout the subclause, in text, tables and figures**		
4	**17.3.5.4**	**NC**	**e**	**N**	**On page 20, line 25, change "LSB first and MSB last" to "bit 0 first and bit 7 last".**		
5	**17.3.4.5**	**NC**	**e**	**N**	**Change bit numbers to reflect that the bits are numbered 0-23.**	Bit 16 shall be reserved for future use. Bit 17 shall be a positive parity (even parity) bit for bits 0-16. The bits 18-23 constitute SIGNAL TAIL field, and all 6 bits shall be set to zero.	
6	**17.3.11**	**NC**	**e**	**N**	**On page 37, line 24 change "LSB to MSB order" into "bit 0 to bit 7 order"**		
	17.3.5.7	**tk**	**E**		**The interleaver/de-interleaver change that was agreed upon in the March meeting, and that is described in doc 99:047r1, was not correctly incorporated into the text. In doc 47r1 the permutation was defined as a two step process whereas in drat 4.0 only one step is described.**	**See attached text change**	
1	**17.3.5.6**	**ko**	**E**		**Texts in the section 17.3.5.6 are not enough to define the interleaver described in doc 99/47r1.**	**See 1st item described in section 5.2 of doc. IEEE 802.11-99/47r1. It requires to do interleave defined by eq. (14) in D3.0 before the bit permutation defined by eq. (15) in D4.0.**	

Data interleaving

All encoded data bits shall be interleaved by a block interleaver with a block size corresponding to the number of bits in a single OFDM symbol, N_{CBPS}. The interleaver is defined by a two step permutation. The first insures that adjacent coded bits are mapped onto nonadjacent subcarriers. The second permutation insures that adjacent coded bits are mapped alternately onto less and more significant bits of the constellation, and by this long runs of low reliability (LSB) bits are avoided.

We shall denote by k the index of the coded bit before the first permutation, i shall be the index after the first and before the second permutation and j shall be the index after the second permutation, just prior to modulation mapping.

The first permutation, is defined by the rule:

$$i=(N_{CBPS}/16)\ (k \bmod 16)+\text{floor}(k/16) \qquad k=0,1,\ldots,N_{CBPS}-1 \quad \text{(eq1)}$$

The function floor(.) denotes the largest integer not exceeding the parameter.

The second permutation is defined by the rule:

$$j= s*\text{floor}(i/s)+ (i + N_{CBPS} - \text{floor}(16*i/N_{CBPS})\ ) \bmod s \quad i=0,1,\ldots\ N_{CPBS}-1 \quad \text{(eq2)}$$

The value of s is determined by the number of coded bits per subcarrier, N_{BPSC}, according to:

$$s = \max(N_{BPSC}/2,1). \quad \text{(eq3)}$$

The deinterleaver, which performs the inverse relation, is also defined by two permutations.

Here we shall denote by j the index of the original received bit before the first permutation, i shall be the index after the first and before the second permutation and k shall be the index after the second permutation, just prior to delivering the coded bits to the convolutional (Viterbi) decoder.

The first permutation is defined by the rule:

$$i= s*\text{floor}(j/s)+ (j+ \text{floor}(16*j/N_{CBPS})\ ) \bmod s \qquad j=0,1,\ldots\ N_{CPBS}-1 \quad \text{(eq4)}$$

where s is defined in equation (eq3). This permutation is the inverse of the permutation described in (eq2).

The second permutation is defined by the rule:

$$k=16*i-(N_{CBPS}-1)\text{floor}(16*i/N_{CBPS}) \qquad i=0,1,\ldots\ N_{CPBS}-1 \quad \text{(eq5)}$$

This permutation is the inverse of the permutation described in (eq1).