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**Source:** [Akifumi Kasamatsu, Toshiaki Matsui, Honggang Zhang, Iwao Nishiyama, Kenichi Takizawa, Ryuji Kohno ]

Company [ (1) Communications Research Laboratory (CRL), (2) CRL-UWB Consortium ]

Connector's Address [3-4, Hikarino-oka, Yokosuka, 239-0847, Japan]

Voice:[+81-468-47-5432], FAX: [+81-468-47-5431],

E-Mail: [kasa@crl.go.jp, matsui@crl.go.jp, honggang@crl.go.jp, nisiyama@crl.go.jp, takizawa@crl.go.jp, kohno@crl.go.jp]

**Re:** [IEEE P802.15 Alternative PHY Call For Proposals, IEEE P802.15-02/327r7]

**Abstract:** [In order to realize the global harmonization and compromise in IEEE 802.15.3a UWB WPAN, SSA-UWB systems are investigated in CRL & CRL-UWB Consortium and the latest implementation achievements are briefly summarized to show feasibility of SSA-UWB and other systems.]

**Purpose:** [For investigating the characteristics of High Rate Alternative PHY standard in 802.15TG3a, based on the Soft-Spectrum Adaptation (SSA) proposal by CRL and CRL-UWB Consortium.]

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# SSA-UWB Implementation: An Approach for Global Harmonization and Compromise in IEEE 802.15.3a WPAN

Akifumi KASAMATSU, Toshiaki MATSUI, Honggang ZHANG, Iwao NISHIYAMA Kenichi TAKIZAWA, Ryuji KOHNO <u>Communications Research Laboratory(CRL)</u> <u>& CRL-UWB Consortium</u>

# Outline of presentation

- 1. Q&A with respect to the requests from MB-OFDM side
- 2. Brief historical retrospect of SSA-UWB PHY proposal
- 3. Description of implementation realization of SSA-UWB transceiver
- 4. Global harmonization and compromise based on SSA-UWB systems
- 5. Conclusion remark

### 1. <u>Q&A with respect to the requests and</u> <u>concerns from MB-OFDM side</u>

Requests and concerns of MB-OFDM side

"World-wide Compliance - The MBOK proposal relies on implementing a Soft Spectral Adaptation (SSA) scheme to ensure compliance with potentially different world-wide regulations. However, the CRL presentation in January 2003 shows that the SSA scheme would require the implementation of at least a 4-bit, 71.1 GHz DAC, or even a 284.4 GHz DAC. We were unable to obtain information regarding the power consumption, complexity or implementation feasibility of such a high-speed DAC. To better understand the global compliance capability of the MBOK proposal we would like answers to the following questions."

### <u>Q 1.a: "Is such a high-speed DAC feasible in Silicon?"</u>

#### <u>Response:</u>

First of all, CRL has implemented a test-bed with a software programmable digital architecture in order not to carry out SSA but to evaluate various UWB schemes with different parameters, e.g. waveforms, modulation schemes etc.

- > Although SSA is feasible with a different architecture, we can also use the test-bed to analyze sensitivity of pulse shaping in spectral design.
- Honestly to reply for this question, using the test-bed we have decreased the bits and sampling rate starting from 71.2 GS/s to 8.9 GS/s (71.2, 35.6, 17.8, and 8.9 GS/s) with 4-bit or 3-bit quantization, in order to investigate the necessary requirement of DAC implementation.
- It has been tested that the DAC implementation of 3-bit or 4-bit, 8 GS/s is feasible and available, utilizing present digital signal processing (DSP) technologies. Some related information are provided in the following slides.
- Other analog CMOS silicon architectures have been implemented for SSA feasibility study separately. They will be announced shortly.

#### Additional information as reference:

By the way, the correct expression for SSA is Soft-Spectrum Adaptation, not "Soft Spectral Adaptation".

➢ In a paper presentation at the ISSCC2004, January, San Francisco, the TelASIC Communications team has presented the details of a 3-bit ADC/DAC chip that demonstrated full functionality to sample at >40 GSPS.

The team has also demonstrated the ability to route signals at a 40 GHz clock rate on chip, while taking into account the parasitic interconnect elements that degrade the signal.

\* W. Cheng, et al. , (TelASIC Communications), "A 3b 40GS/s ADC/DAC in 0.12  $\mu$ m SiGe", ISSCC2004, 14.6, January 2004.

### Additional information as reference (cont.):



# Relation between the sampling rate and resolution bits of ADC/DAC

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### Q 1.b: "What is the expected power consumption and die-area of such a high-speed DAC?"

<u>Response:</u>

The expected power consumption and die-area for the currently tested RF unit including the digital SSA pulse generator with DAC is totally 3.2 mm\*mm and 63 mW, respectively.

### Q 1.c: "What is the trade-off between the DAC sampling rate and the depth and width of the notch that can be generated using SSA?"

#### Response:

It has been observed that decreasing the DAC sampling rate had affected the depth of the required notch in the designed SSA pulse wavelet, namely, decreasing the sampling rate would lower the notch depth to some extent.
Moreover, it has been found that the lower the DAC sampling rate (i.e. fewer quantization bits) we used, the more severe spectrum side-lobes of SSA pulse waveform would be produced.

According to CRL's Test-bed results, using quantization
<3-bit would cause severe spectrum side-lobe problem.</li>

## Response to Q 1.c (cont.):



Spectrum characteristics of SSA-UWB pulse wavelet (Test-bed, low DAC sampling rate) Spectrum characteristics of SSA-UWB pulse wavelet (Test-bed, high DAC sampling rate)

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### Response to Q 1.c (cont.):



Relation between the sampling rate and spectrum characteristics of SSA pulse wavelet (4-bit quantization)

### Response to Q 1.c (cont.):



Relation between the sampling rate and spectrum characteristics of SSA pulse wavelet (3-bit quantization)

Q 1.d: "If it is not feasible to implement the SSA scheme in Silicon, are there any other mechanisms that can be used to ensure worldwide compliance? If yes, can you provide details?" <u>Response:</u>

In fact, CRL and CRL-UWB Consortium have also chosen another approach, namely analog circuit processing, to realize SSA pulse waveform.

Two analog CMOS-MMIC's have been successfully implemented for SSA feasibility study. They will be announced shortly.

The basic method and philosophy are very near to the multiband pulse generation of 3.0-3.8 ns.

Detail information on them will be announced lately at Joint UWBST&IWUWBS2004 in Kyoto, May 18-21, 2004.

### 2. Brief history retrospect of SSA-UWB PHY proposal

- Design a proper pulse wavelet with high frequency efficiency corresponding to any regulatory frequency mask.
- Adjust transmitted signal's spectra adaptively, so as to minimize interference with co-existing systems.



### Features of SSA-UWB

- SSA-UWB with flexible pulse waveform and frequency band can be applied to single and multiband/multi-carrier UWB by
  - → <u>Free-verse type</u> pulse waveform shaping and
  - $\rightarrow$  <u>Geometrical type</u> pulse waveform shaping, respectively.
- Interference avoidance for co-existence, harmonization for various systems, and global implementation can be realized.
  - → <u>SSA-UWB</u> can flexibly adjust UWB signal spectrum so as to match with spectral restriction in transmission power, i.e. spectral masks in both cases of <u>single</u> and <u>multiple</u> bands.
- Scalable, adaptive performance improvement.
- Smooth system version-up similar to Software Defined Radio (SDR).



#### SSA-UWB with flexible band plan



In the future, if the restricting ruggedness of regional spectral mask (e.g. FCC mask) is eased, band allocation can be extended below 3.1 GHz or above 10.6 GHz.



Soft-Spectrum Adaptation (SSA) can correspond freely

### 3. Implementation realization of SSA-UWB transceiver

Press Release by Communications Research Laboratory (CRL):

"Tokyo, Japan, March 15, 2004 – Communications Research Laboratory (CRL) today announced an achievement for having developed a world's first Ultra Wideband (UWB) transceiver modules using 0.18micron CMOS-MMIC technology, realizing maximum data rate of 320 Mbps jointly with a number of industry members in CRL-UWB Consortium. These UWB transceiver modules can be applied to Soft-Spectrum Adaptation (SSA), not only for impulse radio transfer but also for multi-band OFDM transfer etc. It will be used for high data rate transmission evaluation, interference avoidance and UWB regulation establishment. Detailed information are expected to be published at the Joint UWBST&IWUWBS 2004, Kyoto, in May 2004. " Remark: CRL will be reorganized to be NICT by merging with TAO since April 1, 2004.

### Realization of UWB transceiver module based on CMOS-MMIC process



#### Geometrical-type SSA-UWB transceiver module

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### Realization of UWB transceiver module based on CMOS-MMIC process (cont.)



#### Free-verse-type SSA-UWB transceiver module

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### Architecture of SSA-UWB transceiver



### Hardware of geometrical-type SSA-UWB (cont.)



# Hardware for Geometrical SSA



### Realization of SSA-UWB transceiver

Detector of the SSA transceiver consists of <u>mixer</u> with local sine generator and <u>correlator with template</u>, in sequence.

Both free-verse type and geometrical type pulses can be detected by this SSA transceiver.

That's why we call this receiving architecture as an <u>universal detector</u>.

#### **Time-Frequency Hopping band-pass amplifier**



### 4. Global harmonization and compromise based on SSA-UWB systems

- Global Regulatory Satisfaction: Soft-Spectrum adaptation(SSA) can satisfy the FCC Spectrum Mask and any Mask adaptively.
- Interference Avoidance: SSA can be applied to <u>avoid</u> possible interferences with other existing <u>narrowband wireless</u> systems.
- Global Harmonization: SSA is good for harmonization among different UWB systems because SSA includes various proposed UWB systems as its special case
- Future Version-up: SSA is so scalable as to accept future UWB systems with better performance like Software Defined Radio(SDR).

#### Harmonization and compromise by SSA-UWB



# 5. Conclusion remarks

- We have developed two transceiver modules using CMOS-MMIC process for various UWB schemes.
- This UWB transceiver module is suitable for SSA-based UWB transmission with flexible, dynamic pulse waveform shaping so that it can satisfy the FCC spectral mask and other regional regulations around the world.
- The UWB transceiver modules can be applied to Freeverse-type SSA scheme including impulse radio scheme as well as Geometrical-type SSA scheme including DS-UWB and MB-OFDM schemes.
- Since the Geometrical-type module can widely applicable, it is useful for compromising two PHY schemes.
- Scalable and adaptive performance improvement with multi-mode and multi-rate can be further expected by utilizing the improved SSA-UWB schemes.