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Re:	IEEE 802.16.3-00/24 call for contributions dated 2000-12-00
Abstract	This contribution is an 802.16.3 PHY proposal that advocates the use of Turbo Product Codes (TPCs) in either single carrier or multiple carrier implementations. The use of TPCs with either modulation approach provides for a more robust and cost effective system when compared to alternative forward error correction schemes. Implementation details and tradeoffs of both modulation schemes are described in detail.
Purpose	This document forms the basis of a proposed presentation to working group session #11 in Ottawa, Canada (22nd Jan, 2001 – 26th Jan, 2001).
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IEEE 802.16.3 PHY Utilizing Turbo Product Codes

**Dave Williams, Sean Sonander, Neil McSparron,
Garik Markarian and Keith Pickavance**

Advanced Hardware Architectures

Table of Contents

1 Scope

1.1 Introduction

This document describes a proposed Physical Layer (PHY) for IEEE802.16.3 Broadband Fixed Wireless Access (BFWA) systems in licensed frequency bands from 2-11GHz. It is assumed that in a communication system at least one subscriber station communicates with a base station via a point-to-multipoint (P-MP) radio air interface. The broadband wireless access (BWA) system provides digital two-way voice, data, and video services and targets wireless multimedia services to residential, small office home offices (SOHO), small- and medium-sized businesses and multi-tenant dwellings.

The BWA system provides access to one or more (public and private) core networks and the proposed systems serve fixed location customers. As mentioned above, the BWA system constitutes a PHY implementation in which at least one subscriber station communicates with a base station via a point-to-multipoint (P-MP) radio air interface supported by the PHY protocol. Radio communications in the 2-11 GHz frequency range allow near- and non-line-of sight situations between a base station and subscriber station. To reduce the effects of partial blockage, for example by foliage, very powerful forward error correction (FEC) techniques need to be implemented. Furthermore, to reduce the negative effects of multipath propagation, careful choice of modulation and equalization techniques is required. Figure 1 illustrates an example deployment configuration including the use of repeater. The BWA systems shall be deployable in both multiple cell systems and single cell (super cell) frequency reuse systems.

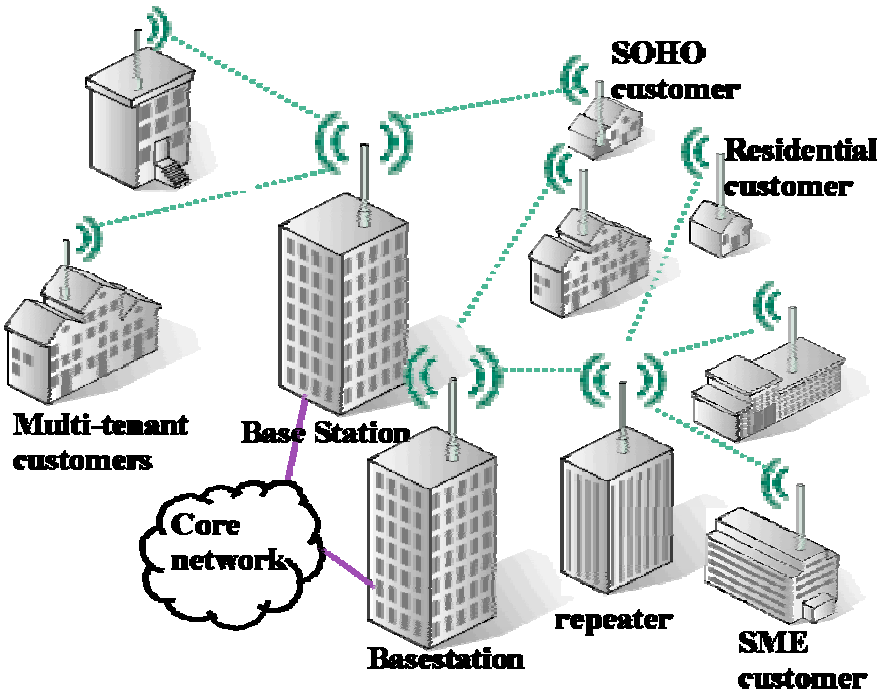

Figure 1 Example Deployment Configuration

1.2 Purpose of Proposal

It is the aim of this proposal to show the performance and suitability of Turbo Product Codes to both single carrier and multicarrier architectures. We provide PHY frameworks into which TPC's may be inserted. It is shown through coding examples in both single and multicarrier environments that TPC's offer substantially higher benefits than other coding schemes, a feature which may be exploited through higher coding rates, greater system operating range or lower transmission powers.

1.3 Format of Proposal

The proposal begins with a description of Turbo Product Codes, describing the encoding and decoding process, including shortening of TPC's. An example of TPC encoding is also included.

Following the TPC tutorial, a single carrier PHY framework is also included with a framing structure into which TPC's may easily be inserted. To balance the proposal, a multicarrier PHY framework is also presented, in which TPC's are featured.

The strength of the TPC based PHY proposals are backed up with simulation results under these frameworks.

1.3.1 Temp

1.3.2 Temp2

2 Turbo Code Description

The Block Turbo Code is a Turbo decoded Product Code (TPC). The idea of this coding scheme is to use well-known product codes in a matrix form for two-dimensional coding, or in a cubical form for three dimensions.

The matrix form of the two-dimensional code is depicted in Figure 2. The k_x information bits in the rows are encoded into n_x bits, by using a binary block (n_x, k_x) code. The binary block codes employed are based on extended Hamming codes.

The redundancy of the code is $r_x = n_x - k_x$ and d_x is the Hamming distance. After encoding the rows, the columns are encoded using another block code (n_y, k_y), where the check bits of the first code are also encoded. The overall block size of such a product code is $n = n_x \times n_y$, the total number of information bits $k = k_x \times k_y$ and the code rate is $R = R_x \times R_y$, where $R_i = k_i/n_i$, $i=x, y$. The Hamming distance of the product code is $d = d_x \times d_y$.

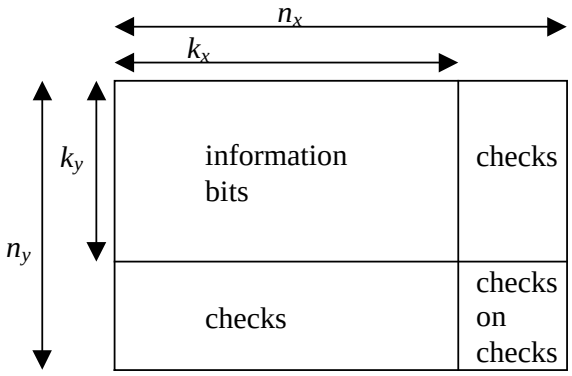

Figure 2 - Two-dimensional product code matrix

2.1 Encoding of a Turbo Product Code

The encoder for TPCs has near zero latency, and is constructed of linear feedback shift registers (LFSRs), storage elements, and control logic. Encoding of a product code requires that each bit be encoded by 2 or 3 codes.

The constituent codes of TPCs are extended Hamming or parity only codes. Table 1 gives the generator polynomials of the Hamming codes used in TPCs. For extended Hamming codes, an overall even parity check bit is added at the end of each codeword.

n	***k***	**Generator Polynomial**
7	4	$x^3 + x + 1$
15	11	$x^4 + x + 1$
31	26	$x^5 + x^2 + 1$
63	57	$x^6 + x + 1$
127	120	$x^7 + x^3 + 1$
255	247	$x^8 + x + 1$

Table 1 - Generators Polynomials of Hamming Codes

In order to encode the product code, each data bit is input both into a row encoder and a column encoder. Only one row encoder is necessary for the entire block, since data is input in row order. However, each column of the array is encoded with a separate encoder. Each column encoder is clocked for only one bit of the row, thus a more efficient method of column encoding is to store the column encoder states in a $k_x \times (n_y\text{-}k_y)$ storage memory. A single encoder can then be used for all columns of the array. With each bit input, the appropriate column encoder state is read from the memory, clocked, and written back to the memory.

The encoding process will be demonstrated with an example.

2.2 Example of a 2-Dimesional Product Code

Assume a two-dimensional (8,4) × (8,4) extended Hamming Product code is to be encoded. This block has 16 data bits, and 64 total encoded bits. Figure 3 shows the original 16 data bits denoted by D_{yx}. Of course the usual way is to have a serial stream of data of 16 bits and then label them as D_{11}, D_{21}, D_{31}, D_{41}, D_{12},…, D_{44}.

D_{11}	D_{21}	D_{31}	D_{41}
D_{12}	D_{22}	D_{32}	D_{42}
D_{13}	D_{23}	D_{33}	D_{43}
D_{14}	D_{24}	D_{34}	D_{44}

Figure 3 - Original Data for Encoding

The first four bits of the array are loaded into the row encoder in the order D_{11}, D_{21}, D_{31}, D_{41}. Each bit is also fed into a unique column encoder. Again, a single column encoder may be used, with the state of each column stored in a memory. After the fourth bit is input, the first row encoder error correction coding (ECC) bits are shifted out.

This process continues for all four rows of data. At this point, 32 bits have been output from the encoder, and the four column encoders are ready to shift out the column ECC bits. This data is also shifted out row-wise. This continues for the remaining 3 rows of the array. Figure 4 shows the final encoded block with the 48 generated ECC bits denoted by E_{yx}.

D_{11}	D_{21}	D_{31}	D_{41}	E_{51}	E_{61}	E_{71}	E_{81}
D_{12}	D_{22}	D_{32}	D_{42}	E_{52}	E_{62}	E_{72}	E_{82}
D_{13}	D_{23}	D_{33}	D_{43}	E_{53}	E_{63}	E_{73}	E_{83}
D_{14}	D_{24}	D_{34}	D_{44}	E_{54}	E_{64}	E_{74}	E_{84}
E_{15}	E_{25}	E_{35}	E_{45}	E_{55}	E_{65}	E_{75}	E_{85}
E_{16}	E_{26}	E_{36}	E_{46}	E_{56}	E_{66}	E_{76}	E_{86}
E_{17}	E_{27}	E_{37}	E_{47}	E_{57}	E_{67}	E_{77}	E_{87}
E_{18}	E_{28}	E_{38}	E_{48}	E_{58}	E_{68}	E_{78}	E_{88}

Figure 4 - Encoded Block

Transmission of the block over the channel may occur in a linear fashion, for example with all bits of the first row transmitted left to right followed by the second row, etc. This allows for the construction of a near zero latency encoder, since the data bits can be sent immediately over the channel, with the ECC bits inserted as necessary. For the (8,4)×(8,4) example, the output order for the 64 encoded bits would be

$D_{11}, D_{21}, D_{31}, D_{41}, E_{51}, E_{61}, E_{71}, E_{81}, D_{12}, D_{22},\ldots, E_{88}.$

Alternatively, a block based interleaver may be inserted to further improve the performance of the system.

2.2.1 3-Dimensional TPC Encoding

For a three-dimensional TPC block, the element ordering for input/output for both encoding and decoding is usually in the order of rows, columns and then the z-axis. If we consider a serial stream of (i×j×k) data bits, labeled as:

$D_{1,1,1}, D_{2,1,1}, D_{3,1,1},\ldots, D_{i,1,1}, D_{1,2,1}, D_{2,2,1},\ldots, D_{\mathrm{i,j,1}}, D_{1,1,2},\ldots, D_{i,j,k}.$

Note: this labeling is for convenience

Then the total size of the encoded block is ((i×j×k) + ECC bits), where there are p ECC bits for the x-axis, q ECC bits for the y-axis and r ECC bits for the z-axis, the bit order for input and output is:

$D_{1,1,1}, D_{2,1,1}, D_{3,1,1},\ldots, D_{\mathrm{i,1,1}},\ldots, E_{p,1,1}, D_{1,2,1}, D_{2,2,1},\ldots, E_{p,2,1},\ldots, E_{p,q,1}, D_{1,1,2}, D_{2,1,2},\ldots, E_{p,1,2},\ldots, E_{p,q,2},\ldots, E_{p,q,r}$

This is shown in Figure 5.

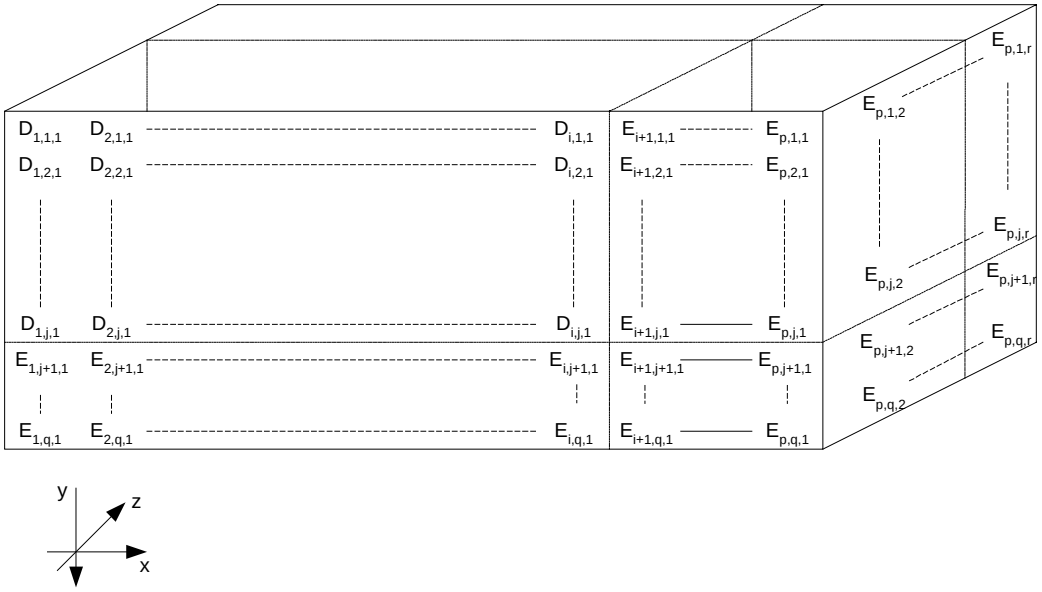

Figure 5 - Structure of 3-Dimensional TPC

Notation:

- the codes defined for the rows (x-axis) are binary (n_x,k_x) block codes
- the codes defined for the columns (y-axis) are binary (n_y,k_y) block codes
- the codes defined for the z-dimension (z-axis) are binary (n_z,k_z) block codes
- data bits are noted $D_{y,x,z}$ and parity bits are noted $E_{y,x,z}$

2.3 Shortened TPCs

To match packet sizes, a product code may be shortened by removing symbols from the array. In the two-dimensional case rows, columns or parts thereof can be removed until the appropriate size is reached. Unlike one-dimensional codes (such as Reed-Solomon codes), parity bits are removed as part of shortening process, helping to keep the code rate high.

There are two steps in the process of shortening of product codes. The first is to remove an entire row or column from a 2-dimensional code, or an entire X, Y, or Z plane from a 3-dimensional code. This is equivalent to shortening the constituent codes that make up the product code. This method enables a coarse granularity on shortening, and at the same time maintaining the highest code rate possible by removing both data and parity symbols. Further shortening is obtained by removing individual bits from the first row of a 2-dimensional code, or from the top plane of a 3-dimensional code.

2.4 Example of a Shortened 2-Dimensional TPC

For example, assume a 456-bit block size is required with a code rate of approximately 0.6. The base code chosen before shortening is the (32,26)×(32,26) code which has a data size of 676 bits. Shortening all rows by 5 bits and all columns by 4 bits results in a (27,21) × (28,22) code, with a data size of 462 bits. To get the exact block size, the first row of the product is shortened by an additional 6 bits. The final code is a (750,456) code, with a code rate of 0.608. Figure 6 shows the structure of the resultant block.

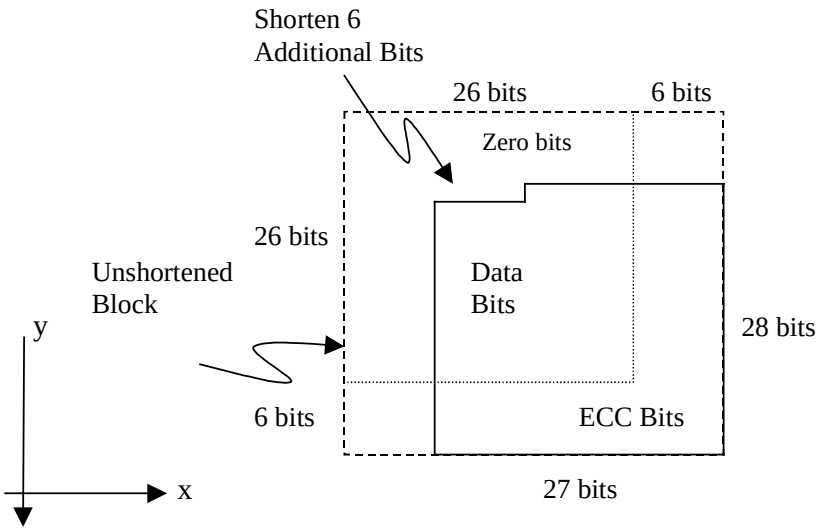

Figure 6 - Structure of Shortened 2 D Block

Modifications to the encoder to support shortening are minimal. The shortening procedure is trivial, and yet an extremely powerful tool that enables construction of a very versatile code set.

2.5 Example of a Shortened 3-Dimensional TPC

Suppose a 0.4 - 0.45 rate code is required with a data block size of 1096 bits. The following shows one possible method to create this code.

Start with a (32,26)×(32,26)×(4,3) code. The *optimum* shortening for this code is to remove rows and columns, while leaving the already very short z-axis alone. Therefore, since a 1096 bit 3-Dimensional code is required, the desired vector data size can be found by taking the square root of 1096/3 and rounding up. This yields a row/column size of about 20. In fact, having a row size of 20, a column size of 19, and a z-column size of 3 gives the closest block size to 1096 bits.

The code size is now a (26,20)×(25,19)×(4,3) = (2600,1140). To get the exact data size, we further shorten the first plane of the code by 44 bits. This is accomplished by shortening 2 full rows from the first (xy)-plane, with each row removing 20 bits from the data block, and shortening another 4 bits from the next row. This results in a (2544,1096) code, with rate = 0.43. The following diagram shows the original code, along with the physical location of the shortened bits.

Figure 7 shows the original code along with the physical location of the shortened bits.

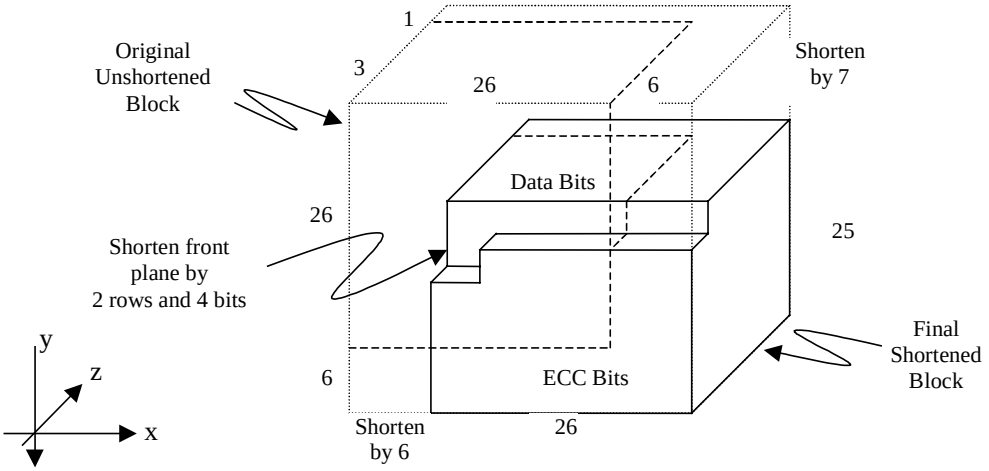

Figure 7 - Structure of Shortened 3-D Block

2.6 Iterative Decoding

Huge performance advantages may be directly associated with the decoding mechanism for product codes. There are many different ways to decode product codes and each has its merits, however, the goal is maximum performance for a manageable level of complexity.

It is known that if it is possible to use unquantised information (so called soft information) from the demodulator to decode an error correcting code, then an additional gain of up to 2 dB over fully quantised (hard decision) information is achievable. It is therefore desirable to have soft information decision available to the TPC decoder.

Of course, we could in theory consider the decoding of this code a single linear code of size $(n_x \times n_y \times n_z, k_x \times k_y \times k_z)$, using a soft decision decoder, but this will in general (apart from the smallest, and of course worst performing) be prohibitively complex.

It makes sense therefore, since these codes are constructed from (simple) constituent code that these soft decoders are used to decode the overall code. However until recently there have only been hard decision decoders for these constituent decoders. In recent years the computational power of devices has made it possible to consider (sub optimal) soft decision decoders for all linear codes. This is only half the solution as the main difficulty is with passing the information from one decoder to the next (i.e. when switching from decoding the rows to decoding the columns). For this, accuracy will need to be kept to a maximum, and so using soft input soft output (SISO) decoders will need to be considered. This is such that an estimate of the transmitted code word may be found and also an indication of the reliability. This new estimate may then be passed onto the next decoding cycle. Inevitably, there will be some degradation from optimal if we are to achieve our decoding using this method, but it does enable the complexity to be reduced to a level that can be implemented. Also, studies have shown that this degradation is very small, so this decoding system is very powerful.

What follows now is an explanation regarding the iterative nature of the decoding procedure. If we consider that, given 2-D TPC block, we define the first round of row and column decoding as a single iteration. We may then perform further iterations, if required. Thus, the main areas of investigation are that of the SISOs, and that of using some previously decoded information in subsequent decoding operations. These are both separate and yet connected areas of interest, as shall be explained.

With regards to the SISOs, there are many different methods including the following which have been described in detail in published academic papers:

1) Soft-Output Viterbi Algorithm (SOVA) [5]

2) The modified Chase algorithm [8]

3) The BCJR algorithm [6],

There have been many other papers explaining these algorithms both as independent algorithms for coding schemes and as part of turbo type decoding schemes. It must be noted that these are not the only algorithms that can achieve soft input soft output style decoding, but they are at present the most readily cited in academic literature.

Each block in a product code is decoded using the information from a previous block decoding. This is then repeated as many times as. In this way, each decoding iteration builds on the previous decoding performance.

Figure 8 illustrates the decoding of a 2-D TPC. Note here that prior to each decoding there needs to be a mathematical operation on all the data we have at that particular time, that is the current estimate of the decoded bits, the original estimate from the demodulator (this will not be used in the first decoding) and the channel information (where applicable).

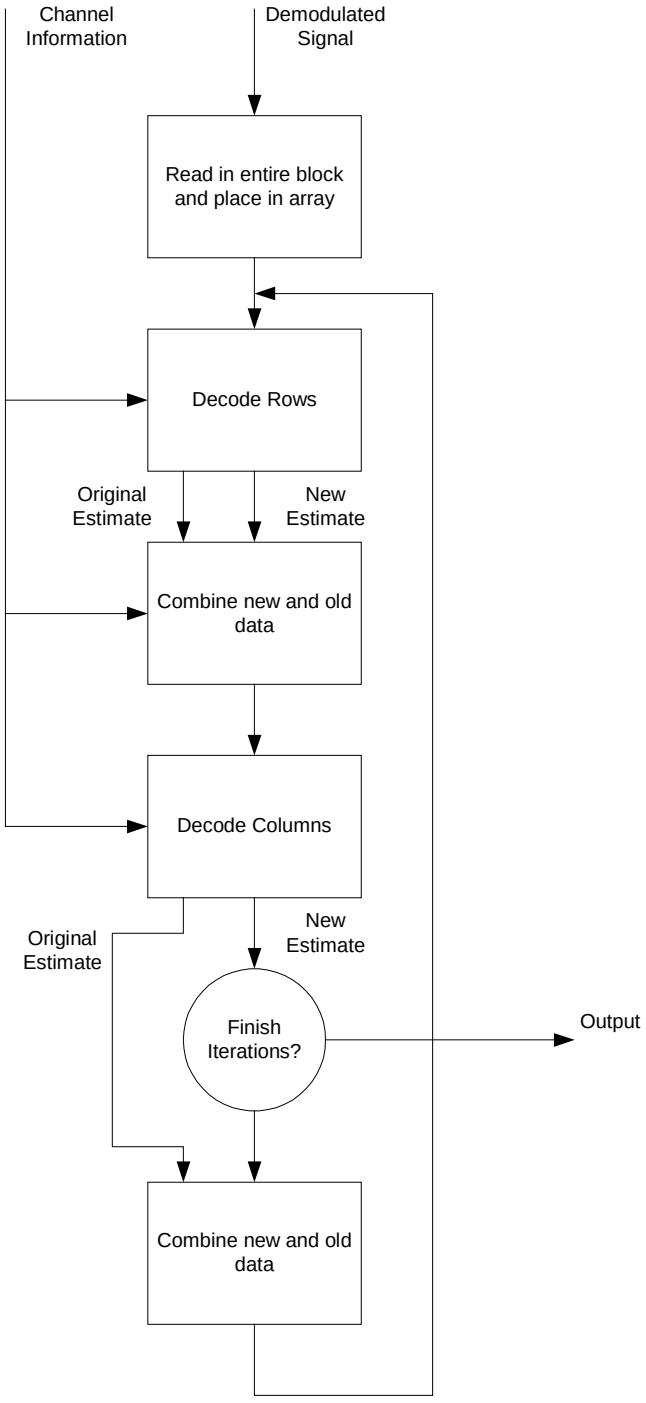

Figure 8 Procedure for decoding of 2-D TPC

It can easily be seen from Figure 8 that the iteration idea is applicable to one complete decoding of the rows and one complete decoding of the columns.

There is an obvious question as to how the iteration procedure is terminated. This is a question only answerable by the system provider and depends on performance and delay; more iterations imply better performance as the expense of a larger latency. Of course, over clocking the system in comparison can

significantly reduce the latency. When considering hardware, the problem of varying delays may be encountered, thus it may be advantageous to fix the number of iterations performed.

3 Bit mapping, Baseband Shaping and Modulation for Single Carrier Systems

3.1 Downstream Channel

The downstream channel supports both continuous and burst mode operation and the proposed FEC incorporates different turbo product codes, for each of these applications. In order to provide the desired flexibility and the required QoS, an adaptive modulation scheme is proposed and different modulation formats and TPC's can be defined on a subscriber level basis. Adaptation of the modulation technique is arranged on a frame-by-frame basis, whereby each frame contains an identification section for a chosen modulation technique. Figure 9 shows the block diagram for the downstream channel.

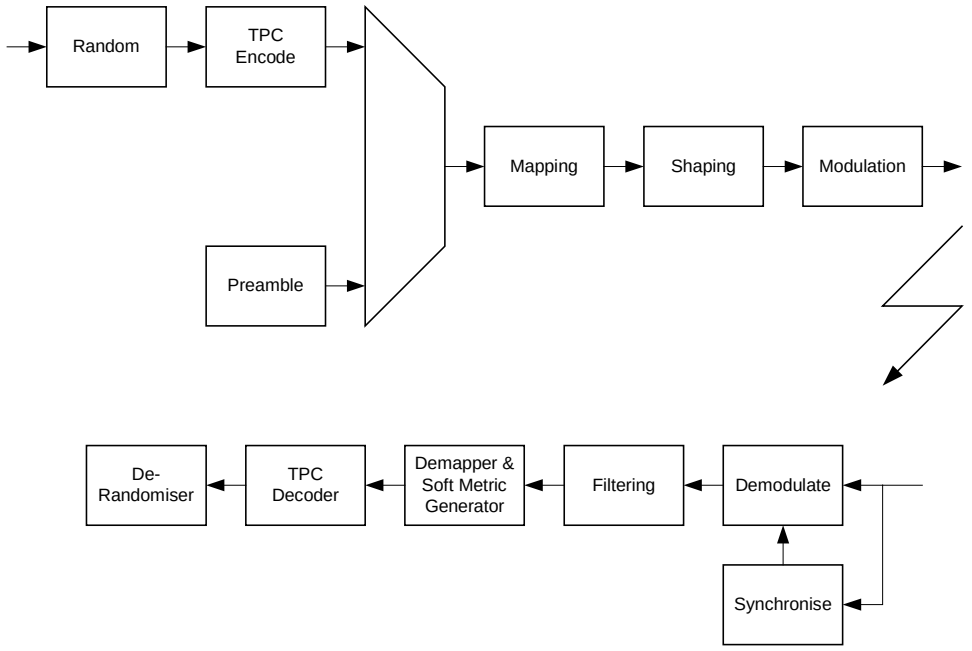

Figure 9 Block Diagram of the Downstream Channel

3.1.1 Randomization for Spectrum Shaping

Prior to FEC encoding, the downstream channel will be randomized to ensure sufficient bit transitions to support clock recovery and to minimize occurrence of the un-modulated carrier frequency. This process is done by modulo-2 addition (XOR'ing) the data with the output of the Linear-Feedback Shift Register (LFSR) with characteristic polynomial $1+X^{14}+X^{15}$. The LFSR is cleared and preset at the beginning of each burst to a known value – 100101010000000.

Only information bits, not preambles are randomized. The LFSR sequence generator pauses while parity bits are being transmitted.

3.1.2 Downstream Modulation Techniques

The selected downstream modulation is: either QPSK, 16 QAM or 64 QAM.

3.1.3 Symbol Mapping

The mapping of bits into *I* and *Q* axis will be based on Gray-codes for all constellations.

3.1.4 Baseband Pulse Shaping

Prior to modulation, *I* and *Q* signals shall be filtered by square-root raised cosine. The roll-off factor α shall be either 0.15 or 0.25. The ideal square-root cosine is defined by the following transfer function *H*(*f*):

$$H(f) = 1 \qquad for \quad |f| \; \langle \quad f_N(1-\alpha)$$

$$H(f) = \left\{ \frac{1}{2} + \frac{1}{2}\sin\frac{\pi}{2f_N}\left[\frac{f_N - |f|}{\alpha}\right] \right\}^{1/2} \qquad for \quad f_N(1-\alpha) \le |f| \le f_N(1+\alpha)$$

$$H(f) = 0 \qquad for \quad |f| \ge f_N(1+\alpha)$$

Where:

$$f_N = \frac{1}{2T_S} = \frac{R_S}{2}$$

is the Nyquist frequency, and Ts is modulation symbol duration.

3.1.5 TDD / FDD

The Single Carrier system will support both a TDD/TDMA uplink and downlink mode of operation and an FDD mode with a continuous downlink and a TDMA uplink.

The TDD/TDMA mode uses a minimum of spectrum and potentially allows the design of simpler RF systems, however, a guard time is needed between uplink and downlink transmissions reducing the overall system capacity.

The FDD mode allows the system to operate with a continuous mode downlink, thus potentially increasing the downlink capacity. However, potentially it forces an operator to operate with an asymmetric system capacity in the uplink and downlink.

3.1.6 Single Carrier Framing Structure

In order to support both proposed modes of operation, TDD and FDD, it is proposed to use a Framing format similar to IEEE 802.16.1.

A preamble is proposed for the start of each downstream / upstream burst in TDD mode followed by a set of signalling bits which signal the combination of FEC / modulation used in the burst. A signalling protocol similar to that proposed in section 4.3 could be used. In the case of the continuous downstream mode the preamble is repeated on a regular basis – possibly every 1ms.

The preamble sequence should be 48 symbols long to optimise the equalizer. It would be possible to modify this structure to allow equalization using Frequency Domain Equalization techniques.

3.1.7 Typical performance with TPC

The performance cited here are based on results given in IEEE802.16.1pc-00/35 [10]**.** That is, 5 decoding iterations and quantization of soft metrics into sign + 3 bits per one dimensional modulation level. No interleaver is assumed. The typical performances for different transmission modes are presented in Table 2 and Table 3.

Code	$(32,26)^2$(16.11), QPSK	$(32,26)^2$(16.11), 16 QAM	$(32,26)^2$(16.11), 64 QAM
Code Rate	0.454	0.454	0.454
Eb/No @BER=10^{-6}	1.5	4.7	8.3
Eb/No @BER=10^{-9}	1.8	5.1	8.6

Table 2 Typical performance for TPC with Large Code Block Continuous Transmission

CODE	$(39, 32)^2$, S1=S2=25, s=0	$(46, 39)^2$ S1=S2=18, s=17	$(63, 56)^2$, S1=S2=1, s=0
Rate	0.673	0.717	0.790
Eb/N0 dB @10^{-6} 4/16/64 QAM	3.5 / 6.5/ 10.7	3.6 / 6.6 / 10.5	3.5 / 6.6 / 10.6
Eb/N0 dB @10^{-9} 4/16/64 QAM	4.3 / 7.5 / 11.7	4.3 / 7.8 / 11.5	4.3 /7.5 / 11.6
Block size, information bits or … (bytes)	1024 (128 bytes)	1504 (188 bytes)	3136 (392 bytes)
Encoder Complexity	10 Kgates	10 Kgates	10 Kgates
Decoder Complexity	Less than 150Kgates	Less than 150Kgates	Less than 150Kgates

Table 3 Typical Performance for TPCs with Small Code Block Burst Transmission

3.2 Upstream Channel

The upstream channel supports only burst mode and has signal-processing units as described for the downstream channel. The subscriber stations are permitted to transmit only after receiving a confirmation from the base station through the MAC messages. The configuration of the upstream channel can be adjusted on a burst-by-burst basis.

3.2.1 Upstream Randomization

The upstream modulator implements a randomizer using a LFSR with the connection polynomial $X^{15} + X^{14} + 1$, with a 15-bit programmable seed. At the beginning of each burst, the register is cleared and the seed value is loaded. The seed value is used to calculate the scrambler output bit, obtained as the XOR of the seed with first bit of DATA of each burst (which is the MSB of the first symbol following the last symbol of the preamble).

3.2.2 FEC Scheme for the Upstream Channel

The FEC in the upstream channel is used to significantly reduce the required C/I level needed for reliable communication, and can be used to extend the range of a base station or increase code rate for greater throughput.

It is expected that for the upstream channel, variable packet size from 14 to 392 bytes will be used. As explained in downstream channel coding Chapter – TPCs support all of this range based on Extended

Hamming constituent codes (64, 57) and (32, 26), combined with code shortening. It is expected that short packets can be used in the upstream channel.

3.2.3 Interleaving for the upstream channel

Interleaving for the upstream channel is not proposed for the TPC implementation but may be added if deemed desirable.

3.2.4 Upstream Modulation Techniques

The selected upstream modulation is QPSK, 16 QAM or 64 QAM.

3.2.5 Baseband Pulse Shaping

Prior to modulation, the I and Q signals shall be filtered by square-root raised cosine. The roll-off factor α shall be either 0.15 or 0.25. The ideal square-root cosine is defined by the following transfer function H(f):

$$H(f) = 1 \qquad for \quad |f| \; \langle \quad f_N(1-\alpha)$$

$$H(f) = \left\{ \frac{1}{2} + \frac{1}{2} \sin \frac{\pi}{2 f_N} \left[\frac{f_N - |f|}{\alpha} \right] \right\}^{1/2} \qquad for \quad f_N(1-\alpha) \le |f| \le f_N(1+\alpha)$$

$$H(f) = 0 \qquad for \quad |f| \ge f_N(1+\alpha)$$

where

$$f_N = \frac{1}{2T_S} = \frac{R_S}{2}$$

is the Nyquist frequency, and T_S is the modulation symbol duration.

3.2.6 Typical Performance for Upstream Channel

The performance cited here are based on results given in IEEE802.16.1pc-00/35 [9]. That is, 5 iterations and quantization of soft metrics into sign + 3 bits per one dimensional modulation level. No interleaver is assumed. The typical performances for different transmission modes are presented in the Table 4.

CODE	$(16, 11)^2$, S1=S2=0, s=9	(30, 24) *(25, 19) S1=2, S2=7, s=0
Rate	0.453	0.608
Eb/N0 dB @10^{-6} 4/16/64 QAM	4.0 / 6.8/ 9.8	3.4 / 6.3 / 10
Eb/N0 dB @10^{-9} 4/16/64 QAM	5.8 / 8.8 / 11.8	4.7 / 7.5 / 11.5
Block size, information bits or (bytes)	112 (14 bytes)	456 (57 bytes)
Encoder Complexity	10 Kgates	10 Kgates
Decoder Complexity	Less than 150Kgates	Less than 150Kgates

Table 4 Typical performance for TPC with small blocks (upstream channel)

4 Multi Carrier Modem and TPC's

4.1 Introduction

The performance of an OFDM modulation system may gain significantly from proper usage of stronger error correction codes, such as turbo codes. In particular turbo product codes as defined in IEEE802.16.1 are recommended for the following system modes to enhance the system performance in both LOS and NLOS operating conditions:

i. A 64-point FFT based OFDM mode as the baseline scheme. TPCs and convolutional code form the baseline coding schemes.

ii. An optional 256-point FFT based OFDM mode, with TPCs and convolutional codes as baseline codes.

Unlike 802.11a, a Fourier period of 16 microseconds and a guard period of 1/8 Fourier period is used here for the 64 pt FFT. For the 256 point FFT OFDM symbol, a Fourier period of 64 microseconds is used, coupled with a guard time of 1/8 Fourier period.

In the following sub sections, we describe a multicarrier PHY with Turbo Product Codes.

4.2 64 Point FFT Mode

The OFDM structure for this mode remains almost unchanged from the 802.11a PHY specification. One difference is the shortened guard interval, from 1/4 to 1/8 of the 64 point IFFT. Another difference is the proposal to use the reserved bit in the PLCP header of the SIGNAL OFDM symbol to signify operation with a TPC FEC. It is proposed to leave the PLCP header encoded using the rate ½ convolutional code to maintain backwards compatibility. The MAC protocol would signal the availability of the TPC option.

As with 802.11a, the carrier spacing is 62.5 KHz.

4.2.1 Subcarrier Allocation

The 64-point frame structure would contain 48 data carriers, 12 null carriers. One of the null carriers is the center carrier and 4 continuous pilot tones. It is proposed that the Guard Interval is 1/8 of the symbol time.

Null Carriers	{0,..,5},33,{59,63}
Pilots	{12,26,40,54}
Other carriers	48 data carriers.
Data Symbols	QPSK, 16QAM or 64QAM coded.

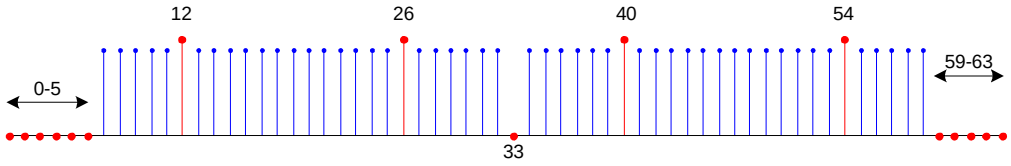

Figure 10 Frequency Structure of 64 Point FFT

4.2.2 Date Rates

The following information is based on the timing for the OFDM symbols, as described in section 4.1. The array of allowable data rate for this format is shown in Table 5.

Subcarrier Modulation	Coding Rate	Data Rate /Mbit/s	Coded Bits per OFDM symbol	Data bits per OFDM symbol
BPSK	1/2	1.33	48	24
BPSK	3/4	2.00	48	36
QPSK	1/2	2.66	96	48
QPSK	3/4	4.00	96	72
16 QAM	1/2	5.33	192	96
16 QAM	3/4	8.00	192	144
64 QAM	2/3	10.67	288	192
64 QAM	3/4	12.00	288	216

Table 5 64 Point FFT Structure Parameters

4.2.3 Convolutional Coding for 64 point FFT Structure

The convolutional coding implemented with this scheme is as 802.11a, supporting rates 1/2, 2/3 and 3/4. The convolutional encoder, complete with connectivity is shown in Figure 11.

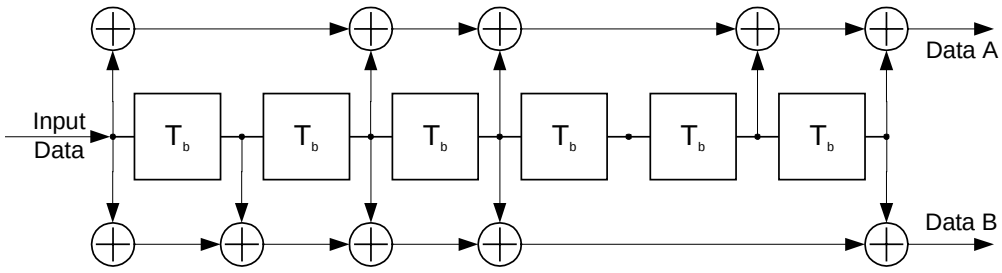

Figure 11 Convolutional Encoder

The puncturing matrices are as follows:

Rate = 3/4:

$$G = \begin{pmatrix} 1 & 1 & 0 \\ 1 & 0 & 1 \end{pmatrix}$$

Rate = 2/3:

$$G = \begin{pmatrix} 1 & 1 \\ 1 & 0 \end{pmatrix}$$

4.2.4 TPC Coding for 64 point FFT Structure

Turbo Product codes, which are best suited to the framing structure of the suggested OFDM symbols, have block lengths that fit evenly into a number of symbols. In the case of the 802.11a symbol framing structure, the number of coded bits per OFDM symbol is given in Table 5. Thus, depending on the sub carrier modulation scheme selected, one best TPC may be chosen, defined by system requirements, such as required data rates, performance, etc.

4.2.5 Performance of Scheme

Simulation results based on the 802.11a standard have been obtained, using convolutional codes and TPC's. Two codes have been simulated; the first of these codes is a (1269,848) Turbo Product Code, with rate 0.668. The equivalent convolutional code is the rate 2/3 code. When simulated in fading conditions, using 64 QAM as the subcarrier modulation, the TPC show a clear 2 dB performance improvement over the convolutional codes at a packet error rate of 10^{-2}.

The second code simulated is the (2304,1681) TPC code compared with it nearest convolutional neighbor, the rate 3/4 convolutional code. Under fading conditions, this TPC outperforms the convolutional code by 3.5 dB.

4.3 256 Point FFT Mode

The framing structure for the 256-point FFT mode follows the same concepts and principles as the 64-point mode. An additional continuous mode is defined which does not include the short OFDM training sequence.

4.3.1 Symbol Level Framing Structure

The framing structure for the 256-point TDMA mode of operation is as follows:

Each burst consists of:

- 6 Short Reference Symbols, followed by
- 2 Long Reference Symbols, followed by
- 1 Signalling Symbol, followed by
- Data Symbols

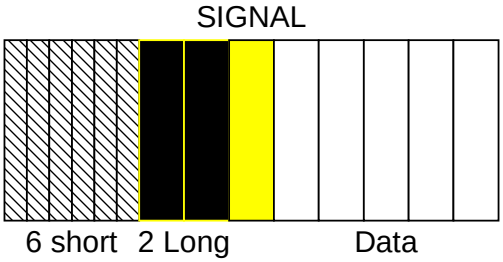

Figure 12 Symbol Level Framing Structure 256 Point Mode

The structure for the continuous TDM mode of operation is as follows:

- 1 Long Reference Symbol, followed by
- 1 Signalling Symbol, followed by
- 48 Data Symbols, followed by
- 1 Long Reference Symbol, etc.

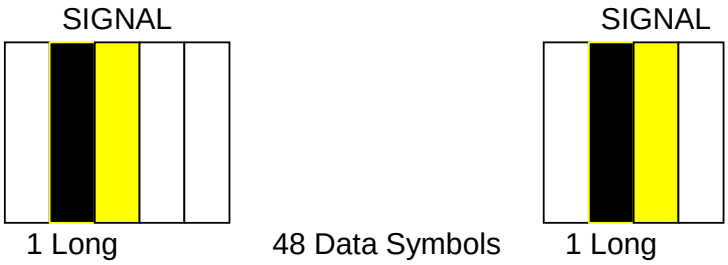

Figure 13 Framing Structure for Continuous TDM Mode

The short and long reference symbols are to be decided.

4.3.2 SIGNAL Symbol for 256 Point FFT Mode

The signal symbol is BPSK modulated with a rate ½ convolutional code giving 96 data bits.

These are allocated as follows:

- F1, F2 Define the FEC scheme
- R1, R2, R3, R4 Define the code rate
- L1 to L6 define the number of OFDM symbols using the specified FEC
- P1 to P6 parity check bits for the 6 possible combinations of Modulation and FEC allowed in any one frame.

0	1	2	3	4	5	6	7	8	9	10	11	12	13
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

14	15	16	17	18	19	20	21	22	23	24	25	26	27
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

28	29	30	31	32	33	34	35	36	37	38	39	40	41
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

42	43	44	45	46	47	48	49	50	51	52	53	54	55
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

56	57	58	59	60	61	62	63	64	65	66	67	68	69
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

70	71	72	73	74	75	76	77	78	79	80	81	82	83
F1	F2	R1	R2	R3	R4	M1	M2	L1	L2	L3	L4	L5	L6

84	85	86	87	88	89	90	91	92	93	94	95
P1	P2	P3	P4	P5	P6	0	0	0	0	0	0

Table 6 Allocation Table for 256 Point FFT Mode

4.3.3 Subcarrier Allocation – Data Symbols

The 256-point frame structure would contain 192 data carriers, 48 null carriers. One of the null carriers is the center carrier and 16 continuous pilot tones. It is proposed that the Guard Interval remains 1/8 of the symbol time. As the absolute symbol time increases by a factor of 4 compared to the 64 point FFT so the Guard Interval will protect against multipath interference that includes echoes 4 times longer than the 64 point mode.

Null Carriers {0, ..,23},128,{233,255}

Pilots {24, 38, 52, 66, 80, 94, 108, 122, 134, 148, 162, 176, 190, 204, 218, 232}

Other carriers 192 data carriers.

Data Symbols QPSK, 16QAM or 64QAM coded.

Advantages of this structure are:

Improved multipath protection

More pilot tones for AFC

Regularly spaced tones give a possibility of performing some limited channel estimation on an individual data symbol basis.

Data Symbols may be QPSK, 16QAM or 64QAM coded.

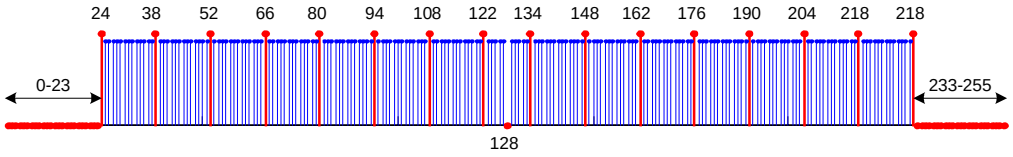

Figure 14 Frequency Structure of 256 Point FFT

4.3.4 Data Rates

The following information is based on the timing for the OFDM symbols, as described in section 4.1. One particular array of allowable data rates for this format is shown in Table 7.

Subcarrier Modulation	Coding Rate	Data Rate /Mbit/s	Code Bits per OFDM symbol	Data bits per OFDM symbol
BPSK	1/2	1.33	192	96
BPSK	3/4	2.00	192	144
QPSK	1/2	2.66	384	192
QPSK	3/4	4.00	384	288
16 QAM	1/2	5.33	768	376
16 QAM	3/4	8.00	768	576
64 QAM	2/3	10.67	1152	768
64 QAM	3/4	12.00	1152	864

Table 7 Data Rates for 256 Point FFT Structure

4.3.5 Convolutional Coding for 256 point FFT Structure

The convolutional coding implemented with this scheme is as 802.11a, supporting rates 1/2, 2/3 and 3/4. See section 4.2.3 for more details.

4.3.6 TPC Coding for 256 point FFT Structure

Turbo Product codes, which are best suited to the framing structure of the suggested OFDM symbols have block lengths that fit evenly into a number of symbols. In the case of the 802.11a symbol framing structure, the number of coded bits per OFDM symbol is given in Table 7. Thus, depending on the sub carrier modulation scheme selected, one best TPC may be chosen, defined by system requirements, such as required data rates, performance, etc.

4.4 Subcarrier Mapping

As mentioned in 4.2.1 and 4.3.3, the allowed subcarrier modulation schemes for both the 64 and 256 point FFT based OFDM symbols, are BPSK, QPSK, 16 QAM and 256 QAM. The constellation bit encoding is depicted in the following tables:

Input Bits b0, b1, b2	I - out	Output Bits b3,b4,b5	Q - out
000	-7	000	-7
001	-5	001	-5
011	-3	011	-3
010	-1	010	-1
110	1	110	1
111	3	111	3
101	5	101	5
100	7	100	7

Table 8 256 Point FFT Structure Parameters

Input Bits b0,b1	I - out	Output Bits b2,b3	Q- out
00	-3	00	-3
01	-1	01	-1
11	1	11	1
10	3	10	3

Table 9 16 QAM Mapping

Input Bits b0	I - out	Input Bits b1	Q - out
0	-1	0	-1
1	1	1	1

Table 10 QPSK Mapping

Input Bits b0	I - out
0	-1
1	1

Table 11 BPSK Mapping

NB. Scaling factors are used to ensure constant signal power.

4.5 Duplex Operation

The proposed OFDM PHY will support both TDD / TDMA and FDD with a TDM downlink and a TDMA uplink. It is proposed that the 64 point mode will only operate in a duplex mode using the TDD / TDMA. The 256 point mode will support both the TDD / TDMA duplex and FDD mode using TDM for the downlink and TDMA for the uplink frequency.

4.5.1 TDD Duplex

Sharing the channel for Uplink and Downlink – example 64 point FFT mode.

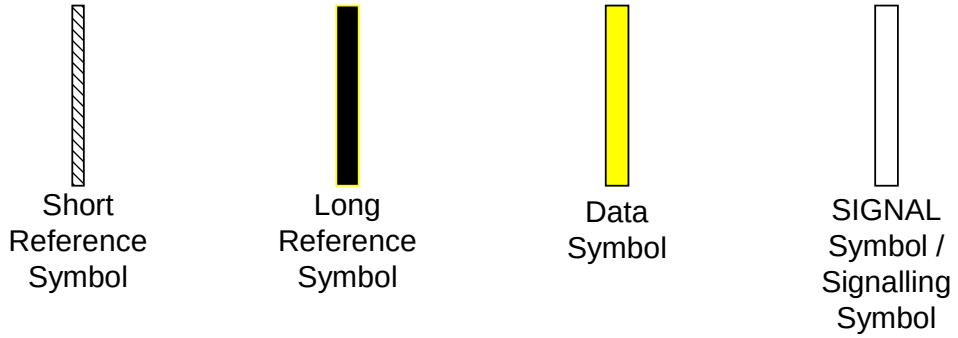

Figure 15 Symbol Key

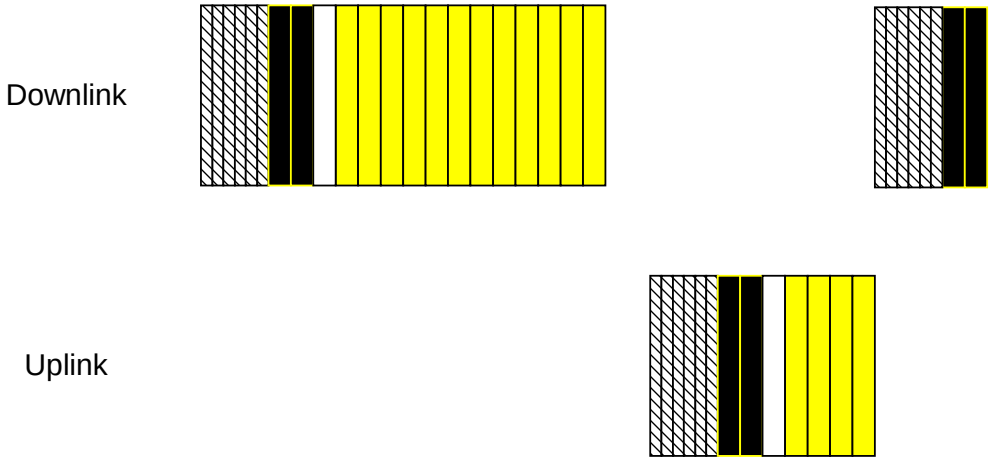

Figure 16 TDD Duplex Operation

4.5.2 FDD Duplex

The FDD operating mode supported by the 256 point FFT system only. A regular framing structure is proposed for the downlink.

A framing structure for the continuous downlink is proposed to start with a single Long Reference symbol followed by a SIGNAL symbol followed by 48 data symbols making a 50 symbol repeating structure.

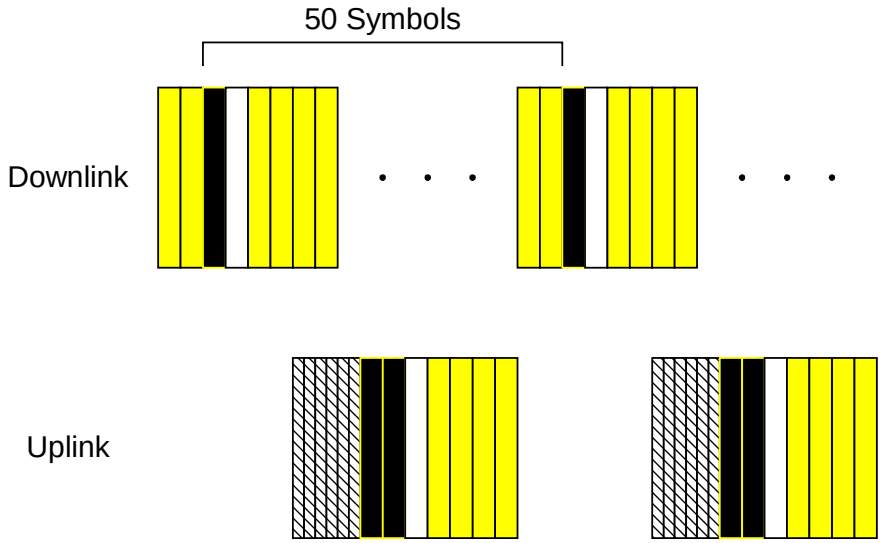

Figure 17 FDD Duplex Operation

5 Antenna Systems

The PHY layer will support the future applications of a smart antenna i.e. having the primary feature of providing the ability to track the line of sight target within a predetermined angle of uncertainty. Typically, one would expect 3 or more degrees of tracking. This active tracking capability of smart antennae will potentially provide better coexistence and will optimize the antenna pattern.

6 Addressing Evaluation Criteria

This proposal shows that TPC's when used in conjunction with both single carrier and multicarrier modulation schemes, offers excellent performance. Given the flexibility of TPC's, in terms of block length, information length and performance, Turbo Product Codes (TPCs) provide a near optimal coding solution. TPCs have an inherent flexibility in code rate (0.2 to 0.98) and block size (4 to 1800 bytes) to meet most any requirement whether it be a single carrier or multiple carrier (OFDM) system. In addition, basic TPC technology is free of intellectual property constraints, with multiple vendors offering solutions and an inherent implementation cost that is consistent with both base station and subscriber station targets.

Table 12 below includes a description of the evaluation criteria and addresses the proposals contribution in this area.

Number	Criteria	Proposal meets Criteria
1	Meets system requirements	This proposal addresses both single carrier and the multicarrier frameworks and as such offers two alternative approaches that will meet the system requirements. This proposal builds on the strengths of 802.16.1 and 802.11a by utilizing the most appropriate portions of these standards.
2	Channel Efficiency	Single carrier and multicarrier modems address issues of channel efficiency in different ways. For the multicarrier option, the channel spectrum efficiency ranges between 0.38 bits/sec/Hz and 3.43 bits/sec/Hz, for both the 64 point FFT and the 256 point FFT option. The proposed channel bandwidth is 3.5 MHz. The data rates supported vary between 1.33 Mbps (BPSK option, 1/2 rate code) and 12 Mbps (64 QAM, 3/4 rate code).
3	Simplicity of Realization	Both the single carrier and multicarrier approaches suggested in this proposal are capable of providing a cost efficient solution for the base station and subscriber station. Installation costs for the two approaches should be similar. All of the afore mentioned technology draws upon existing, well understood technologies. In particular, 802.11a and 802.16.1. Both single carrier and multicarrier modulation techniques are well know and well understood. The coding techniques suggested are also well known and used. Turbo Product Codes (TPCs are very widely used and researched (section 2)). Also included are the industry standard convolutional codes (section 4.2.3).
4	Channel Spectrum Flexibility	Channel spectrum flexibility is met in the single carrier system by scalability of the allocated bandwidth to the modulated signal. This may be achieved, for example, by modifying the system clocks. For the case of the multicarrier system, the data rates in Table 5 are based upon a scaled 802.11a set of parameters, to 3.5 MHz. Thus any realistic bandwidth may be easily incorporated. Thus the framework mentioned in this proposal allows for a broad range of spectrum occupancies.
5	System service flexibility	The convergence layer between the PHY and the MAC is transparent for both the single carrier and multicarrier proposal. Many re-definable parameters have been included in the proposal, such as data rates, modulation scheme etc., giving the overall scheme a good degree of service flexibility. Both of proposed frameworks (single carrier and multicarrier) readily support FRD optional services and with the inherent flexibility of these architectures (which utilize highly flexible turbo product coding) both of these approaches will be able to meet the challenges of many potential future services.

6	Robustness to interference	The use of Turbo Product Codes in both approaches suggested in this proposal provide a very high level of resistance to intra-system interference, co-channel interference, adjacent channel interference and spectral spillage resulting from the respective modulation schemes. In particular, TPCs can provide 3 dB or more of additional coding gain when compared to legacy coding solutions such as RS or Convolutional codes as well as providing superior burst error correction capability. In addition, the modulation schemes proposed also offer an inherent ability to combat interference. The single carrier framework offers excellent immunity against out of band emission through use of the variable root raised cosine filter. The multicarrier scheme inherently delivers low spectrum spillage.
7	Robustness to Channel Impairments	Turbo Product Codes and interleaving techniques mentioned in this document provide an excellent robustness to other channel impairments such as rain fade, muti-path, and obviously additive white Gaussian noise. Results presented in this document illustrate the large performance gains over other suggested coding techniques. The inclusion of time guards in the framework provides a good quantity of immunity from selective fading caused by multipath.
8	Robustness to radio Impairments	With the data rates suggested in this proposal, techniques such as digital IQ demodulation mitigate many classic radio impairments. Channel estimation is another technique that combats radio impairments. Many of these system impairments may be modeled as an implementation loss which strengthens the need for the strong coding capability of TPCs.
9	Support of advanced antenna techniques	Section 5 of this proposal describes the ability of this proposal to utilize advanced antenna techniques including smart antennas. The use of such techniques provides for improved system robustness but with the tradeoff of increased system cost and installation complexity. The use of TPC coding has the potential of enhancing the performance of advanced antenna technology, thereby allowing a further system trade-off with which to improve the cost effectiveness of the system.
10	Compatibility with existing relevant standards and regulations	The basis for this proposal utilizes key aspects of 802.11a and 802.16.1. Every effort has been made to ensure that the most relevant qualities from these proposals are brought forward to form this proposal

Table 12Criteria Qualifying Proposal

Statement on Intellectual Property Rights:

All the authors of this proposal have read this document and the IEEE patent policy and agree to abide by its terms.

7 References

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[9] IEEE 802.16.1p-00/07r2, Draft Physical Layer Specification for the 802.16.1 “Air, Interface Standard”

[10] IEEE 802.16.1 pc-00/35, “Turbo Product Code FEC Contribution”, 2000-06-14.