Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**TPC/TCC Complexity Comparison (Latency, Data Rate, Size)**
Date Submitted	**2002-07-09**
Source(s)	Jim Simkins Xilinx 4505 Wasatch Blvd, Suite 205 Salt Lake City, Utah 84124 Voice: 801.424.2477 Fax: 801.424.0191 Email:James.Simkins@Xilinx.com
Re:	C802.16a-02/59
Abstract	Demonstrate the advantage of TPC low latency and high data rates
Purpose	Provide background information on optional coding standard.
Notice	This document has been prepared to assist IEEE 802.16. It is offered as a basis for discussion and is not binding on the contributing individual(s) or organization(s). The material in this document is subject to change in form and content after further study. The contributor(s) reserve(s) the right to add, amend or withdraw material contained herein.
Release	The contributor grants a free, irrevocable license to the IEEE to incorporate material contained in this contribution, and any modifications thereof, in the creation of an IEEE Standards publication; to copyright in the IEEE's name any IEEE Standards publication even though it may include portions of this contribution; and at the IEEE's sole discretion to permit others to reproduce in whole or in part the resulting IEEE Standards publication. The contributor also acknowledges and accepts that this contribution may be made public by IEEE 802.16.
Patent Policy and Procedures	The contributor is familiar with the IEEE 802.16 Patent Policy and Procedures (Version 1.0) <http://ieee802.org/16/ipr/patents/policy.html>, including the statement "IEEE standards may include the known use of patent(s), including patent applications, if there is technical justification in the opinion of the standards-developing committee and provided the IEEE receives assurance from the patent holder that it will license applicants under reasonable terms and conditions for the purpose of implementing the standard." Early disclosure to the Working Group of patent information that might be relevant to the standard is essential to reduce the possibility for delays in the development process and increase the likelihood that the draft publication will be approved for publication. Please notify the Chair <mailto:r.b.marks@ieee.org> as early as possible, in written or electronic form, of any patents (granted or under application) that may cover technology that is under consideration by or has been approved by IEEE 802.16. The Chair will disclose this notification via the IEEE 802.16 web site <http://ieee802.org/16/ipr/patents/notices>.

TPC/TCC Complexity Comparison

Jim Simkins
Xilinx

Introduction

Since existing DVB-RCS cores have latencies far exceeding 10microseconds, a question exists as to whether a DVB-RCS decoder can meet this latency and what is the corresponding increase in complexity. A block-decode time of less than 10microsecond is required to meet latency of an OFDM symbol (QPSK, Rate1/2, 192/384 block size) in a 20MHz channel. Included is a survey of FPGA turbo FEC cores.

Latency and Data Rate

An advantage of the TPC architecture is that the number of SISO (Soft-Input Soft-Output) units can be increased or decreased depending on required latency and data rates. With the constituent codes given in P802.16a/D4, Table 234, the number of SISOs could be increased to eight if another factor of two in latency reduction is desired. The (8,7) code limits the number of parallel SISOs to eight, which is the number of columns processed in parallel. The number of SISOs could be reduced by a factor of 2 or 4 if the channel bandwidth is narrow and decoding latency can be increased by a factor of 2 or 4 respectively.

Latency and data rate for two TPC cores and two DVB-RCS cores are listed in Table 1, given four iterations. The DVB-RCS cores don't support the 802.16a block sizes, but it is assumed the DVB-RCS cores can be modified slightly to support 802.16a block sizes.

Modulation	Data/Coded Data(Bytes)	Rate	TPC "A" Latency/Mbps	TPC "B" Latency/Mbps	DVB_RCS "C" Latency/Mbps	DVB_RCS "D" Latency/Mbps
QPSK	24/48	1/2	3.7us/51Mbps	13.2us/14.5Mbps	17.1us/11.3Mbps	45.9us/4.2Mbps
QSPK	36/48	3/4	4.1us/71Mbps	TBD	23.6us/12.3Mbps	50.7us/5.7Mbps
16 QAM	58/96	3/5	5.7us/82Mbps	21.8us/21.3Mbps	35.2us/13.2Mbps	59.5us/7.8Mbps
16 QAM	77/96	4/5	5.9us/105Mbps	TBD	45.3us/13.4Mbps	67.1us/9.2Mbps
64 QAM	92/144	2/3	9.5us/78Mbps	TBD	53.3us/13.8Mbps	73.1us/10.1Mbps
64 QAM	120/144	5/6	9.5us/101Mbps	TBD	68us/14.1Mbps	84.3us/11.4Mbps

Table 1: Latency and Date Rate Comparison

Size

Table 2 lists the sizes of various FPGA cores. For narrow bandwidth channels that don't have stringent latency requirements, a single SISO (factor of four lower data rate) TPC core is very cost effective. TPC "A" memory utilization for larger 2k TPC blocks is 45Kbit; small 512 TPC blocks scale down to 11.25Kbits, including I/O double buffering. Since a K=7 Viterbi decoder requires roughly 24Kbits of memory for Trellis storage, the standard coding method and optional TPC method have similar memory utilization. Actual size of a DVB-RCS core that meets 10microsecond latency is unknown at this time.

	RS/Viterbi	TPC "A" SISOx4	TPC "B" 4xRate	TPC "A" SISOx1	TPC "B" 1xRate	DVB_RCS " C "	DVB_RCS " D "
Slices	3862	3260	3349	1000	1041	3333	2357
BlockRAM	6	13(45Kbit)	14	7(45Kbit)	6	8	9
Freq(MHz)	60/150	150	108	150	116	75	80

Table 2: Comparison of Core Sizes

Complexity

DVB-RCS decoders vary from 4.6 to 8 times more complex than TPC decoders, even if latency is not an issue. The question exists as to how complex a low latency DVB-RCS solution really is. The DVB-RCS "C" decoder architecture has a data rate advantage over the DVB-RCS "D" decoder for small 48 byte packets; but for larger 96 byte packets the overall complexity is roughly the same when comparing size, data rate, and latency. This illustrates variations possible with different DVB-RCS architectures.

Given the latency advantage of TPC "A" decoder, it is possible to process more iterations (6 or 8) with a TPC solution and still meet 10microsecond latency. This tradeoff improves TPC BER by 0.2dB. The TPC "A" SISOx4 core is very competitive with RSV standard coding size. For moderate latency applications, the TPC "A" SISOx1 core is roughly 3.8 smaller than RSV.

Summary

The TPC "A" core is an example of a low-complexity Turbo core which is usable in high data-rate 802.16, or low-latency 802.16a. The question of low latency TCC complexity is still unanswered. Second-generation TPC cores are possible, which will further improve BER for low code rates and small block sizes at the expense of more complexity.