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Title	Preamble sequence for supporting scalable FFT	
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Re:		
Abstract	Preamble sequences for FFT size other than 2048-FFT	
Purpose	Adopting of proposed method into P802.16e	
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Preamble sequence for supporting scalable FFT

Problem Definition and Proposed Solutions

In IEEE 802.16e/D3, section 8.4.6.1.1 describes the preamble for scalable FFT as “For FFT size other than 2048-FFT, only the first k elements of table 307 shall used to modulate the DL preamble subcarriers, where k is the number of carriers.” However, the truncated preamble sequence from that of 2048-FFT may result in high PAPR (peak to average power ratio). We propose new preamble sequences for 128-FFT, 512-FFT, and 1024-FFT in this contribution, which have low PAPRs.

Suggested change to the standard

In ‘8.4.6.1.1 Preamble’

[CHANGE the sentence]

“For FFT size other than 2048-FFT, ~~only the first k elements of table 307 shall be used to modulate the DL preamble sub-carriers, where k is the number of carriers~~ use the following preamble sequences corresponding to the FFT size”

[ADD the following text]

For the FFT size of 128-FFT, the preamble sequences can generated using the shift register structure in figure aaa where the initial state value are defined in table xxx. The first k elements of output sequence are used for a preamble, where k is the number of carriers.

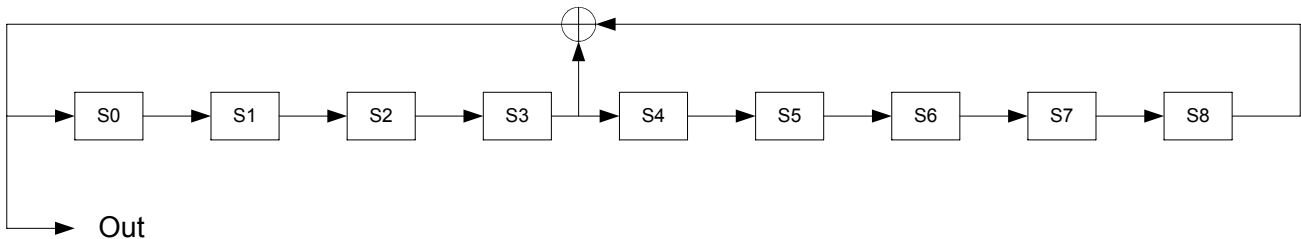


Figure aaa – Preamble sequence generator for 128-FFT

Table xxx – Initial values of preamble sequence generator for 128-FFT

Index	S0 S1 S2 S3 S4 S5 S6 S7 S8	Index	S0 S1 S2 S3 S4 S5 S6 S7 S8	Index	S0 S1 S2 S3 S4 S5 S6 S7 S8
0	1 1 1 0 1 1 0 1 0	38	1 1 0 1 0 1 0 1 1	76	1 1 0 0 0 1 1 0 1
1	0 1 1 0 0 1 0 1 1	39	1 0 1 0 1 1 0 0 1	77	1 0 1 1 1 0 1 0 1
2	1 1 0 0 1 1 0 1 1	40	1 0 1 0 0 0 0 1 1	78	1 0 1 0 0 1 0 0 1
3	0 1 0 1 1 0 0 1 0	41	1 1 0 1 0 1 1 1 1	79	0 0 0 1 1 0 0 1 1
4	0 0 0 1 0 0 1 0 0	42	1 1 1 1 1 0 1 1 0	80	0 1 0 0 0 0 1 0 1
5	1 0 0 1 1 1 0 1 0	43	0 1 1 0 1 0 1 1 1	81	0 0 1 1 0 0 1 1 1
6	1 0 1 1 0 1 0 0 0	44	0 1 1 0 1 1 0 0 1	82	1 1 0 0 0 1 0 0 0
7	0 1 1 1 0 1 1 0 1	45	0 0 1 1 0 1 1 0 0	83	1 1 1 0 0 1 0 0 0
8	0 1 0 0 1 0 1 1 0	46	1 0 1 0 0 1 1 1 0	84	0 0 1 0 1 1 0 1 1
9	1 0 0 1 1 0 1 0 0	47	0 1 1 1 0 1 0 0 1	85	0 1 1 1 1 1 1 0 0
10	0 1 0 0 0 0 0 0 1	48	1 1 1 0 0 0 0 0 1	86	0 1 0 1 0 0 1 1 1

11	101100000	49	111010111	87	101011010
12	000011101	50	010101110	88	101010001
13	110110100	51	011010001	89	011101111
14	100001111	52	010010010	90	110101100
15	010011101	53	100000101	91	110101000
16	001110110	54	101000010	92	001001011
17	110000010	55	110110011	93	000011001
18	110011101	56	011011000	94	001011000
19	010010011	57	110110000	95	000100010
20	011000001	58	101110010	96	001110011
21	111101011	59	101100011	97	100001010
22	000011000	60	100010110	98	000110110
23	000001011	61	010111000	99	001101000
24	001001000	62	101100101	100	100111110
25	110100001	63	110110010	101	110011111
26	001111111	64	111111011	102	011111101
27	001110100	65	001001001	103	001111100
28	100100100	66	010101101	104	110010010
29	100000010	67	111000011	105	101011111
30	010100001	68	111001101	106	110100010
31	011100100	69	000111100	107	101100111
32	101110001	70	000111001	108	001110111
33	100101101	71	100100101	109	101010111
34	110100100	72	011111111	110	110010110
35	100110110	73	110101110	111	111011110
36	100001100	74	110010001	112	101000000
37	111010110	75	110011010	113	010001010

For the FFT size of 512-FFT, the preamble sequences are generated using the shift register structure in figure bbb where the initial state value are defined in table yyy. The first k elements of output sequence are used for a preamble, where k is the number of carriers.

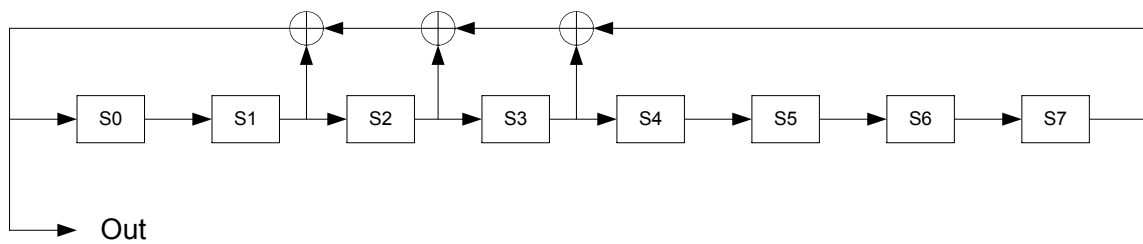


Figure bbb – Preamble sequence generator for 512-FFT

Table yyy – Initial values of preamble sequence generator for 512-FFT

Index	S0 S1 S2 S3 S4 S5 S6 S7	Index	S0 S1 S2 S3 S4 S5 S6 S7	Index	S0 S1 S2 S3 S4 S5 S6 S7
0	00100000	38	00001011	76	01111011
1	10101101	39	11111011	77	00101001
2	01000001	40	00010111	78	11000010
3	00111101	41	11101100	79	01000101
4	11101111	42	11100011	80	01110101
5	01011011	43	11000111	81	00001010

6	01101101	44	11100111	82	11000011
7	10010000	45	10011100	83	11101011
8	10000101	46	11001110	84	11110111
9	10001101	47	11000110	85	11101000
10	10110110	48	00011010	86	01000000
11	01111110	49	10110010	87	00110100
12	00000101	50	00011101	88	00000100
13	10000010	51	00111110	89	11110101
14	11110001	52	11010001	90	01000011
15	11011010	53	01010110	91	10111010
16	01011101	54	00011001	92	00101111
17	10011110	55	11110000	93	10011000
18	10100100	56	00111010	94	00101110
19	00011111	57	01010100	95	10101010
20	11011111	58	11011011	96	00110101
21	01001000	59	10001000	97	11100101
22	10100111	60	10100000	98	00111011
23	10010001	61	11001100	99	01110110
24	11001000	62	00010110	100	10000000
25	01100111	63	11100110	101	00111000
26	10101110	64	01010011	102	00001000
27	10111111	65	10011101	103	00001100
28	01111101	66	10000111	104	00110001
29	11110110	67	01101010	105	10001110
30	01110100	68	11110010	106	11001101
31	00000111	69	10110011	107	11101101
32	01011100	70	00101101	108	11001111
33	01110000	71	11100001	109	00000001
34	00101011	72	10110001	110	11101110
35	00001111	73	11010100	111	10110101
36	00001110	74	11100100	112	10100010
37	11010111	75	00111001	113	11111101

For the FFT size of 1024-FFT, the preamble sequences are generated using the shift register structure in figure ccc where the initial state value are defined in table zzz. The first k elements of output sequence are used for a preamble, where k is the number of carriers.

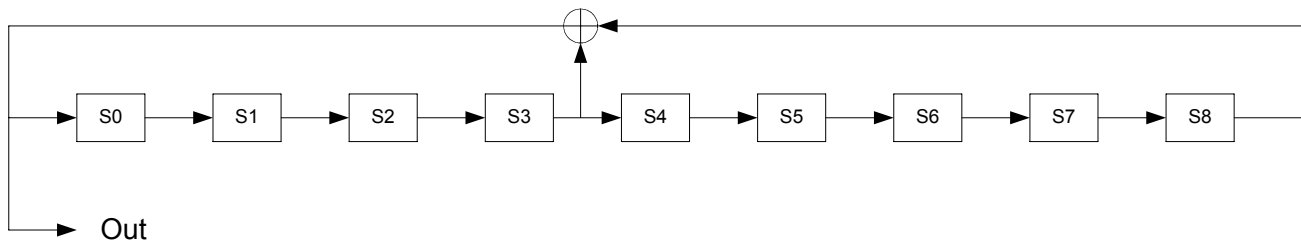


Figure ccc – Preamble sequence generator for 1024-FFT

Table zzz – Initial values of preamble sequence generator for 1024-FFT

Index	S0 S1 S2 S3 S4 S5 S6 S7 S8	Index	S0 S1 S2 S3 S4 S5 S6 S7 S8	Index	S0 S1 S2 S3 S4 S5 S6 S7 S8
0	010111110	38	011110110	76	100111011

1	111010101	39	110101110	77	110110110
2	101101011	40	010110001	78	100100101
3	111101010	41	011101010	79	010001011
4	011010111	42	010010111	80	111101001
5	111110101	43	111001000	81	010000110
6	000010110	44	010111010	82	010111100
7	000101101	45	001111110	83	000000111
8	101010101	46	110100110	84	111101011
9	110101010	47	000000110	85	001001101
10	101011111	48	100110000	86	100001000
11	011111010	49	010111011	87	110001000
12	011010011	50	111111010	88	011011011
13	001011010	51	001100000	89	011101101
14	101110111	52	001110110	90	111000000
15	110000000	53	011111100	91	100111101
16	100000001	54	110110000	92	101000101
17	010011011	55	011101100	93	000001001
18	111011000	56	011100100	94	001010000
19	111011100	57	000001110	95	101001011
20	111111101	58	001100010	96	000011101
21	101111101	59	100001100	97	010011101
22	110101111	60	001001000	98	011110100
23	111110100	61	011011111	99	010011110
24	111011011	62	101111111	100	101010110
25	110111111	63	010101010	101	111110111
26	000000011	64	100101100	102	110100000
27	010110101	65	011000001	103	101100011
28	101010100	66	000001011	104	011000000
29	101110101	67	101101100	105	010101000
30	110100010	68	010101111	106	110011000
31	101101110	69	010100000	107	100000101
32	101101001	70	010010110	108	111111001
33	010100010	71	110000010	109	011011010
34	101001101	72	001110111	110	010011010
35	011101110	73	100101101	111	001101101
36	110100111	74	000111011	112	101001110
37	111101000	75	111000101	113	101011110

References

- [1] IEEE P802.16-REVd/D5-2004 Draft IEEE Standards for local and metropolitan area networks part 16: Air interface for fixed broadband wireless access systems.
- [2] IEEE P802.16-REVe/D3-2004 Amendment for Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Band.