Project	**IEEE 802.16 Broadband Wireless Access Working Group <http://ieee802.org/16>**
Title	**Hybrid ARQ buffer issues**
Date Submitted	**2008-07-07**
Source(s)	[1] Zheng Yan-Xiu, Ren-Jr Chen, Chang-Lan Tsai, Chung-Lien Ho, [2]Richard Li, ITRI Wern-Ho Sheen, NCTU/ITRI Voice: [1]+886-3-5914715 [2]+886-3-5917596 E-mail: [1]zhengyanxiu@itri.org.tw [2]richard929@itri.org.tw *<http://standards.ieee.org/faqs/affiliationFAQ.html>
Re:	Call for Comments and Contributions on Project 802.16m System Description Document (SDD) issued on 2008-06-16 (IEEE 802.16m-08/024) Topic: Hybrid ARQ (PHY Aspects)
Abstract	This contribution describes H-ARQ buffer issue. A new mechanism is necessary to reduce H-ARQ buffer. New channel coding scheme might be also necessary to reduce packet error rate.
Purpose	For discussion and approval by IEEE 802.16m TG
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Hybrid ARQ Buffer Issues

Zheng Yan-Xiu, Ren-Jr Chen, Chang-Lan Tsai, Chung-Lien Ho, Richard Li
ITRI

Wern-Ho Sheen,
NCTU/ITRI

1 Introduction

This contribution provides a formula to calculate the necessary buffer for H-ARQ mechanism corresponding to various system throughputs. Comparing with existing 3GPP LTE QPP turbo code [1] and IEEE 802.16e CTC [2], the necessary buffer is impressive. However the buffer is not necessary. A mechanism is necessary to accommodate this situation.

2 HARQ buffer formula

Fig. 1 illustrates H-ARQ communication system. The system will stores the received transmission redundant bits if the decoded bits do not pass CRC verification. Since the receiver has to allocate a buffer for H-ARQ mechanism, the case that no packet passes CRC verification would be generally considered to avoid packet discarding. Therefore the necessary buffer would increase with system throughput S_{Mbps}. The buffer is also linear to round trip delay T_{ms}. Since the H-ARQ mechanism stores coded samples, higher code rate R_c leads less storage. Higher modulation order M also reduces memory storage if symbol level storage is considered. Therefore we have a formula to describe the relationship between buffer size and system throughput.

$$B_{Kbits} = \frac{S_{Mbps} \cdot T_{ms}}{R_c \cdot M} [\text{Soft Bits}] \quad (1)$$

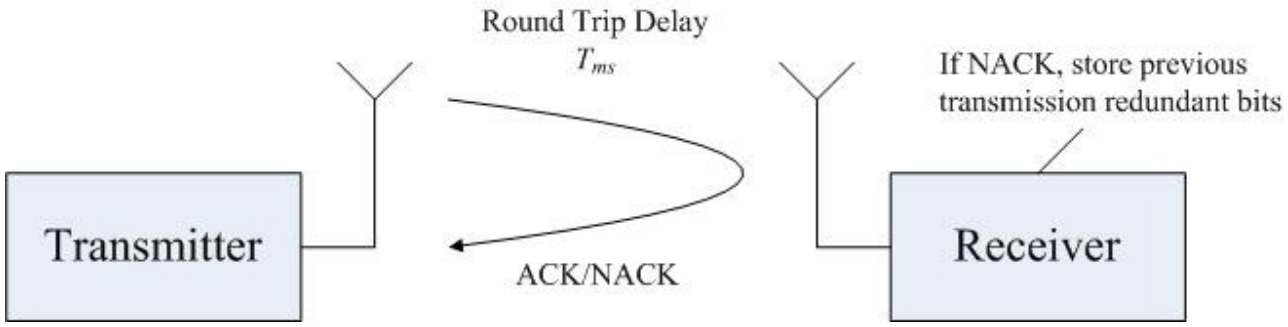

Fig. 1: H-ARQ communication system.

Given this formula, Table 1 shows examples for the necessary buffer. Comparing with 3GPP LTE QPP turbo code [1], the decoder only requires around 30.720 soft bits for received samples and extrinsic information. Comparing with the WiMAX reference system [3], the decoder only requires 2.880 soft bits for received samples and extrinsic information. Comparing with H-ARQ buffer, all algorithm are low complexity under the mentioned throughput.

Table 1: Throughput calculation corresponding to various system throughput.

	S_{Mbps}=100Mbps T_{ms}=5ms	S_{Mbps}=1000Mbps T_{ms}=5ms
Rc=1/2, M=1 (Bit level buffer)	1000K [Soft Bits]	10M [Soft Bits]
Rc=4/5, M=1 (Bit level buffer)	625K [Soft Bits]	6.25M [Soft Bits]
Rc=1/2, M=1 (QPSK) (Symbol level buffer for one retransmission)	1000K [Soft Bits]	10M [Soft Bits]
Rc=1/2, M=2 (16QAM) (Symbol level buffer for one retransmission)	500K [Soft Bits]	5M [Soft Bits]
Rc=1/2, M=3 (64QAM) (Symbol level buffer for one retransmission)	334K [Soft Bits]	3.34M [Soft Bits]

3 Conclusions

H-ARQ requires a mechanism to reduce hybrid ARQ buffer without performance degradation.

H-ARQ requires a new coding scheme to avoid hybrid ARQ buffer with less packet error rate.

References

[1] 3GPP TS 36.212 v.8.2.0, “Multiplexing and Channel Coding,” March, 2008.
[2] IEEE DRAFT P802.16, "Part 16: Air interface for fixed broadband wireless access systems," March, 2007.
[3] WiMAX Forum™ Mobile System Profile Release 1.0 Approved Specification, WiMAX, Certification Working Group, April 2007.

========== TEXT Proposal ==========

H-ARQ requires a mechanism to reduce hybrid ARQ buffer without performance degradation.

H-ARQ requires a new coding scheme to avoid hybrid ARQ buffer with less packet error rate.