Proposal for IEEE 802.16m Hybrid ARQ and FEC

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Venue:

IEEE 802.16m-08/024, “Call for Comments and Contributions on Project 802.16m System Description Document (SDD)”,

On topic of “Hybrid ARQ (PHY aspects)”

Base Contribution:

None

Purpose:

To be discussed and adopted by TGm for use in 802.16m SDD

Notice:

Release:

Patent Policy:

Proposal for IEEE 802.16m Hybrid ARQ and FEC

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About This Contribution

- Goal and scope of this contribution
  - Propose requirements on the PHY aspects of Hybrid ARQ for 802.16m
- Issue to be addressed in this contribution
  - Mother code rate for 802.16m
  - Procedure for FEC and Hybrid ARQ
  - FEC
    - Convolutional Codes (CC)
    - Convolutional Turbo Codes (CTC)
    - Low-Density Parity-Check (LDPC) Codes

Mother code rate for 802.16m

- The proposed mother code rate for 802.16m is lower than or equal to 1/3
  - CTC, CC: 1/3
  - LDPC: 1/5
- Code rate lower than mother code rate should be supported by repetition coding.

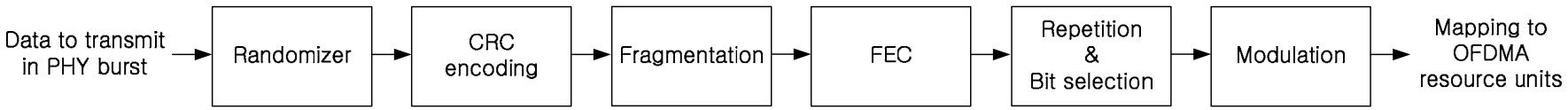
IR type Hybrid ARQ

- Incremental redundancy shall be a mandatory hybrid ARQ operation for 802.16m.
  - Chase combining is a special case of IR HARQ.
  - Non-HARQ is a special case of IR HARQ.
- Constellation Re-arrangement shall be used.
  - For high order modulation, re-transmission of bits using constellation re-arrangement shows more performance gain.

Procedure for FEC and HARQ

- Proposed requirements for 16m
  - Need to determine the maximum size for the encoder input which reflect s channel coding schemes.
  - Need to change the concatenation rules of 16e to increase coding gain.
    - The encoding packet size after fragmentation should be same or two consecutive bytes.
    - Simple and efficient fragmentation rule taking account of a multiple of 7 as an encoder input size.
  - Need to operate without signaling overhead for HARQ.

- Proposed procedure for FEC and HARQ



Convolutional codes (CC)

- The mother code rate needs to be lower than 1/2
  - Some control channel should be transmitted using lower code rate.
  - When concatenated by repetition code, 1/3 is better than 1/2.
  - Constraint length 9, Rate 1/3 CC is proposed
- CC will not support IR type Hybrid ARQ

Convolutional Turbo Codes (CTC)

- CTC should support variable code lengths and rates by rate matching
  - Rate matching is accomplished by padding, deleting, and bit selection
- Finer granularity of block size
  - Efficient utilization of limited resources
  - Inner interleavers with various sizes are required
  - No exceptional fragmentation rule when the size of encoder input is multiple of 7.

LDPC Codes

- Problem of 16e LDPC Code
  - Can not support IR type Hybrid ARQ
  - Inconsistent with other parts of 16e specification.
- Requirements for 16m LDPC Code
  - LDPC code for 16m should be rate-compatible.
  - Support IR type Hybrid ARQ using a small number of parity-check matrices
    - The number of matrices shall be at most 12.
    - 8 matrices are preferred
  - Support various information & codeword lengths
    - Flexible shortening & puncturing should be supported
  - The lowest code rate should be lower than 1/3
    - Rate 1/5 is proposed

LDPC Codes

- Structured LDPC codes are proposed as used in 16e.
  - Flexible support to variable code length by lifting
  - Simple implementation complexity
  - Easy adjustment of parallelization, e.g. full parallel, partial parallel

- Structured LDPC codes
  - Consist of a number of the element matrices.
  - Support code length flexibility from adjusting a size of the element matrix.
  - The element matrix is a circular shift of identity matrix or all-zero matrix
  - Have the special form for the fast encoding.

LDPC Codes

- MET (Multi-Edge Type) LDPC codes are proposed.
  - Good performances with lower degrees comparing with irregular LDPC codes
  - Lower complexity in terms of memory

- MET LDPC codes
  - A generalization of irregular LDPC codes
  - Consist of various variable nodes with multi-edge types.
    - Information nodes : state variable nodes with puncturing, and variable nodes without puncturing
    - Parity nodes contain degree 1 variable nodes

Text Proposal to 802.16m SDD

Insert the following text into Physical Layer clause (Chapter 11 in [IEEE 802.16m-08/003r3])

11.x FEC and Hybrid ARQ

11.x.1 Procedure

The procedure for FEC and Hybrid ARQ is shown in figure xxx.

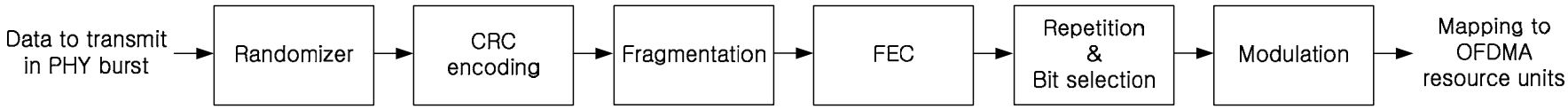


Figure xxx. Procedure for FEC and Hybrid ARQ

11.x.2 Hybrid ARQ

Incremental redundancy shall be a hybrid ARQ operation for 802.16m . Chase combining HARQ and Non-HARQ are special cases of IR HARQ.

11.x.3 FEC

11.x.3.1 Convolutional Codes (CC)

A Rate 1/3 CC shall be used. CC shall not support IR type Hybrid ARQ .

Text Proposal to 802.16m SDD (cont’)

11.x.3.2 Convolutional Turbo Codes (CTC)

CTC should support finer granularity of block size than 802.16e. CTC should support variable code lengths and rates by rate matching .

11.x.3.3 Low-Density Parity-Check (LDPC) Codes

The LDPC codes shall be multi-edge type structured LDPC codes. IR type HARQ shall be supported by at most 12 parity-check matrices. Variable information and codeword sizes shall be supported by shortening and puncturing. The lowest code rate of parity-check matrices is 1/5.

11.x.3.4 Repetition

Code rate lower than mother code rate shall be supported by repetition coding.