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Title	Corrections in the Implementation of C80216m-09/2532r1 on Four Sector Deployments (Sections 16.3.5 and 16.3.8)		
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Re:	Category: P802.16m/D3 comments for LB30b Area: Sections 16.3.5 (DL PHY Structure) and 16.3.8 (UL PHY Structure)		
Abstract	Errors were made during the implementation of contribution C80216m-09/2532r1, which was accepted at Session #64 in Atlanta, GA. This contribution proposes to correct the errors so that the text is as proposed in the previously accepted contribution.		
Purpose	Discuss and adopt		
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Corrections in the Implementation of C80216m-09/2532r1 on Four Sector Deployments (Sections 16.3.5 and 16.3.8)

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1. Introduction

Contribution C80216m-09/2532r1 proposed changes to the DL and UL PHY structure to better support four sector deployments. The contribution was accepted at Session #64 in Atlanta, GA but was implemented with errors. This contribution proposes changes which correct the errors made in implementing the previously accepted contribution.

2. Proposed Text Changes

DFPC	Freq. Partitioning (FP ₀ :FP ₁ :FP ₂ :FP ₃)	FPCT	FPS ₀	FPS _{<i>i</i>} (<i>i</i> >0)
0	1:0:0:0	1	N _{PRU}	0
1	0:1:1:1	3	0	N _{PRU} * 1/3
2	1:1:1:1	4	N _{PRU} * 1/4	N _{PRU} * 1/4
3	3:1:1:1	4	N _{PRU} * 1/2	N _{PRU} * 1/6
4	9:5:5:5	4	N _{PRU} * 3/8	N _{PRU} * 5/24
<u>5</u>	<u>0:1:1:0</u>	<u>2</u>	<u>0</u>	$\frac{N_{PRU} * 1/2 \text{ for } i = 1, 2}{0 \text{ for } i = 3}$
<u>6</u>	<u>1:1:1:0</u>	<u>3</u>	<u>N_{PRU} * 1/3</u>	$\frac{N_{PRU} * 1/3 \text{ for } i = 1, 2}{0 \text{ for } i = 3}$
<mark>5</mark> _7	Reserved			

[Modify Table 781 (5 MHz bandwidth) on page 325 as follows:]

[Modify the second line (to the right of the equals sign) in Equation 185 on p. 325 as follows:]

DFPSC i>0, FPCT = 4, or DFPC = 1

[Modify the last two lines (to the right of the equals sign) in Equation 185 on p. 325 as follows:]

 $K_{SBF}/2$ i = 1, 2, FPCT = 2 K_{SBF} i = 0, FPCT = 1

[Modify lines 62-65 on p. 328 and lines 1-2 on p. 329 as follows (2 changes):]

When FPCT = 2, $DCAS_{SB,i}$ and $DCAS_{MB,i}$ for i=1 and 2 are signaled using the $DCAS_{SB,0}$ and $DCAS_{MB,0}$ fields in the SFH. Since FP₀ and FP₃ are empty, $L_{SB-CRU,FP0} = L_{MB-CRU,FP0} = L_{DRU,FP0} = 0$ and $L_{SB-CRU,FP3} = L_{MB-CRU,FP3} = 0$. For i=1 and 2, $L_{SB-CRU,FPi} = N_1 * DCAS_{SB,0}$ and $L_{MB-CRU,FPi}$ is obtained using the mappings in Table 782 through Table 784 for system bandwidths of 20 MHz, 10 MHz and 5 MHz, respectively.

UFPC	Freq. Partitioning (FP ₀ :FP ₁ :FP ₂ :FP ₃)	FPCT	FPS _{<i>i</i>} (<i>i</i> =0)	FPS _{<i>i</i>} (<i>i</i> >0)
0	1:0:0:0	1	N _{PRU}	0
1	0:1:1:1	3	0	N _{PRU} * 1/3
2	1:1:1:1	4	N _{PRU} * 1/4	N _{PRU} * 1/4
3	3:1:1:1	4	N _{PRU} * 1/2	N _{PRU} * 1/6
4	9:5:5:5	4	N _{PRU} * 3/8	N _{PRU} * 5/24
<u>5</u>	<u>0:1:1:0</u>	<u>2</u>	<u>0</u>	$\frac{N_{PRU} * 1/2 \text{ for } i = 1, 2}{0 \text{ for } i = 3}$
<u>6</u>	<u>1:1:1:0</u>	<u>3</u>	<u>N_{PRU} * 1/3</u>	$\frac{N_{PRU} * 1/3 \text{ for } i = 1, 2}{0 \text{ for } i = 3}$
4 –7	Reserved			

[Modify Table 874 (5 MHz bandwidth) on page 499 as follows:]

[Modify the options (i.e., to the right of the large brace) in Equation 237 on p. 499 as follows:]

$K_{SB} - (FPCT - 1) \cdot \mathbf{D} UFPSC$	i = 0, FPCT = 4
D UFPSC	i > 0, $FPCT = 4$, or $UFPC = 1$
$K_{SB} - (FPCT - 1) \cdot UFPSC$	$i = 0, FPCT = 3, UFPC \neq 1$
UFPSC	$i = 1, 2, FPCT = 3, UFPC \neq 1$
<i>K</i> _{SB<i>F</i>} /2	i = 1, 2, FPCT = 2
K _{SBF}	i = 0, FPCT = 1

[Modify lines 62-65 on p. 328 and lines 1-2 on p. 329 as follows:]

When FPCT = 2, $\mathcal{PU}_{CAS_{SB,i}}$ and $\mathcal{PU}_{CAS_{MB,i}}$ for i=1 and 2 are signaled using the $\mathcal{PU}_{CAS_{SB,0}}$ and $\mathcal{PU}_{CAS_{MB,0}}$ fields in the SFH. Since FP₀ and FP₃ are empty, $L_{SB-CRU,FP0} = L_{MB-CRU,FP0} = L_{DRU,FP0} = 0$ and $L_{SB-CRU,FP3} = L_{MB-CRU,FP3} = L_{DRU,FP3} = 0$. For i=1 and 2, $L_{SB-CRU,FPi} = N_1 * \mathcal{PU}_{CAS_{SB,0}}$ and $L_{MB-CRU,FPi}$ is obtained using the mappings in Table 8705 through Table 8747 for system bandwidths of 20 MHz, 10 MHz and 5 MHz, respectively.