**Turbo Product Code Tutorial**

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Purpose:
- Provide information on the state of TPC technology

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Turbo Product Code Tutorial

May 1 2000

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Agenda

- Forward Error Correction Tutorial
- Turbo Product Codes
- Galaxy Simulation SW demonstration
- Open Discussion
- Summary and Conclusions
Forward Error Correction
Typical System Design Goals

- Maximize data rate
- Maximize data reliability
- Minimize required transmission energy
- Minimize required bandwidth
- Minimize system complexity (cost)

Forward Error Correction can be instrumental in helping meet these goals!
Definitions

- **Forward Error Correction Coding**
  - The addition of redundancy to a message through encoding prior to transmission

- **Code Rate**
  - Ratio of data bits / total bits transmitted

- **Shannon Channel Capacity**
  - Theoretical bound for channel capacity for a given modulation and code rate
The minimum distance or “Dmin” of an error correction code characterizes the codes strength.

The error correcting capability, “t”, of a code is defined as the maximum number of guaranteed correctable errors per codeword:

\[ t = \left\lfloor \frac{D_{\text{min}} - 1}{2} \right\rfloor \]
Shannon Capacity vs. Code Rate

Shannon Limit versus Code Rate

<table>
<thead>
<tr>
<th>Bit Error Rate, P(e)</th>
<th>Code Rate ~0.0</th>
<th>Code Rate 0.5</th>
<th>Code Rate 0.8</th>
</tr>
</thead>
</table>

Eb/No (dB)
Error Correction Coding

Format/MAC → ECC Encode → Modulate → RF/Upconversion

Format/MAC → ECC Decode → Demodulate → RF/Down Conversion
Why Use Error Correction?

Designers can choose between levels of improved data reliability, reduced systems costs or increases in range

3 dB of coding gain can:
- reduce the required bandwidth by 50% or
- increase data throughput by a factor of 2 or
- increase range by 40% or
- reduce antenna size by 30% or
- reduce transmitter power by a factor of 2

Bottom line...reduced cost or increased value
Error Correction Codes

- Block Codes
  - Hamming
  - BCH
  - Reed–Solomon
- Convolutional Codes (Viterbi)
- Trellis Codes
- Concatenated
  - Viterbi/Reed–Solomon
- Turbo Convolutional Codes (TCC)
- Turbo Product Codes (TPC)
Hamming Codes

- Linear and systematic
- Specified as \((n,k)\)
  - \(n\) is the encoded number of bits
  - \(k\) is the number of information bits
- Example: \((7,4)\)
  - \(d_1\) \(d_2\) \(d_3\) \(d_4\) \(e_1\) \(e_2\) \(e_3\)
- Easy to both encode and decode
Hamming Codes

- Hamming codes
  - $D_{\text{min}} = 3$
- Extended Hamming codes add a parity bit
  - $D_{\text{min}} = 4$
- TPCs utilize extended Hamming codes and parity codes to construct Product Codes
  - $D_{\text{min}} \gg$ than constituent codes
- Iterative decoding enhances performance
  - Turbo Product Codes
Turbo Product Code History

- Product codes first described by Elias (1954)
- Iterative decoding of product codes described by Tanner (1981), Lin & Costello (1983) and others
- Although described in the literature, commercial implementation had to wait for a cost efficient SISO decoder algorithms
- Efficient SISO algorithms have made commercially viable TPCs possible
- AHA4501 introduced in November 1998
Turbo Product Codes

- Turbo Product Codes (TPCs) are based on block codes, not convolutional codes.
- TPCs are built on a 2 or 3 dimensional arrays of extended Hamming codes.
  - Encoding is done in a single iteration.
  - Minimum distance of a 2-D product code is square of constituent code; for a 3-D code, cubed.
- Thus minimum distance is:
  - 16 for 2-Dimensional codes
  - 64 for 3-Dimensional codes
2D Product Code Example

- **(8,4) x (8,4) Code**
  - Code is systematic
  - D represents input data
  - E represents ECC bits
  - D     D     D     D     D     E     E     E     E
  - D     D     D     D     D     E     E     E     E
  - D     D     D     D     D     E     E     E     E
  - D     D     D     D     D     E     E     E     E
  - E     E     E     E     E     E     E     E     E
  - E     E     E     E     E     E     E     E     E
  - E     E     E     E     E     E     E     E     E
  - E     E     E     E     E     E     E     E     E

- **3D codes follow the same concept, but in three dimensions**
TPCs will work with hard decision or soft decision decoding

- Two bit soft decision decoding typically picks up 2 dB of additional coding gain
- Additional soft bits can add about 1/2 dB more
- Soft decoder input requires a “soft metric”
  - BPSK/QPSK proportional to I/Q voltage
  - Higher order constellations require LLR computation
Soft vs. Hard Decision Decoding

Turbo Product Code Soft Input Bits

(4096,3249) TPC at 6 iterations

Bit Error Rate, $P(e)$

$E_b/N_0$ (dB)

- Uncoded PSK, rate=1
- 3 bit Soft Viterbi/RS, Rate=0.806
- 3 bit Soft Viterbi/RS, Rate=0.790
- Hard Decision TPC, Rate 0.79
- 2 bit Soft TPC
- 3 bit Soft TPC
- 4 bit Soft TPC
Iterative Decoding

Down

1. Family pet
Iterative Decoding

Across

2. Advanced Hardware Architectures

Down

1. Family pet
Iterative Decoding

Down
1. Family pet

Across
2. Advanced Hardware Architectures
3. Cyclical Redundancy Check
TPC Decoding

Each iteration decodes all rows, then all columns.
System Level Tradeoffs

Turbo Product Code System Level Trade-Offs

Eb/No (dB) for BER = 10^-5

Iterations Soft Input Bits

(64,57)x(64,57) Rate 0.793 Code
Burst Error Performance

- Given that extended Hamming codes can only correct a single bit error how well can a TPC handle a burst of errors?
Burst Error Performance

- Product code array is the key!

<table>
<thead>
<tr>
<th>D</th>
<th>D</th>
<th>D</th>
<th>D</th>
<th>D</th>
<th>E</th>
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<tbody>
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</tr>
</tbody>
</table>
Product code array is the key!

```
D  D  D  D  E  E  E  E  E  E
D  D  D  D  E  E  E  E  E  E
D  D  D  D  E  E  E  E  E  E
D  D  D  D  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
E  E  E  E  E  E  E  E  E  E
```
Burst Error Performance

- **Product code array is the key!**

<table>
<thead>
<tr>
<th>E</th>
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</thead>
<tbody>
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</tr>
</tbody>
</table>
Burst Error Performance

- Data scrambling enhances burst error performance
- \((64,57)^2\) code performance (helical scrambling)
  - Tolerates 384 burst errors in each code block
  - This burst represents 9.4% of the bits in the block
  - A 128 bit burst event every block shifts the BER curve by only 1.2 dB
  - AWGN channel model used in addition to burst
Burst Error Performance

- 3D codes provide even more performance
- \((16,11)^3\) code performance (helical scrambling)
  - Handles 1024 burst errors in each code block
  - This burst represents 25% of the bits in the block
  - A 128 bit burst event every block shifts the BER curve by only 0.5 dB
  - For example, BER < \(10^{-6}\) at Eb/No of 2 dB with a 128 bit burst error event every block
Asymptotic Bounds

- Minimum Distance ($d_{\text{min}}$) Determines Slope of Asymptotic Bound
- Number of Codewords at $d_{\text{min}}$ Determine Position of Bound
TCC Distance Structure

- Decreases Number of Codewords at $d_{\text{min}}$
- However, $d_{\text{min}}$ is not High (Especially After Puncturing)
- Can Cause Characteristic ‘Error Floor’
TPC Distance Structure

- Distance Properties of Product Code are Equal to the Product of the Constituent Codes

(32,26)² Product Code
\[ d_{\text{min}} = 16 \]

(16,11)³ Product Code
\[ d_{\text{min}} = 64 \]
Because of high Dmin (typ 16 or greater), there is no error floor for TPCs

Depending on the TPC code used:
- No Flare
- Minor flaring starting @ about $10^{-7}$
  - Flare is < 0.3 dB/decade
  - Minor flaring starting @ about $10^{-12}$

Flare is predictable
- Block size
- Dmin
Turbo Product Codes

Performance Comparison

RSV, TPC, TCC, eTPC
4K Block Size, Rate = 0.8

Bit Error Rate P(e)

Eb/No (dB)
# Competitive Comparisons

<table>
<thead>
<tr>
<th>Attribute</th>
<th>TPC</th>
<th>RS</th>
<th>Viterbi</th>
<th>RS-Viterbi</th>
<th>TCC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Coding Gain</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>@ BER of $10^{3.4}$</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>$10^{6.7}$</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>&lt;10$^{10}$</td>
<td>4-5</td>
<td>3</td>
<td>2</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td><strong>Latency (bits)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>&lt;256</td>
<td>4</td>
<td>2</td>
<td>5</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>1024 – 204</td>
<td>5</td>
<td>3-4</td>
<td>3</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>&gt;4096</td>
<td>5</td>
<td>3</td>
<td>2</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td><strong>Complexity</strong></td>
<td>3</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>1-2</td>
</tr>
<tr>
<td><strong>IP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4-5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td><strong>Code Rate</strong></td>
<td>5</td>
<td>2</td>
<td>4</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>(flex/range)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Max Data Rate</strong></td>
<td>4</td>
<td>5</td>
<td>3</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

5 = best
Why Use TPCs?

- Excellent performance at high code rates, no puncturing required
- Low complexity relative to coding gain
  - Lower cost
  - Lower power consumption
- TPCs offer significant improvement over concatenated Reed–Solomon/Viterbi
- TPCs are available as standard products and as licensable cores
Flexibility

- A single low cost TPC encoder/decoder can support code rates from 1/5 to 19/20
  - No puncturing required
  - Code change on the fly supports changing channel
    - Near zero latency, no “tail biting” required
- Readily adapted to most any constellation
  - See IEE paper (dgw, Nov99)
- Can support any packet size
  - See RAWCON paper (EH, Aug99)
- Available as standard ASICs or licensed cores
  - VHDL or Verilog targeted to any foundry
  - Licenses available to end users and foundries
TPC Constituent Codes

- Constituent Codes can be mixed and matched to achieve desired code characteristics
- Two or three dimensions as desired

<table>
<thead>
<tr>
<th>Extended Hamming Codes</th>
<th>Parity Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td>(128, 120)</td>
<td>(128, 127)</td>
</tr>
<tr>
<td>(64, 57)</td>
<td>(64, 63)</td>
</tr>
<tr>
<td>(32, 26)</td>
<td>(32, 31)</td>
</tr>
<tr>
<td>(16, 11)</td>
<td>(16, 15)</td>
</tr>
<tr>
<td>(8, 4)</td>
<td>(8, 7)</td>
</tr>
<tr>
<td>-</td>
<td>(4, 3)</td>
</tr>
</tbody>
</table>
### Representative Codes

- TPCs can provide a wide range of code rates and block sizes
- Code shortening enhances this flexibility
  - Shorten rows, columns, and/or bits

<table>
<thead>
<tr>
<th>Product Code</th>
<th>Block Size</th>
<th>Code Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>(128,127) x (128,127)</td>
<td>16,383</td>
<td>0.98</td>
</tr>
<tr>
<td>(128,120) x (128,127)</td>
<td>16,383</td>
<td>0.93</td>
</tr>
<tr>
<td>(64,57) x (32,26)</td>
<td>2,048</td>
<td>0.72</td>
</tr>
<tr>
<td>(32,26) x (16,15) x (8,7)</td>
<td>4,096</td>
<td>0.66</td>
</tr>
<tr>
<td>(16,11) x (16,11)</td>
<td>256</td>
<td>0.47</td>
</tr>
<tr>
<td>(16,11) x (16,11) x (16,11)</td>
<td>4,096</td>
<td>0.32</td>
</tr>
</tbody>
</table>
Constellation Mapping

Source Data → TPC Encoder → Shift Reg. → ROM or RAM Lookup Table → IQ Modulator
I/Q Soft Metric Mapping

Demodulator

I
Q

ROM or RAM Lookup Table

4 by n bits

Shift Reg.

TPC Decoder

Receive Data
ATM Performance

Packet Size = 57 Data Bytes

Bit Error Rate vs. Eb/No (dB)

- Uncoded PSK
- Viterbi, R = 0.67
- Viterbi, R = 0.50
- TPC, R = 0.61, Simulation
- TPC, Asymptotic Bound
MPEG Performance

Packet Size = 192 Data Bytes

Bit Error Rate

Eb/No (dB)

Uncoded PSK, rate=1
RS/Viterbi, R=0.74
TPC, R=0.72
TPC, 2 Iterations
eTPC, R=0.707
RS+BC(40,32)
TPC, Asymptotic Bound
eTPC, Asymptotic Bound

mpegs_small
Large Packet Size Plot

Packet Size up to 2800 Byte

Bit Error Rate

Eb/No (dB)

Uncoded PSK, rate=1
RS/Viterbi, R=0.74, 192 Byte
RS/Viterbi, Perfect Interleaving
RS+BC(40,32), Infinite Interleaving
TPC, R=0.73, 1500 Byte
TPC, R=0.68, 2800 Byte
Higher Order Modulation

- Constellation is Square 64-QAM
- TPC
  - \((64,57)^2 = (4096,3249)\)
  - 4.76 Bits/Symbol
- Concatenated Code
  - Ungerboeck 16 State, 2-D TCM
  - \((255,239), t=8\) Reed–Solomon
  - Interleaver Depth of 2
  - 4.69 Bits/Symbol
TPC vs TCM with RS

Turbo Product Code Performance

(64,57) x (64,57) TPC, 64 QAM, AWGN Channel

Bit Error Rate

Eb/No (dB)

10^{-8} 10^{-7} 10^{-6} 10^{-5} 10^{-4} 10^{-3} 10^{-2} 10^{-1} 10^{0}

8 9 10 11 12 13 14 15 16

Uncoded QPSK
TCM/RS, 4.69 Bits/Sym, l=2
TPC, 4.76 Bits/Sym
- Single Chip Turbo Product Code Encoder/Decoder
- No external memory required for encoding or decoding
- Up to 2 dB coding gain over concatenated Reed–Solomon/Viterbi
- Up to 3 dB coding gain over standalone RS
Channel rates for AHA4501 are up to 36 Mbit/sec
- Multiple AHA4501 devices can be run in parallel with a simple multiplexor to achieve any desired speed

Block sizes from 256 bits to 4096 bits

AHA4501 handles all data formatting for 2 or 3 dimensional codes in a single chip
- Half Duplex Encode/Decode
- Helical Encoding On-chip
- Support for external block synchronization
- No external memory required
New TPC Products

- Astro OC–3
  - Supports OC–3 data rates (155 Mbits/s)
  - Block size up to 16K bits
  - Code rates from 1/4 to 0.98
  - ATM packet or user defined formats
  - Parallel data input/output, programmable
  - Supports code changing on the fly
  - Protos: June 2000  Production: September 2000

- Astro LE
  - Low Cost
  - Data rates to 25 Mbits/sec
  - Architectural definition stage
  - Protos: 4th Quarter, 2000
Next Generation TPC Trends

SoC type logic replaces costly FPGA functions resulting in significant cost savings

- Framing and packet synchronization
- Bit and block error rate monitoring
- Soft metric computation logic
- Encoder and decoder on one chip
- Code change on the fly
- Wide range of block size and code rates
Astro OC-3

Applications

High data rate, bandwidth efficient, data reliability.
Anything over 50 Mbits/sec.

- Satellite communications
  - Data and video
  - HDTV
  - Electronic news gathering
- Broadband point-to-point
- Point to multi-point broadband
TPC with 64 QAM

Turbo Product Code Performance

64 QAM, AWGN Channel

- Uncoded 64 QAM
- (64,57)×(64,57), 4.76 Bits/Sym
- (128,120)×(64,57), 5.01 Bits/Sym
- (128,120)×(128,120), 5.27 Bits/Sym
- (128,127)×(128,120), 5.58 Bits/Sym
- (256,247)×(256,247), 5.91 Bits/Sym
- (256,247)×(256,247), 5.99 Bits/Sym

Bit Error Rate, P(e)

Eb/No (dB)

AHA Confidential

64QAM
TPC with 256 QAM

![256 QAM Turbo Product Code Performance Graph](image)
Support Tools

- Evaluation SW
- Hardware demonstration board(s)
  - Generate BER curves
  - Connect to modem for system analysis
  - Connect to BER test equipment
- Application Notes
  - TPC primer
  - Designers guide
  - Code shortening
  - Burst Error performance
- Galaxy Simulation SW
Galaxy Simulation Software

- Windows based simulation software
  - Support for all Galaxy TPC Core codes
  - Supports all AHA TPC ASIC codes
- Evaluation version
  - No cost to qualified customers
- Simulation Toolkit
  - Two versions available
    - C/C++ API
    - Matlab API
  - Enables integration of TPC encoding/decoding with user system and channel modeling
Galaxy Simulation Software
TPC Galaxy Core Generator

- Generates custom TPC cores
- VHDL or Verilog
- Data rates to 1+ Gbit/sec in 0.25 um CMOS
- Code rates from 0.20 to 0.98
- Block sizes from 64 bits to 128 Kbits
- Incorporates next generation eTPC technology
Turbo Product Code Cores

- Deliverables for Galaxy TPC Decoder cores include:
  - C/C++ behavioral model
  - VHDL or Verilog netlist
  - Verification vectors (>95% fault coverage)
  - VHDL or Verilog test bench
  - Bus functional model
- HW performance that matches SW simulations
- Supported with Galaxy Simulation Toolkit
Turbo Product Code Core

TPC Engine

Input Data Storage
Dual Port RAM
(2 x input block size)

Intermediate Storage
Dual Port RAM
(1 x or 2x block size)

Output Data Storage
Dual Port RAM
(2 x block size)

Boundary Scan

JTAG Controller

RESETN

TPC Core

IDATA
IRDY
IACPT
SYNCO
SYNCI
SCAN_IN
SCAN_OUT
SCYNIO
CONFIG

ODATA
ORDY
OACPT
SYNCO

JTAG IN
JTAG OUT
CLK
Conclusions

- TPCs provide a superior, cost effective FEC solution for a wide range of applications
- Available now
- Standard products and licensable cores
- More information and support is available
  - Application Notes
  - Product Brief
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Thank You!

Questions?