PHY Logical Interfaces and Services

IEEE 802 Resilient Packet Rings Study Group
July 11-14, 2000.

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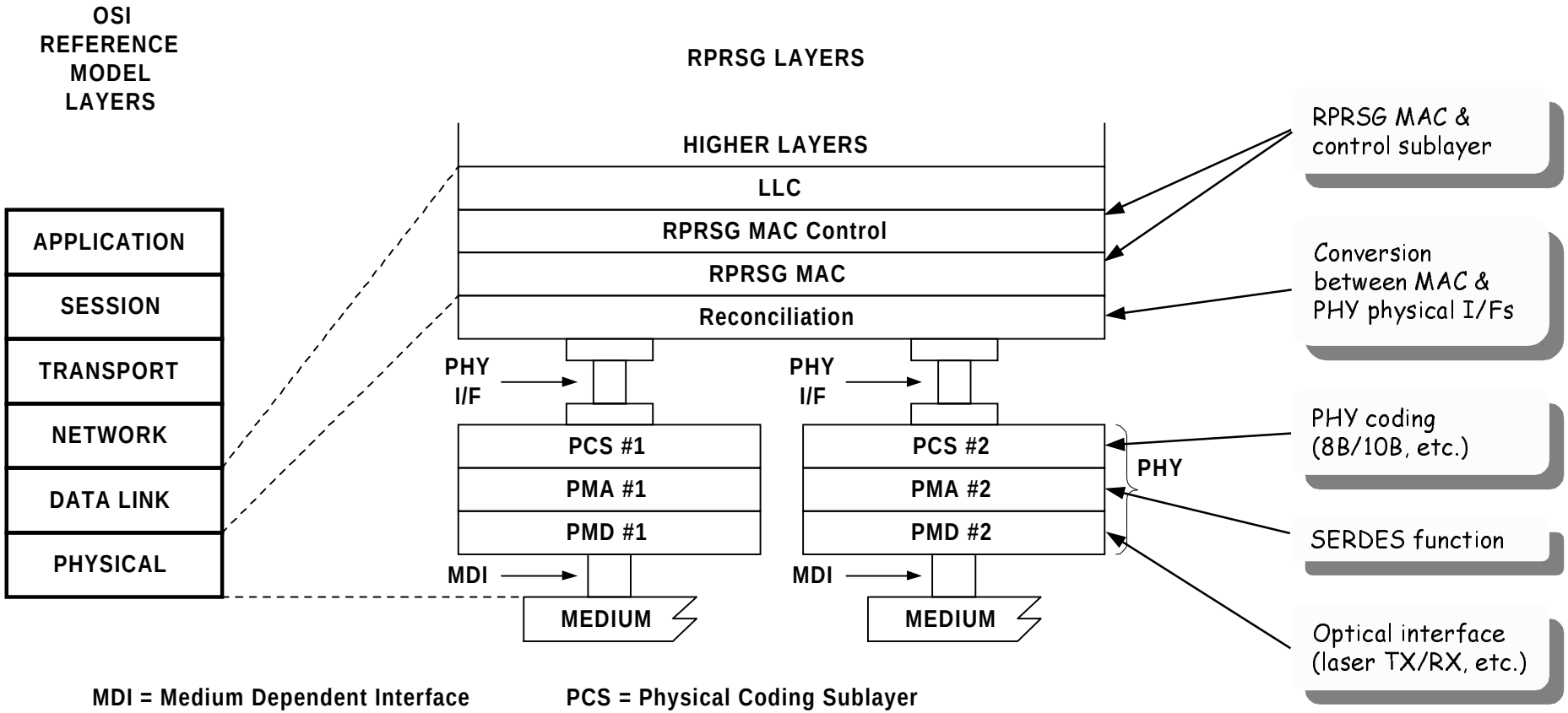
Outline

Summarize general 802 PHY service model & map to Ethernet/SONET

- Functional partitioning between RPRSG PHY and RPRSG MAC
- Mapping of PHY functions to SONET/POS, 1G Ethernet and 10G Ethernet PHY layers
- Logical Service Interface (high-level view)
  - Transmit request and receive data indication
  - PHY status indications
- Existing inter-layer and inter-sublayer interfaces
  - GMII, TBI
  - XAUI (in definition)
  - OIF SFI-4
  - ULx / PLx
- Open issues

802 Layer Diagram



MDI = Medium Dependent Interface
MAC = Medium Access Control
PHY = Physical Layer Device
LLC = Logical Link Control

PCS = Physical Coding Sublayer
PMA = Physical Medium Attachment
PMD = Physical Medium Dependent

Functional Partitioning

MAC Functions

- Packet encapsulation
  - Framing
  - FCS
- Addressing, packet switching
  - Forwarding
  - Multicast
- Priority and fairness
  - Queueing, traffic shaping
  - Congestion management
- Protection switching
  - Hello/keepalive, etc.
  - Redundant path discovery
  - Redundant path selection

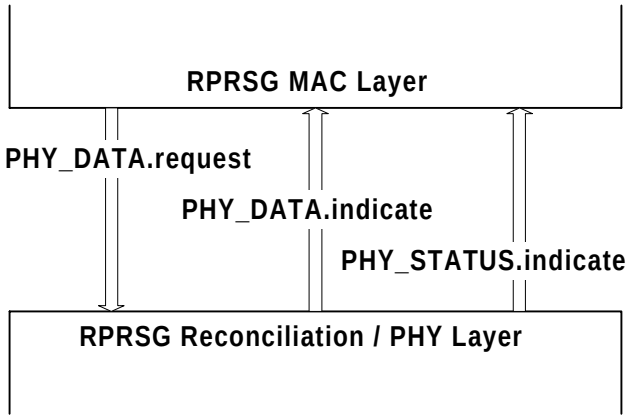
PHY Functions

- L1 Framing and coding
  - Frame delineation
  - Line coding, scrambling
- Clock/data recovery
  - Clock generation, recovery
  - Data recovery
  - SERDES
- Optical interface
  - Laser drivers, receivers
  - Connectors, media
- Signal quality detection
  - Signal fail (could be in MAC)
  - Signal degrade (could be in MAC)

PHY Functions and Mapping

PHY Function	SONET/POS	1G Ethernet	10G WAN Enet
Character Delineation	A1/A2 Framing	8B/10B Comma Detect	A1/A2 Framing
Frame Delineation	HDLC	8B/10B SOP/EOP Detect	64B/66B Coding
DC Balance	Scrambling	8B/10B Coding	Scrambling
Optical Media	Single-mode Fiber	Various Fiber	Various Fiber
MAC/PCS Interface	ULx/PLx	GMII	XGMII/XAUI
PCS/PMA Interface	OIF SFI-4, etc.	Ten Bit Interface	XBI (SFI-4 variant)
PMA/PMD Interface	Not Specified	Not Specified	Not Specified
Fault Detection	Loss of Signal Loss of Framing Loss of Pointer BIP errors (local) BIP errors (remote) Provisioning errors	Code errors (usually bit errors) Odd/Even comma errors Loss of signal (implementation-specific)	TBD, in progress (Likely to include part of SONET TOH error detection)

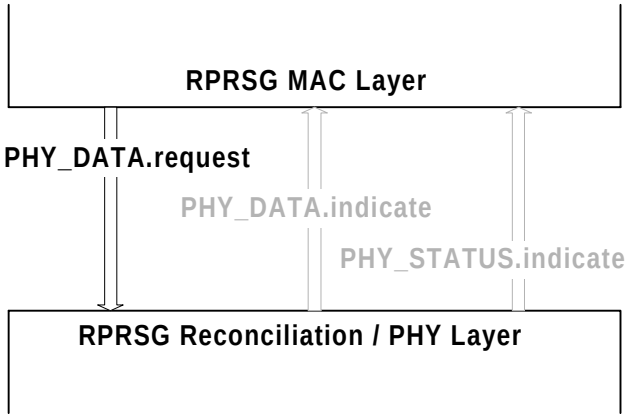
PHY Logical Interface



PHY Logical Service Interface

- Very simple interface between MAC and PHY
  - Transmit data request
  - Receive data indication
  - PHY error detect indication
- Maximal inter-compatibility
  - Minimal set of required facilities
  - Could potentially use both complex SONET PHYs and simple Ethernet PHYs
- PHY hides all Layer-1 functions
  - Common logical interface
  - Possible physical instantiation of PHY service interface (optional, like GMII)

PHY Logical Interface (TX)

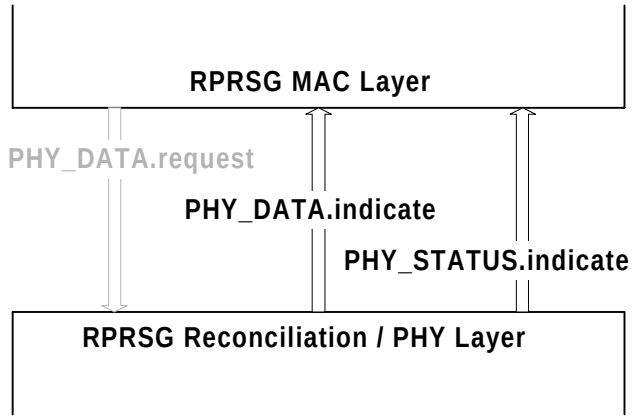


Service Interface: Transmit Data

PHY_DATA.request(OUTPUT_UNIT, IF_ID)

- Causes OUTPUT_UNIT of data to be sent on interface specified by IF_ID
- Logical interface specification required due to dual-ring topology

PHY Logical Interface (RX + Status)



Service Interface: Receive Data and PHY Status

PHY_DATA.indicate(INPUT_UNIT, IF_ID)

- Transfers INPUT_UNIT of data from interface specified by IF_ID to MAC layer
- Logical interface specification required due to dual-ring topology

PHY_STATUS.indicate(SIGNAL_FAIL, SIGNAL_DEGRADE, IF_ID)

- Generated whenever PHY status changes on interface specified by IF_ID
- SIGNAL_FAIL is asserted to indicate that synchronization is lost, or no valid signal
- SIGNAL_DEGRADE is asserted to indicate excessive error rate or poor signal quality

Current Physical Interfaces

Some standard physical instantiations of PHY/MAC and PHY/PCS I/Fs exist:

- 1 Gigabit Ethernet: TBI and GMII
  - TBI (Ten Bit Interface) between PCS (8B/10B) and PMA (SERDES)
    - 10 bits wide, 8B/10B coded data, minimal status indications
  - GMII (Gigabit Media Independent Interface) between PHY and MAC
    - 8 bits wide, uncoded data, out-of-band framing and status indications
- 10 Gigabit Ethernet: XAUI and XBI
  - XAUI (10G Ethernet Attachment Unit Interface) between PHY and MAC
    - 4 bits wide with clock recovery, 8B/10B coded, in-band framing/status
  - XBI (10G Ethernet SERDES Interface) between PCS and PMA (SERDES)
    - 16 bits wide, uncoded data, no framing or status indications; OIF SFI-4 based
- SONET: ULx/PLx and OIF SFI-4
  - UL3/UL4 and PL3/PL4 between PHY and upper layer (MAC?)
    - 32 or 16 bits wide, uncoded data, in-band or out of band framing and status indications
  - OIF SFI-4 between PCS (framer) and PMA (SERDES)
    - 16 bits wide, uncoded data, no framing or status indications

However, there is little commonality between these interfaces.

Open Issues

- Need a clear definition of status indications required from PHY
  - Loss-of-signal and Signal-degrade are probably minimal set
  - What additional indications are required for protection switching?
- Need some 802-compatible means of handling multiple interfaces at the MAC/PHY boundary, for the two rings
  - Should an RPRSG MAC sublayer handle this (like 802.3ad Link Aggregation)?
  - Should the PHY handle this (as described in the preceding)?
- Difficult to find a standardized MAC/PHY physical interface
  - Ethernet and SONET PHYs have different interfaces
  - Ethernet PHYs typically provide much less link status information
  - Finding a common interface is necessary if the RPRSG MAC is to support both PHYs in an interoperable fashion