RPR Physical Layer Proposal

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- RPR P-SAP Interface
- Ethernet RS and PHYs
- SONET/SDH RS and PHYs
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  - PoS
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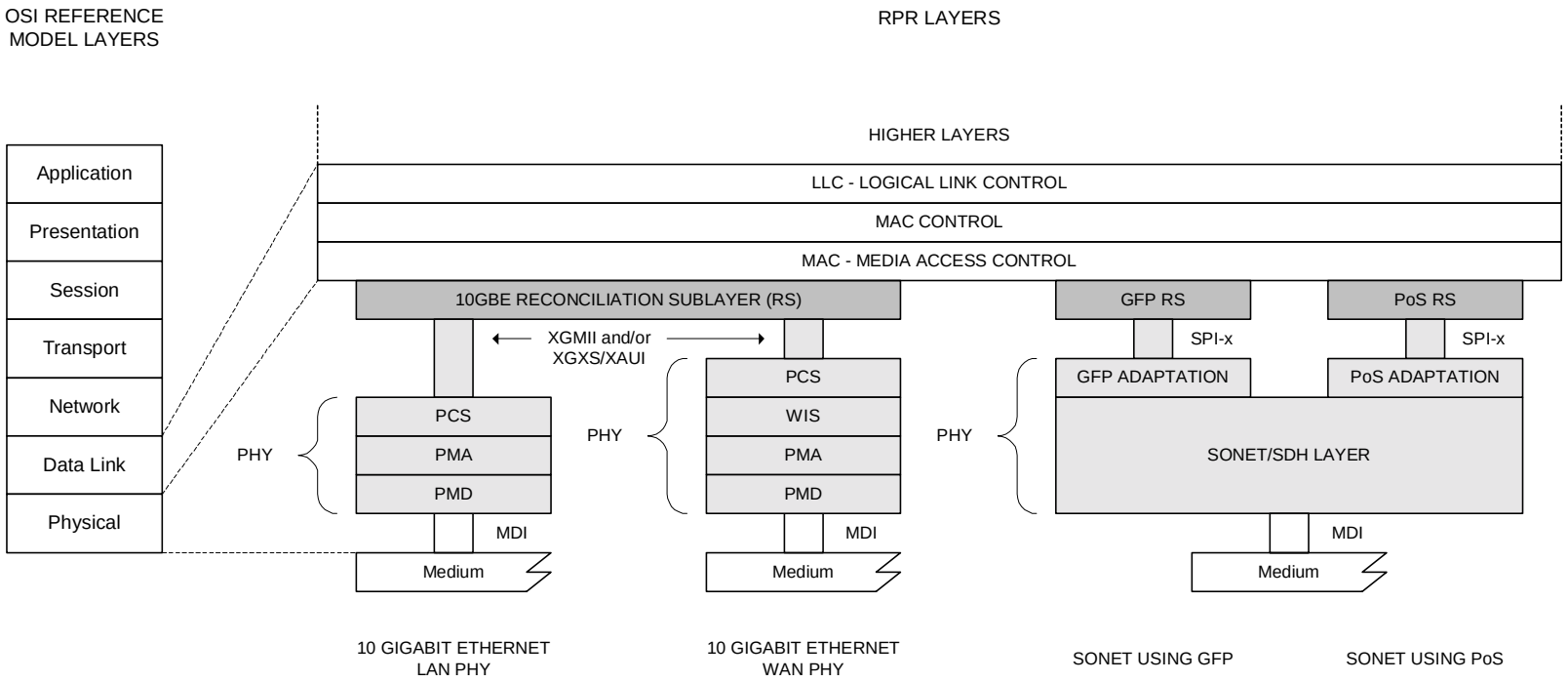
Objectives

- Present a uniform layer model view of SONET and Ethernet PHYs for RPR.
- Define a single MAC-PHY interface interface common to all physical layer implementations.
- Define a family of Reconciliation Sublayers to adapt the logical MAC-PHY interface to SONET and Ethernet PHYs, using industry-standard electrical interfaces.
- Describe the mapping of the logical frames at the MAC-PHY interface to physical frames compatible with standard SONET and Ethernet PHYs.

Layer Diagram – RPR PHYs



RPR P-SAP (MAC-PHY) Interface

- Define a logical P-SAP interface between the RS (PHY) and the MAC, common to all PHY implementations.
- The interface is defined as a set of service primitives:
  - PHY_DATA.request
  - PHY_DATA.indicate
  - PHY_DATA_VALID.indicate
  - PHY_LINK_OK.indicate
  - PHY_READY.indicate
- The interface does not operate at a constant data rate.
  - The P-SAP primitives define the transfer of whole frames, fields, and other parameters.
  - Some PHY specific fields are inserted by RS (such as IPG for Ethernet).

What is the RPR P-SAP?

- The P-SAP is a logical interface between the MAC and PHY layers, for the purpose of describing the interaction between these layers in the standard.
- The P-SAP is a set of logical primitives.
- The P-SAP does not define an electrical interface. There are no signals specified that correspond to the P-SAP interface.
- The P-SAP is not a compliance point. The existence and operation of the P-SAP cannot be verified or measured.

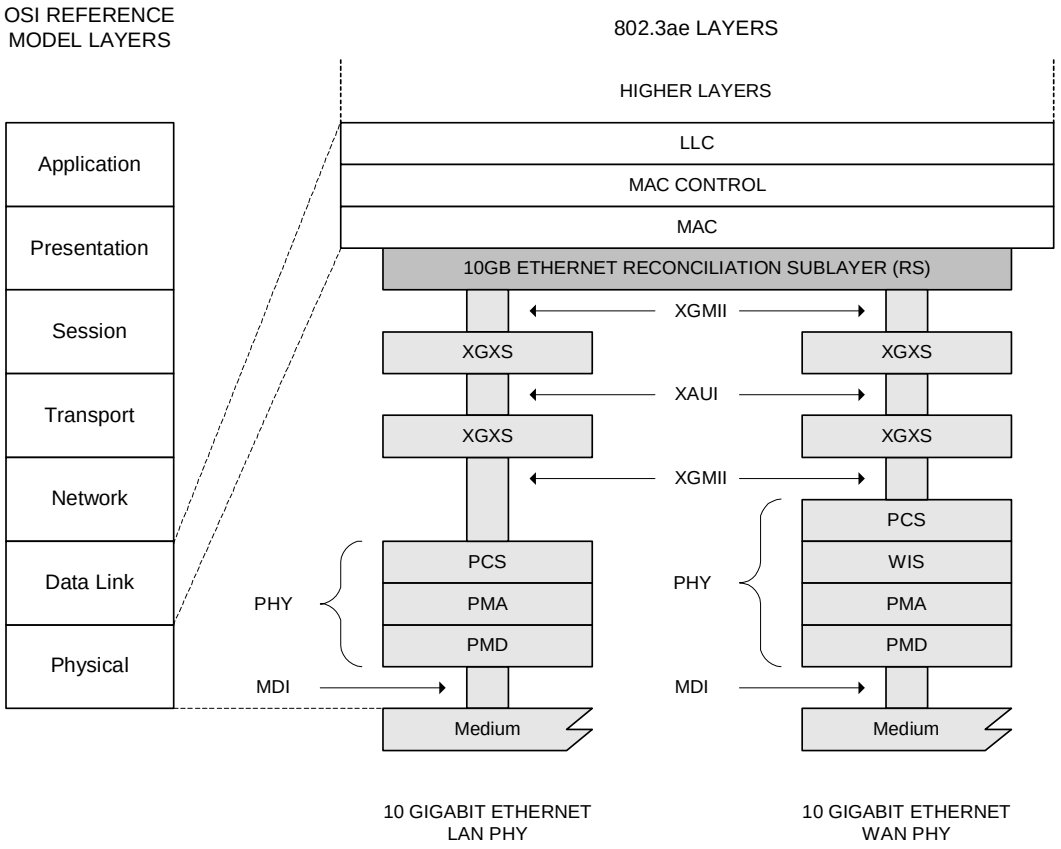
RPR P-SAP Service Primitives

- The RPR P-SAP service primitives:
  - PHY_DATA.request(OUTPUT_FRAME, length)
    Defines the transfer of a frame from the MAC to the RS.
    OUTPUT_FRAME={frame, NO_FRAME}
    The length parameter is an optional field required only for the GFP RS sublayer
  - PHY_DATA.indicate(INPUT_FRAME, length)
    Defines the transfer of a frame from the RS to the MAC.
    INPUT_FRAME={frame}
    The length parameter is an optional field required only for the GFP RS sublayer
  - PHY_DATA_VALID.indicate(DATA_VALID_STATUS)
    Indicates whether the parameter of PHY_DATA.indicate contains valid data.
    DATA_VALID_STATUS={VALID, NOT_VALID}
  - PHY_LINK_STATUS.indicate(LINK_STATUS)
    Indicates whether the PHY indicates that the link is OK.
    LINK_STATUS={OK, FAIL, DEGRADE}
  - PHY_READY.indicate(READY_STATUS)
    Indicates whether the PHY is ready to accept a new MAC frame.
    READY_STATUS={READY, NOT_READY}

Ethernet RS and PHYs

- Define a 10 GbE Reconciliation Sublayer (RS) for RPR to map the RPR P-SAP primitives to the P802.3ae PHYs and interfaces.
- Other than the RS, support the P802.3ae Physical Layer interfaces and sublayers with no changes.
- Support all seven LAN and WAN PHYs specified by P802.3ae.
- This proposal specifically addresses 10 GbE, but is intended to be extensible to other Ethernet speeds.

Ethernet RS and PHYs - Layer Diagram



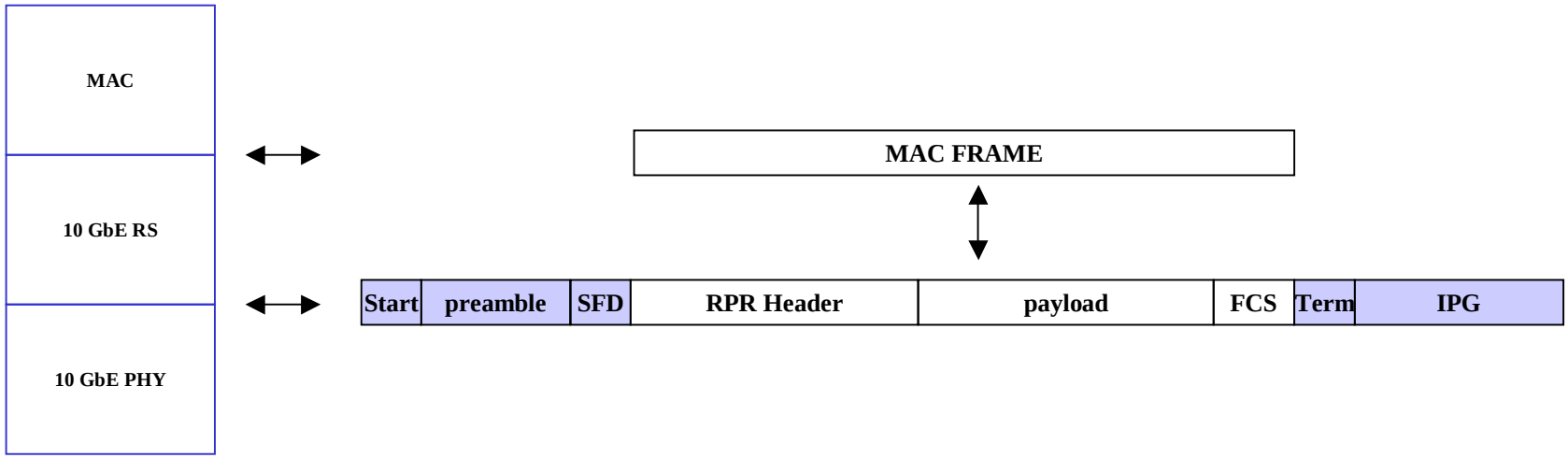
LLC = LOGICAL LINK CONTROL
MAC = MEDIA ACCESS CONTROL
MDI = MEDIUM DEPENDENT INTERFACE
PCS = PHYSICAL CODING SUBLAYER
PHY = PHYSICAL LAYER ENTITY
PMA = PHYSICAL MEDIUM ATTACHMENT
PMD = PHYSICAL MEDIUM DEPENDENT
WIS = WAN INTERFACE SUBLAYER
XGMII = 10 GIGABIT MEDIA INDEPENDENT INTERFACE

Ethernet RS and PHYs – RS Functions

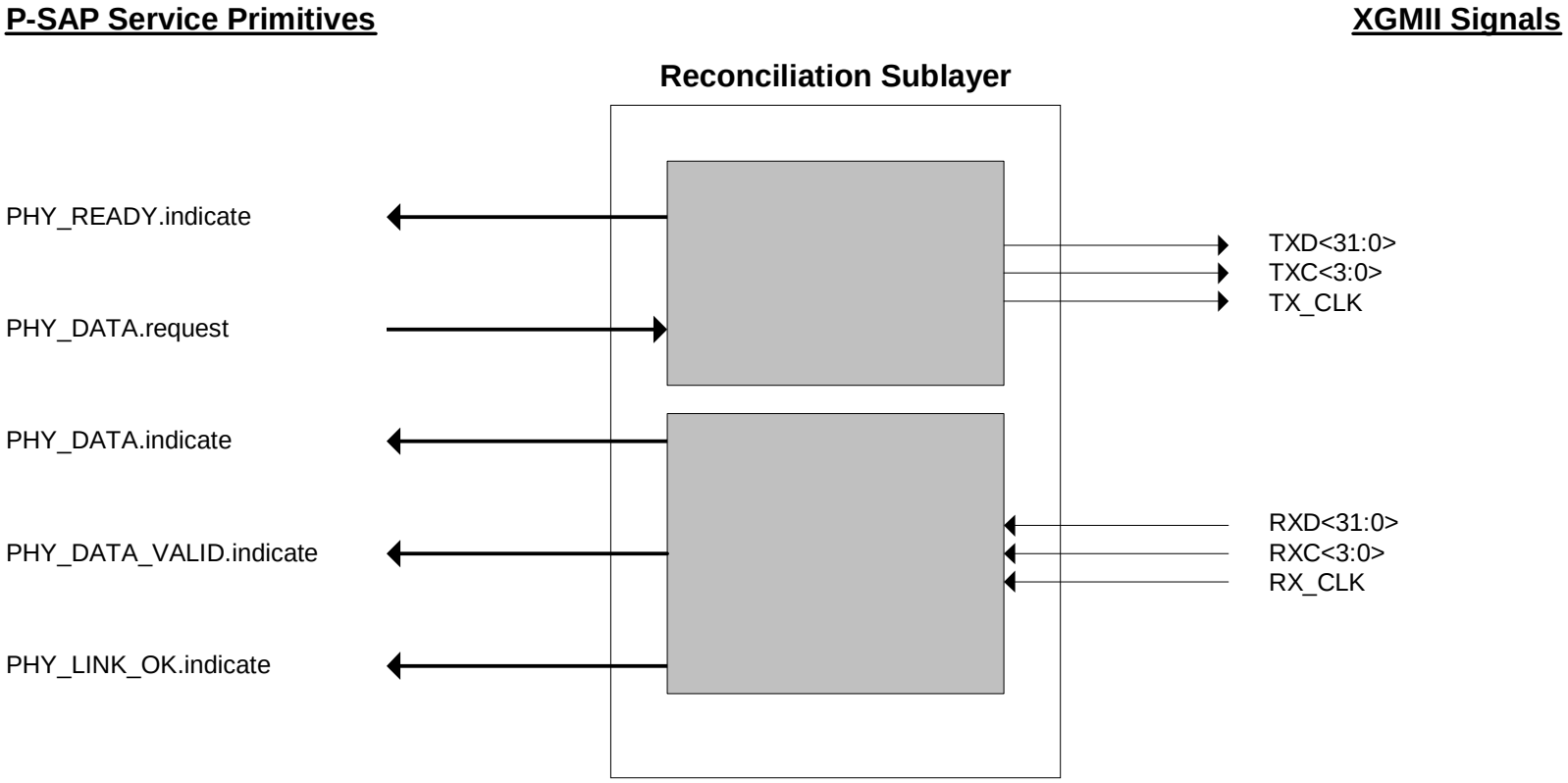
- The RS retains the following functions specified by P802.3ae, Clause 46:
  - Converts the logical P-SAP service primitives to/from electrical signals at the XGMII.
  - Map the first octet of Preamble to a Start control character, and align it to “lane 0” on the XGMII.
  - Map the first octet of IPG following a packet to a Terminate control character.
- For RPR, add/modify the following RS functions:
  - Generate IPG according to the rules specified in 802.3 (for ethernet, interframe gap period is generated by the MAC).
  - Modify the Link Fault Signaling behavior of the RS to allow dual-simplex operation as described in 802-17-01-0075 (Sept).

Ethernet RS and PHYs – Frame mapping

- The Reconciliation Sublayer maps a logical RPR MAC frame to an Ethernet-compatible physical frame, and adds IPG:



Ethernet RS and PHYs – RS I/Os

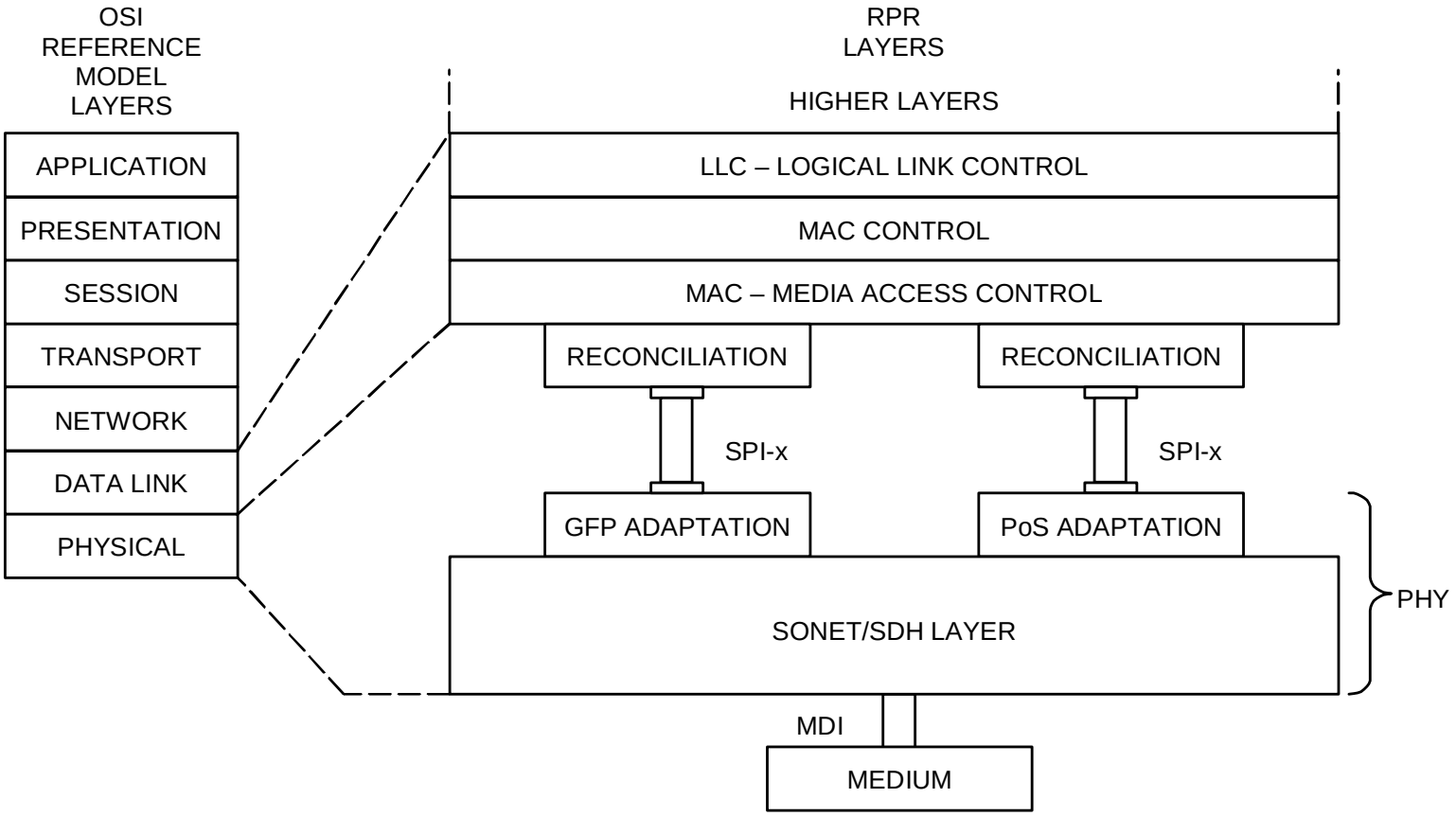


Ethernet RS and PHYs – PHYs

- Include the 10 GbE Physical Layer in the RPR standard by reference to P802.3ae (excluding the RS).
  - Support the optional XGMII with no change.
  - Support the optional XGXS/XAUI with no change.
  - Support all seven PHYs with their associated sublayers with no changes.
    - Four “LAN PHYs” operating at a data rate of 10.0 Gbps.
    - Three “WAN PHYs” operating at a data rate and format compatible with SONET STS-192c and SDH VC-4-64c.

SONET/SDH PHYS

SONET RS and PHYs - Layer Diagram



MDI – MEDIUM DEPENDENT INTERFACE

SPI – SYSTEM PACKET INTERFACE

Main Points

- SONET/SDH PHY supports full-duplex operations
- The SONET/SDH layer used in IEEE 802.17 is fully compliant with the existing ITU-T Recommendations (e.g. G.707 and G.783)
- Two different adaptation sublayers are foreseen for IEEE 802.17
  - The GFP adaptation sublayer
  - The PoS adaptation sublayer
- The adaptation layers work over any defined SONET/SDH Path layer (VC4 or VC4-4Nc) or virtually concatenated Path (VC4-Nv or STS-1-Nv)

System Level Interface (SPI)

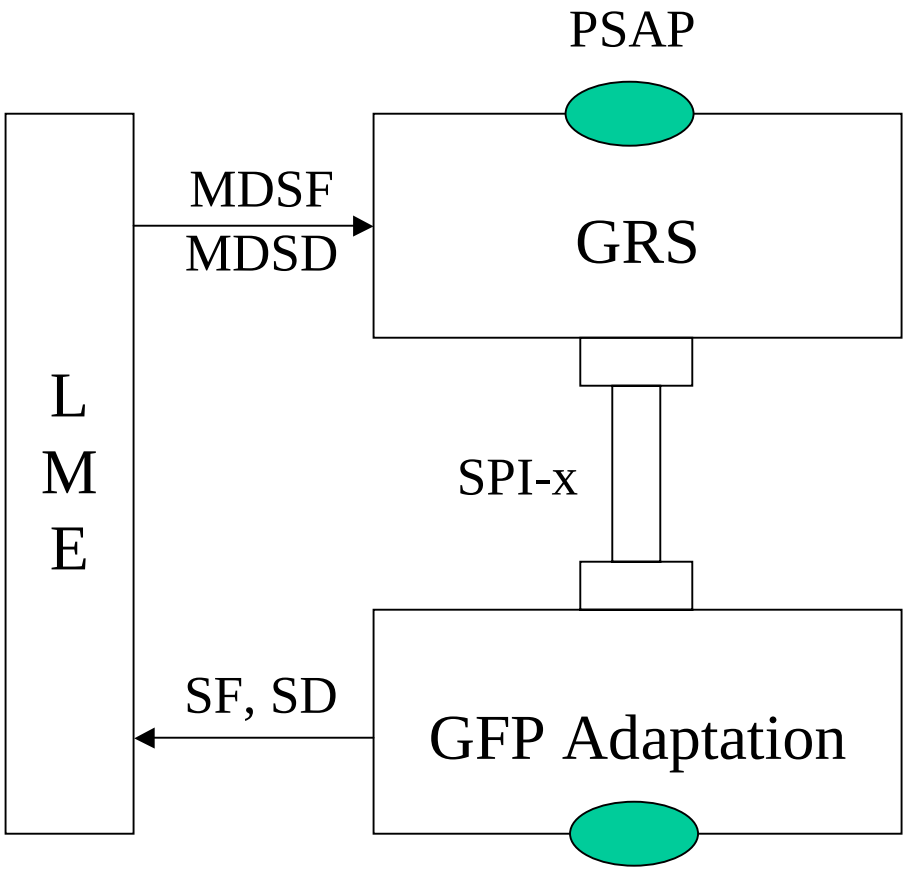
- SPI is a family of interfaces already defined by the OIF to interconnect the MAC and the PHY entities
- Two versions are supported for IEEE 802.17
  - SPI Level 3
  - SPI Level 4 Phase 1 and 2

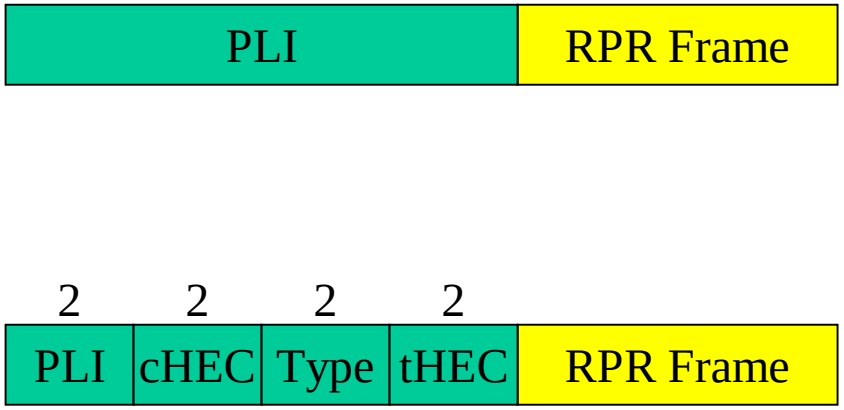
GFP Framing

- GFP operations should be compliant with G.7041
- It is proposed to use the frame-mapped GFP with the null extension header and no GFP FCS

- These functions are divided into two blocks
  - The Generic Reconciliation Sublayer (GRS)
  - The GFP Adaptation sublayer

GFP Framing – 2





[Defined by ITU-T]

Generic Reconciliation Sublayer

- Adds the first 8 bytes of the RPR frame according to the GFP specification (Tx direction)
- Optionally check the tHEC and Type fields and regenerates the first 8 bytes of the RPR frame (Rx direction)
- Sends/Receives the GFP frames to/from the SPI
- Conveys the Signal Fail (MDSF) and Signal Degrade (MDSD) information from the Layer Management up to the RPR MAC sublayer
- Three GRS versions are defined
  - GRS Version 1 with the 8-bit SPI-3
  - GRS Version 2 with the 32-bit SPI-3
  - GRS Version 3 with the SPI-4 Phase 2

GFP Adaptation Sublayer

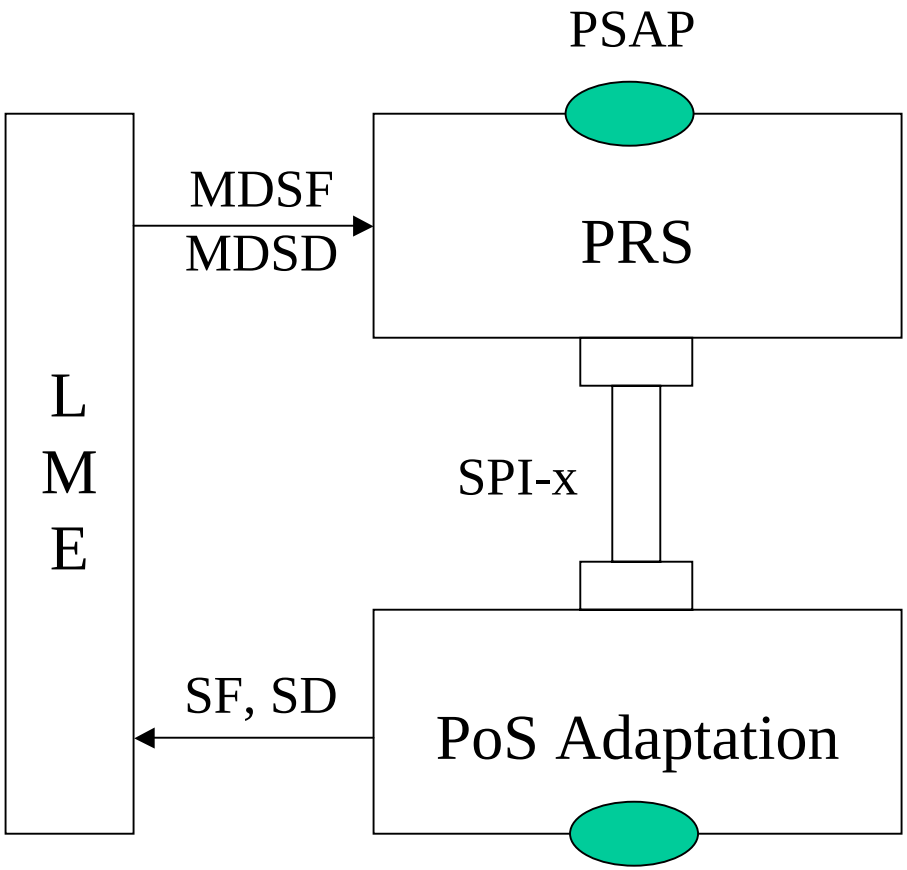
- Performs GFP frame delineation (Rx direction)
- Performs GFP rate adaptation (inserting/removing GFP idle frames)
- Performs scrambling/descrambling of the GFP payload area
- Conveys the Trail Signal Degrade (TSD) from the SONET/SDH layer to the LME
- Conveys the Trail Signal Fail (TSF) from the SONET/SDH layer to the LME
- Detects the Payload Mismatch (PLM) and the Loss of Frame Delineation (LFD) defects

PoS Framing

- The PoS framing is another option for mapping RPR frames over SONET/SDH interfaces
- PoS shall use byte-synchronous HDLC for frame delineation. There is no PPP/HDLC frame encapsulation.

- These functions are divided into two blocks
  - The PoS Reconciliation Sublayer (PRS)
  - The PoS Adaptation sublayer

PoS Framing – 2



RPR Frame

RPR Frame

[Defined by ITU-T]

PoS Reconciliation Sublayer

- Sends/Receives the RPR frames to/from the SPI
- Conveys the Signal Fail (MDSF) and Signal Degrade (MDSD) information from the LME up to the RPR MAC
- Three PRS versions are defined
  - PRS Version 1 with the 8-bit SPI-3
  - PRS Version 2 with the 32-bit SPI-3
  - PRS Version 3 with the SPI-4 Phase 1
  - PRS Version 3 with the SPI-4 Phase 2

PoS Adaptation Sublayer

- Performs flag insertion and deletion
- Performs octet stuffing and de-stuffing
- Conveys the Trail Signal Degrade (TSD) from the SONET/SDH layer to the LME
- Conveys the Trail Signal Fail (TSF) from the SONET/SDH layer to the LME
- Detects the Payload Mismatch (PLM) defect

RPR Clocking

- Ethernet stations are independently clocked.
  - 10 GbE sublayers support multiple clock domains—MAC and PHY could be separately clocked.
- SONET stations are either synchronous or independently-timed:
  - Local timing from a station clock source
    - Stratum-3 supported for interoperability but not required
  - Line timing from the received clock.
  - Operation over virtual channels of a synchronous network.

Summary

- SONET and Ethernet PHYs for RPR are described using a uniform layer model.
- A single, PHY-agnostic PSAP interface is defined between the MAC and PHY layers.
- A family of Reconciliation Sublayers are used to adapt the logical PSAP interface to standard Ethernet and SONET electrical interfaces.
- Use standardized Ethernet and SONET PHYs for RPR with no changes.
- Common physical layer approach to several proposals.