Project	**IEEE 802.20 Working Group on Mobile Broadband Wireless Access** <**http://grouper.ieee.org/groups/802/20/**>
Title	**LG Electronics Components Proposal for 802.20 MBWA**
Date Submitted	**2007-03-07**
Source(s)	Young C. Yoon LG Electronics Mobile Research 10225 Willow Creek Rd. San Diego, CA 92131 Voice: 858-805-6555 Fax: Email: ycyoon@lge.com
Re:	MBWA Call for Proposals
Abstract	This contribution describes a number of component proposals for a Mobile Broadband Wireless Access (MBWA) system – referencing the current draft proposal.
Purpose	For consideration and adoption into the 802.20 MBWA standard.
Notice	
Release	
Patent Policy	

LGE 802.20 Components Proposal

LG Electronics

March 7, 2007

Introduction

- LG proposes a number of 802.20 component proposals
  - » Primarily aimed to enhance the current draft of the STD IEEE 802.20
- The proposed components are:
  - » RL Frame Design Enhancement during Silence Periods
  - » Shared Signaling Control Assignment Channel (F-SSACH)
  - » Acknowledgement Channel for Shared Signaling Channel (R-sschACKCH)
  - » Flexible LDPC Code
  - » MIMO
  - » Interlace-switching

RL Frame Design Enhancement during Silence Periods

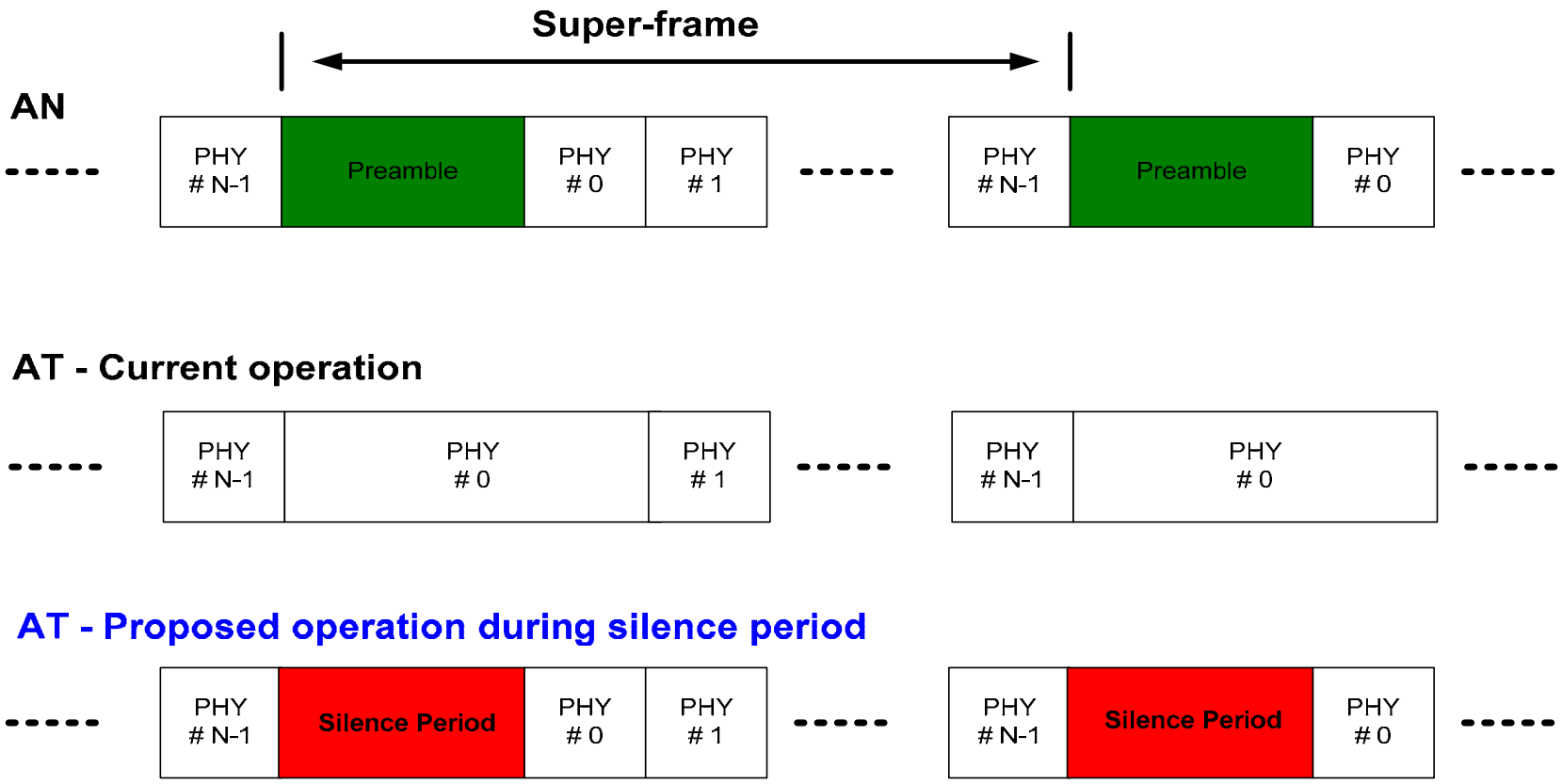
RL Frame Design Enhancement during Silence Periods 1/2

- We propose an enhancement to the RL frame design during the silence period
  - » Specifically, the design of RL PHY Frame #0
- Relates to:
  - » Section 7.1.3 “Superframe timing”
  - » Section 7.7.6.5 “Reverse link silence interval”
  - » Could be added into both sections

RL Frame Design Enhancement during Silence Periods 2/2

- Currently, RL PHY frame #0 is elongated for alignment w/:
  - » the FL preamble and FL PHY frame #0 [2, p. 19]
- We propose changing the RL PHY frame #0 design during silence periods
  - » Instead of the elongated RL PHY frame #0, use the regular sized RL PHY frame for frame #0 – aligned w/ FL PHY frame #0.
  - » The remaining unused portion can be used for the silence period
- Periodicity is in SilenceIntervalPeriod

RL Frame #0 Design During Silence Period



RL Frame #0 During Silence Periods - Benefits

- The benefits of this enhancements are:
  - » No interruption of RL PHY layer
    - H-ARQ operation is maintained
  - » Currently, a duration of one RL PHY layer frame is lost
    - which pre-empts control and data transmissions originally “scheduled” for transmission during frame #0

Shared Signaling Assignment Channel (F-SSACH)

Shared Signaling Assignment Channel (F-SSACH)

- A broadcast/multicast channel sent each slot for F-SSCH management
- F-SSACH implicitly indicates the real-time partitioning of the resources between the F-SSCH's and the F-DCH's (at the slot-rate)
- Indicates:
  - The number of F-SSCH's used in a slot
  - The subset of selected F-SSCH's taken from a pool of potential F-SSCH's
- Relates to Section 7 Lower MAC Sublayer
  - Could be inserted after 7.4 "Default Shared Signaling Channel MAC Protocol"

F-SSACH – Benefits & Costs 1/2

- Benefits:
  - » Greater sector throughput via more efficient FL resource utilization:
    - F-SSCH inactivity (“OFF”) yields unused resources which can be re-allocated to carry data traffic over the F-DCH
    - Amounts to adaptive partitioning of F-DCH and F-SSCH resources
    - Eg. when no F-SSCH’s are needed in a slot, then all those tone resources earmarked for the F-SSCH’s can be used by the F-DCH’s
  - » Minimize the F-SSCH processing requirements at ATs which are able to decode SSACH:
    - These ATs will know how many F-SSCH’s to process and need only read as many as defined by the F-SSACH.

F-SSACH – Benefits & Costs 2/2

- Benefits (cont'd):
  - » Flexibility / Adaptability
    - The distribution of the *K* F-SSCH formats can be tailored to the distribution of bad to good geometry ATs.
    - For example, when the majority of ATs are in good geometry, conditions, the majority of selected F-SSCH formats can high spectrally-efficiency formats
- Cost:
  - » F-SSACH signalling overhead incurred. The overhead may not be significant because it need not be broadcasted
  - » Slight modification of sub-packet start points for those AT which has restricted nodes assigned

F-SSACH – Design

- Define *L* (eg. 4) F-SSCH formats – where each uses different spectral efficiencies
  - » To support varying AT geometries
- *K* (eg. 8) distinct F-SSCH's are defined
  - » F-SSCH_*k* where *k = 0, … , (K-1)*
  - » There are no-overlapping of tone resources
- Define a bitmap of length *K*
- The *k*th bitmap position indicates whether or not F-SSCH_*k* is transmitted or not transmitted

F-SSACH – Sharing resources on restricted nodes

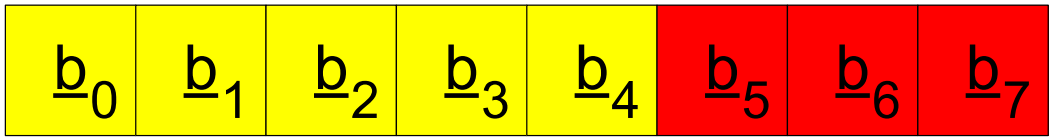
- Certain Channel IDs / nodes, denoted as restricted nodes, are specified by FL primary broadcast channel as the resource used by SSCHs.
- AN may schedule certain ATs with high geometry on these restricted nodes for data transmission.
- A DCH can use the extra resources from a restricted node only when the resource is not used by the SSCH
- ATs scheduled on the restricted nodes (either from new scheduling or a continuation sub-packet) are informed of the resource partitioning by decoding the SSACH.

F-SSACH – Notes

- Notes:
  - » ATs able to decode SSACH demodulate only those F-SSCH's which are "ON" as indicated by the bitmap
  - » ATs not able to decode SSACH try to demodulate all the F-SSCHs
  - » Leftover resources from "OFF" F-SSCH's are used for carrying traffic (F-DCH)
  - » Protective-measure:
    - When an F-SSACH decoding failure occurs at a particular AT, the AT decodes all *K* F-SSCH's.
    - This requires ATs which are assigned restricted nodes to have pre-defined start locations for each encoder sub-packet re-transmission (to be shown later)
  - » AT geometry determines detection sequence of the SSCH's
    - Eg. Bad geometry ATs begin reading F-SSCH formats w/ lower spectral efficiencies
  - » SSACH is sent w/ a power level sufficient to reach those ATs which are assigned restricted nodes

F-SSACH – Example w/ *K*=8, *L*=2 1/2

Bitmap supporting a maximum of 8 F-PDCCHs

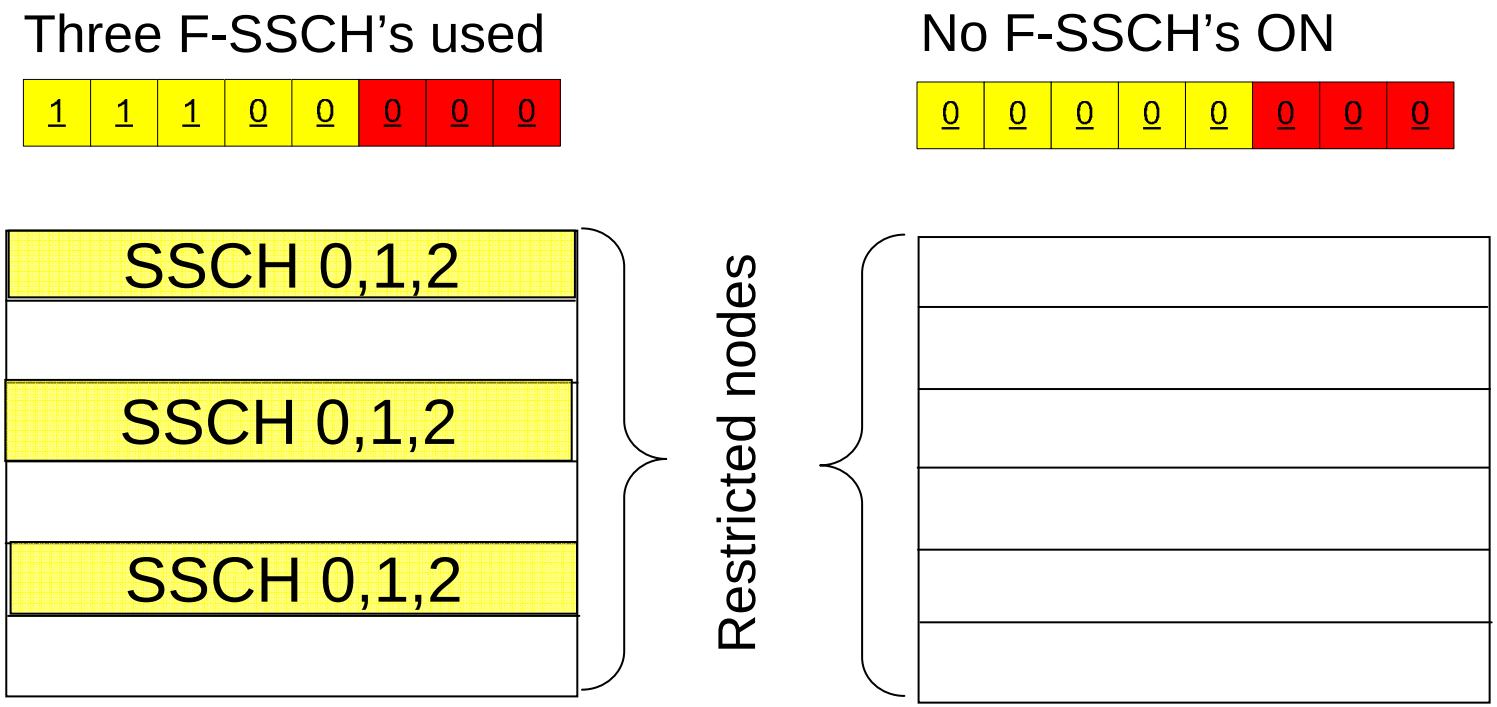


Bitmap for a F-PDCCH format selection with low spectral efficiency

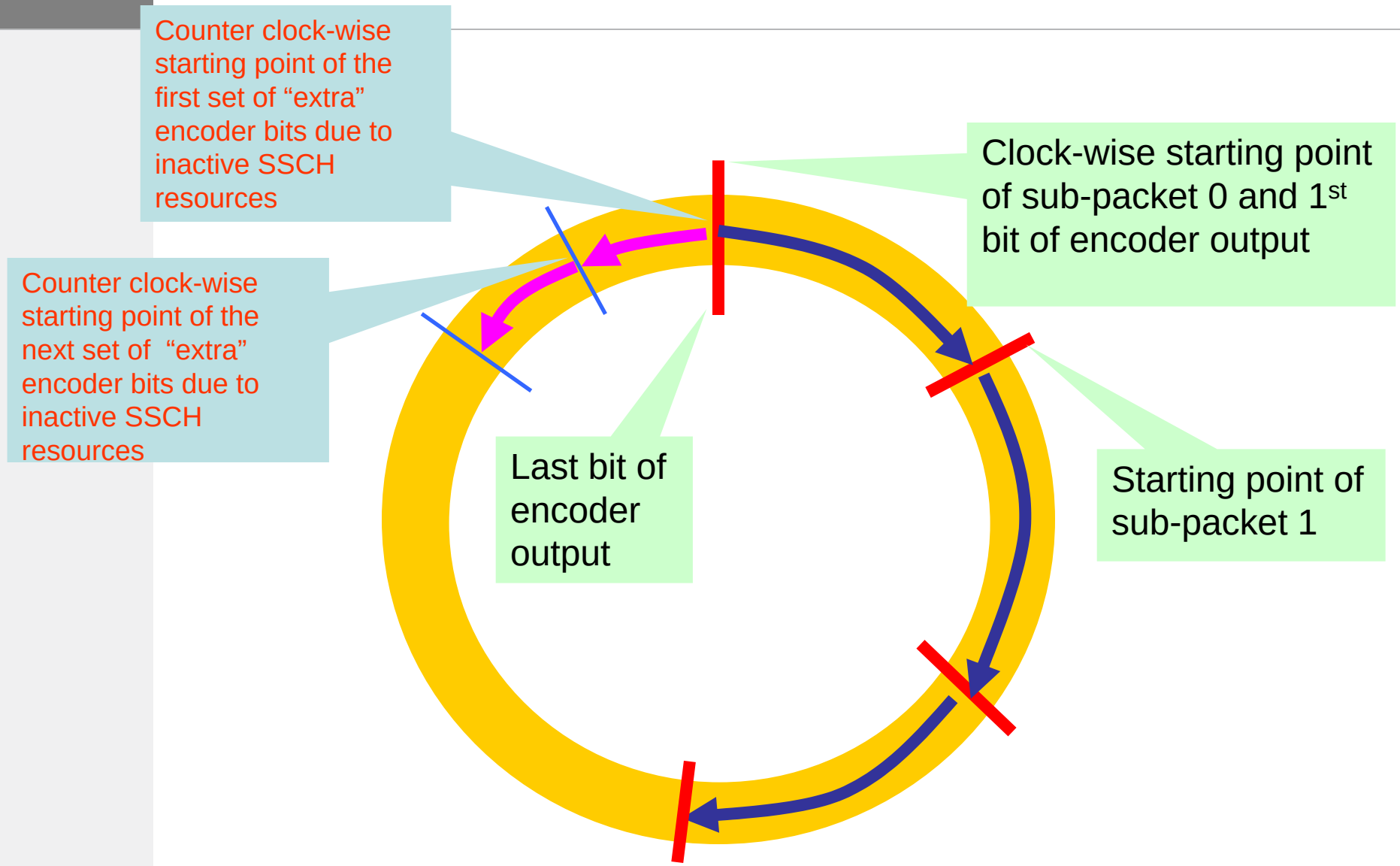
Bitmap for a F-PDCCH format selection with high spectral efficiency

F-SSACH – Example w/ *K*=8, *L*=2 2/2

- Resource partitioning between F-DCH and F-SSCH



F-DCH Encoder Rule for “Extra” Bits



F-SSACH formats / configurations

- Length K bitmap + 16 bit CRC coded / sent as a separate PHY channel
  - One or multiple channels can be defined depending on the length of K
- K, spectral efficiency of SSACH & the configuration : announced in the super-frame preamble
- SSACH can be either:
  - » Enabled or not enabled or
  - » Not sent, if enabled

R-sschACKCH

F-SSCH Acknowledgements

- We propose an Acknowledgement channel for acknowledging the F-SSCH:
  - » R-sschACKCH
- This relates to the following sections of [1]:
  - » Section 7.4 “Default Shared Signaling Channel MAC Protocol”
    - Could be added to 7.4.6.3.1.3 “General Rules for F-SSCH” [1, p. 453 (pdf)]
  - » Section 9.4.1.4 R-ACKCH

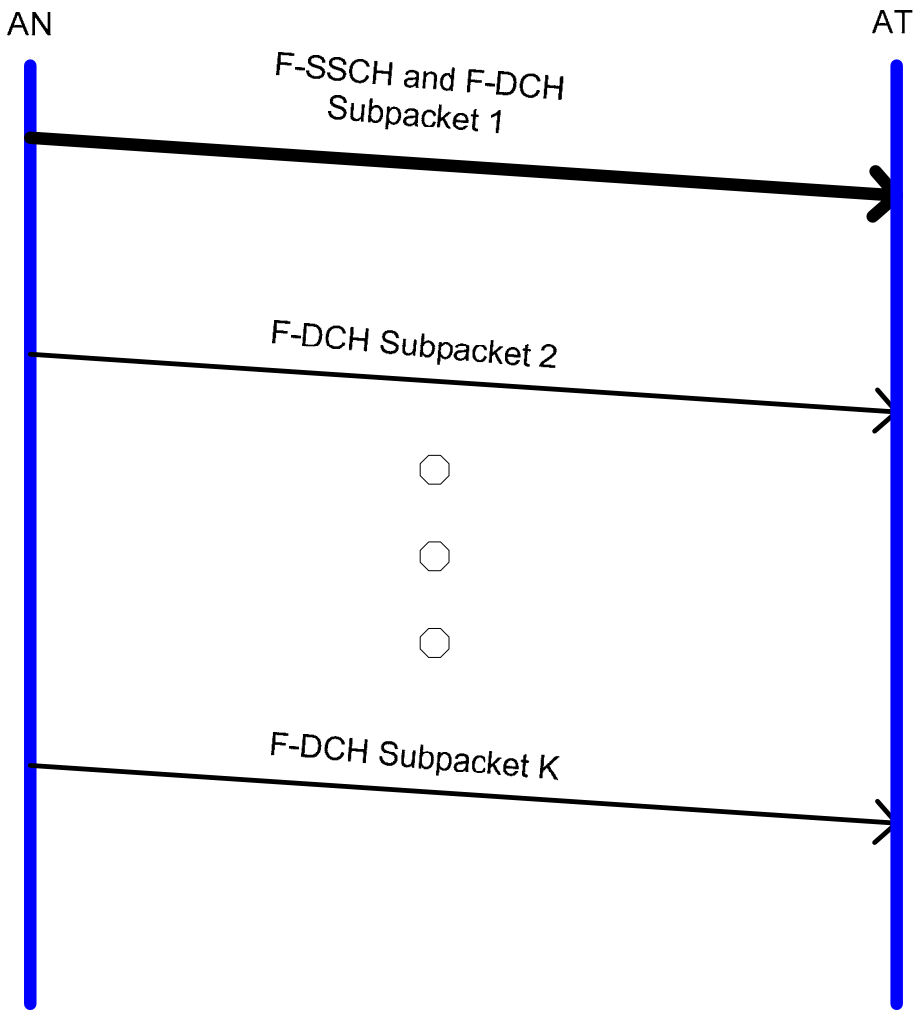
F-SSCH Acknowledgements

- Motivation:
  - » To manage not only the FER performance and Tx power of the F-DCH, but also that of the F-SSCH
- Benefits:
  - » Improved FL resource utilization and throughput:
    - Enables detection of F-SSCH FLAM decoding failure:
      - an AT misses all F-DCH sub-packets transmitted and sends no energy on the R-ACKCH indicating a NAK (Off) since it uses On-Off Keying (OOK)
      - The AN scheduler continues to schedule resources to the AT until the maximum number of re-transmissions is exhausted.

F-SSCH Acknowledgements

- Benefits (cont'd):
  - Resource and capacity hit can become significant:
    - When the node assignments for FLAM channel allocations is large e.g. greater than or equal to 20 tiles OR
    - When the data rate or payload size is large e.g. 1 Mbps, 10 Mbps or higher
      - » *Particularly acute for transmissions at or close to the proposed peak rates of 260 Mbps (20 MHz) or ~ 65 Mbps (5 MHz) [1*
  - » Enables independent power control of the F-DCH and F-SSCH – by providing Frame error event feedback
    - Allows, for example, a lower FER operating point for the SSCH (e.g. 1%) and a higher FER one (e.g. 5%) for the F-DCH
    - Can schedule those ATs w/ poor channel quality (reliability) now more reliably
    - This can allow for greater throughput and operational flexibility w/ more aggressive operation of the F-DCH.

Example: Where an AN cannot distinguish between a SSCH from a F-DCH Decoding Error



R-sschACKCH – Concept 1/3

- If R-sschACKCH ACK received, AN proceeds as usual.
- If R-sschACKCH NAK received (and 1st subpacket NAK “received” on R-ACKCH), AN either:
  - » Re-sends the same F-SSCH and 1st subpacket or
  - » Terminates the transmission (and re-schedules a different or same AT w/ a different F-SSCH)

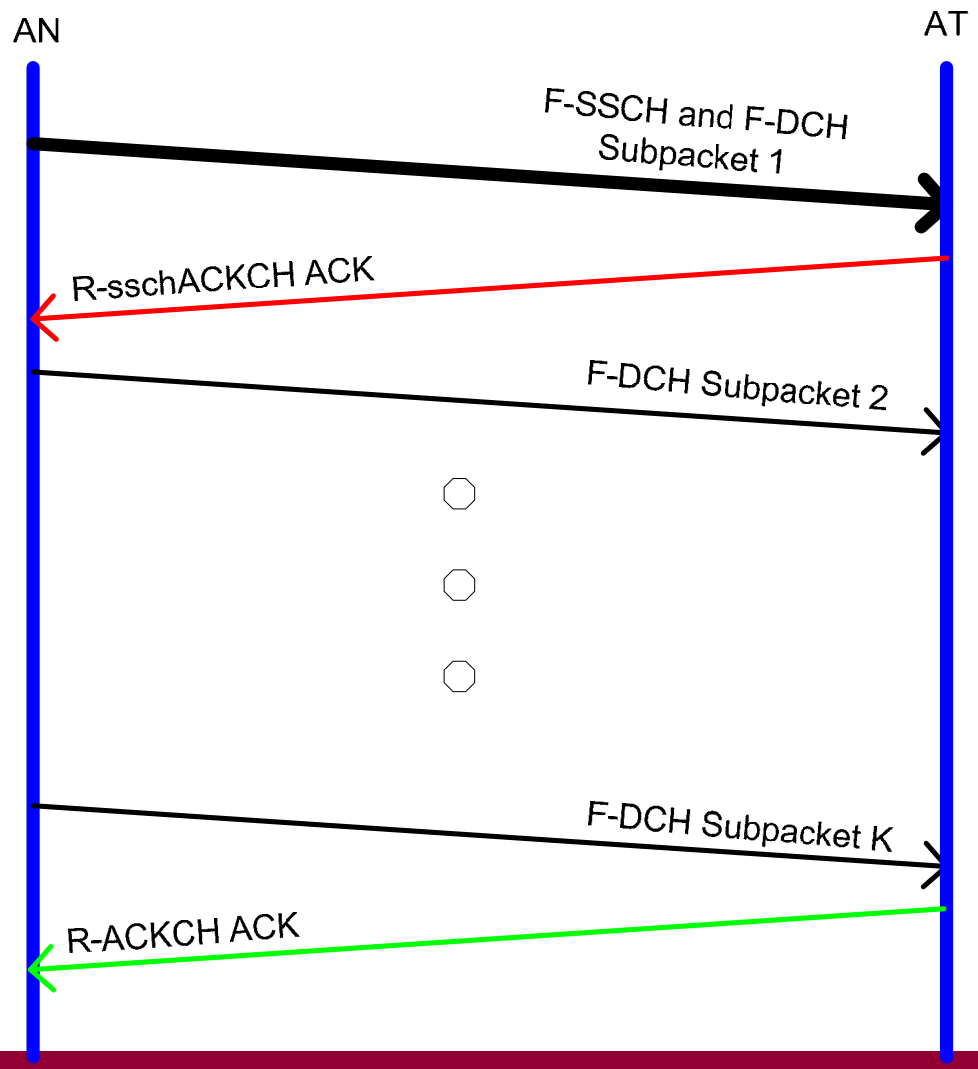
R-sschACKCH – Concept 2/3

- Transmit R-sschACKCH only if 1st sub-packet decoding fails
  - » if 1st sub-packet decoding succeeds, R-ACKCH ACK is sent which implies an R-sschACKCH ACK
- Re-use the same design approach as the R-ACKCH with the following modifications:
  - » Use “extra” unused R-ACKCH’s to carry the R-sschACKCH for F-SSCH Acknowledgement
    - For example, in 5 MHz, there are roughly 5 to 6 “unused” R-ACKCH’s given that 32 R-ACKCH’s are available but 26 to 27 R-ACKCH’s are reserved at most for F-DCH acknowledgements.
  - » Each F-SSCH can be assigned a corresponding dedicated R-sschACKH.
  - » AT, when scheduled on a F-SSCH with an enabled R-sschACKCH, sends ACK/NAKs on the corresponding R-sschACKCH when scheduled w/ a FL assignment type message.

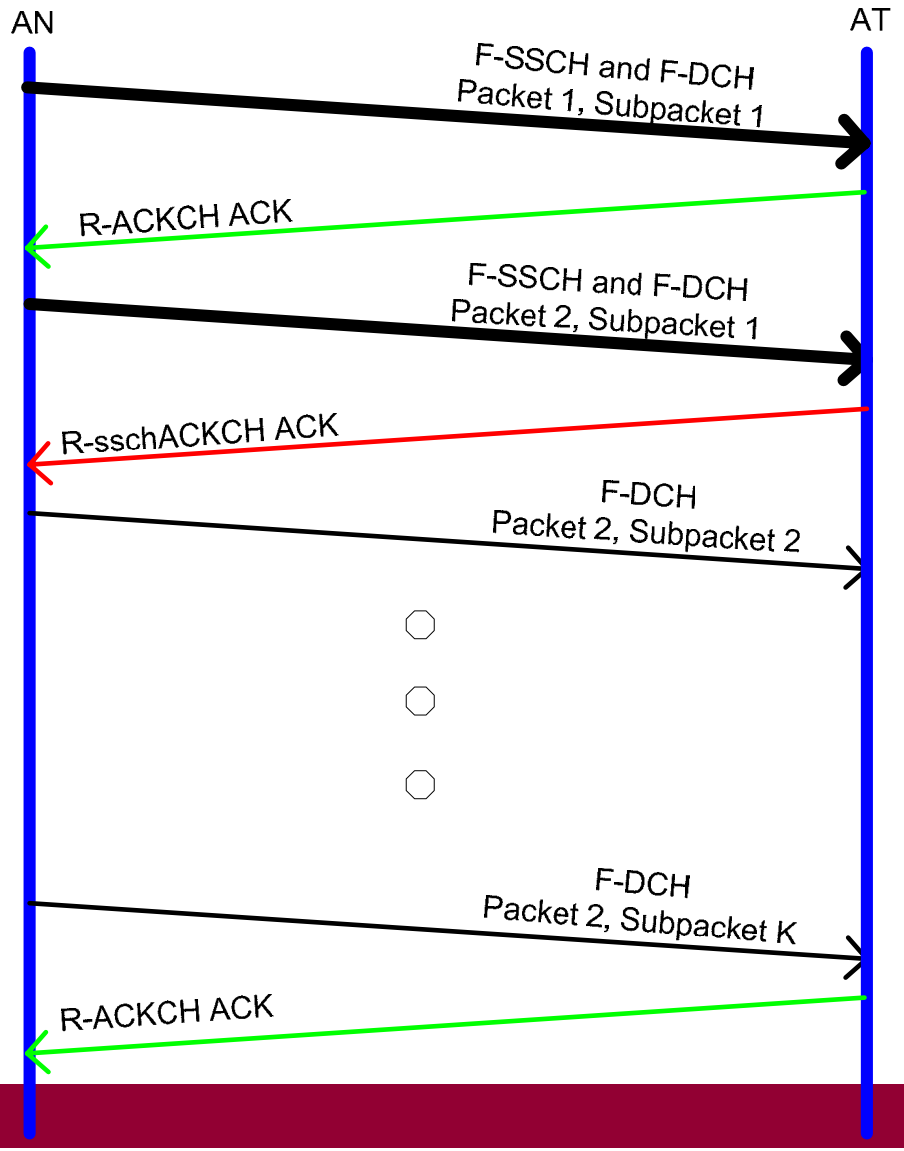
R-sschACKCH – Concept 3/3

- For example, given three F-SSCH's:
  - » Two F-SSCH's: F-SSCH_0 and F-SSCH_1 can be assigned their own dedicated R-sschACKCH's: R-sschACKCH_0 and R-sschACKCH_1.
  - » The third F-SSCH: F-SSCH_2 can be without a R-sschACKCH.
  - » ATs w/ unreliable links can be scheduled on F-SSCH_0 or F-SSCH_1.
  - » ATs w/ reliable links can be scheduled on F-SSCH_2.

Example 1: if 1st subpacket undecoded

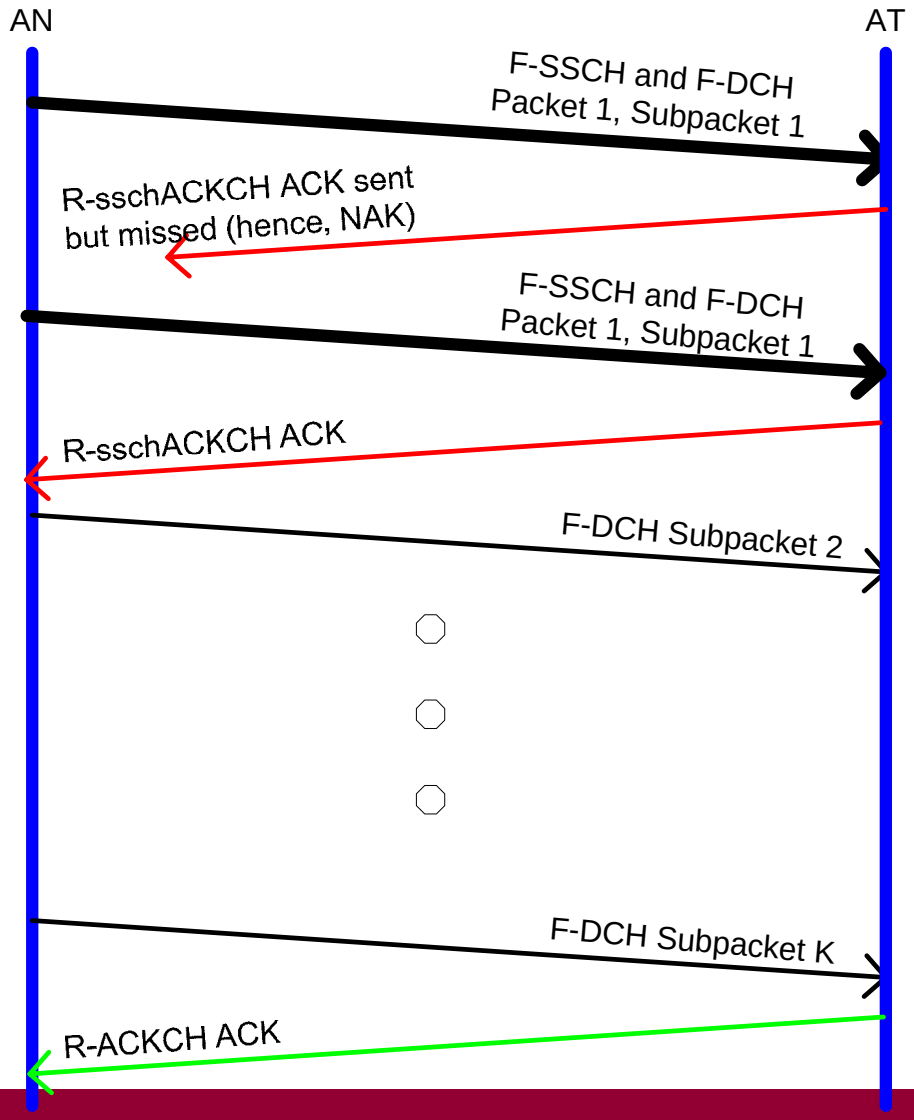


Example 2: if 1st subpacket decoded



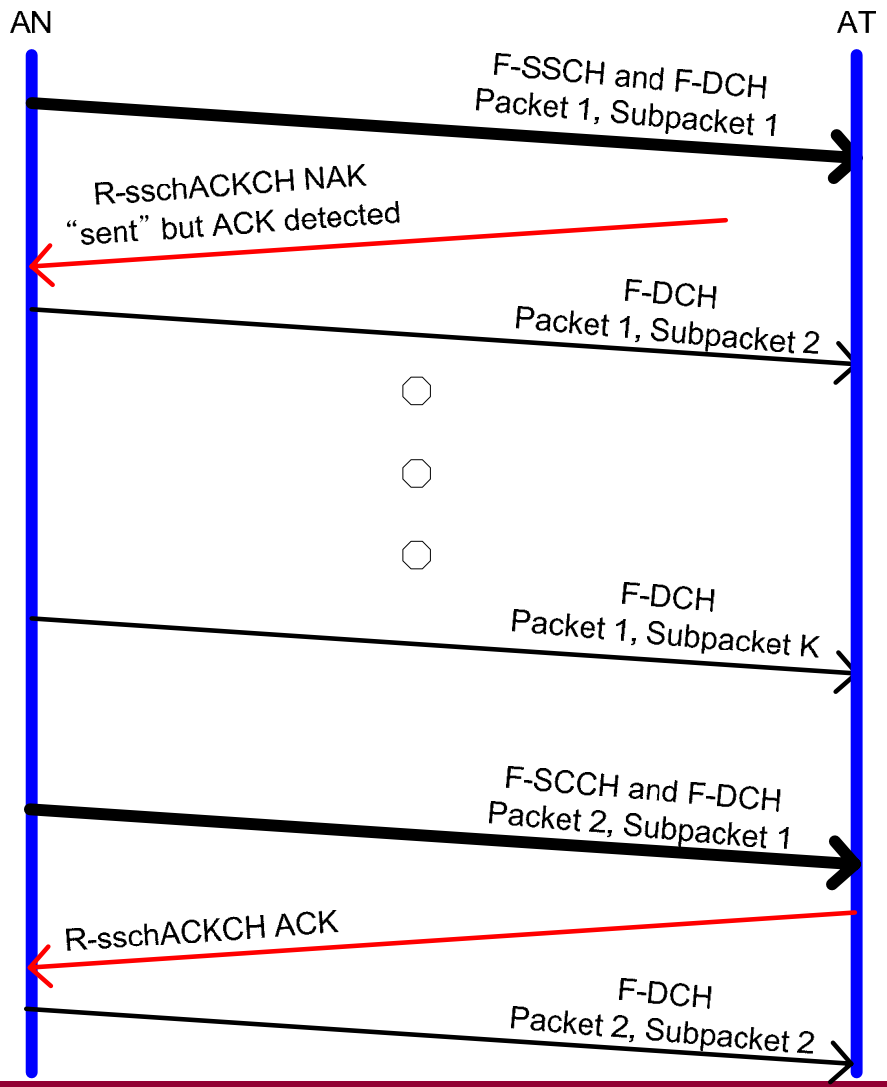
R-ACKCH ACK on 1st sub-packet implies that the F-SSCH was decoded.

Example 3: if R-sschACKCH ACK missed (ACK → NAK)1st subpacket decoded



Same AT is re-scheduled or new AT scheduled incurring a loss of one sub-packet Tx instance.

Example 4: if R-sschACKCH ACK false-alarmed (NAK → ACK)



Falls back to the original case as if R-sschACKCH never existed.

R-sschACKCH – Benefits and Costs

- Benefits:
  - » Saves on FL resources and capacity by preventing sub-packet re-transmissions of large packet sizes when F-SSCH is missed.
  - » Can be used for F-SSCH FER and power control in conjunction w/ or w/o the R-auxACKCH.
  - » No extra BW required (since “unused” R-ACKCH resources are used).
- Costs:
  - » Small RL signalling overhead

R-sschACKCH – Notes 1/2

- When R-sschACKCH ACK sent is received as NAK
  - » AN re-sends same F-SSCH (at target or boosted power) or terminates packet transmission
  - » AT expects regular operation and, hence, expects next sub-packet (unless 1st sub-packet is ACK'ed)
    - If AT detects an "unexpected" F-SSCH indicating early packet termination, then the same process is repeated and ACK is re-transmitted (at target or boosted power) .
- When R-sschACKCH NAK is received as ACK
  - » The AN operates as currently defined in [1] (as if R-sschACKCH never existed)
    - The AN continues to re-transmit sub-packets until either a R-ACKCH ACK is received or the max # of re-transmissions is exceeded.
    - AT does not realize it has been scheduled and misses the packet

R-sschACKCH – Notes 2/2

- R-auxACKCH can be used to complement R-sschACKCH operation
- For example,
  - When R-sschACKCH is not activated or
  - As a second, back-up, signalling scheme to correct for the case where R-sschACKCH ACK is sent but received by AN as NAK
    - The R-auxACKCH ACK is sent when the AT fails to decode the packet after the max. # of sub-packets received).

Flexible LDPC codes

LG Electronics, Inc.

Flexible LDPC Code – Contents

- **Introduction to Flexible-LDPC Codes**
- **Simulation Results**
- **Description of H matrix**
- **Conclusion**

- Note:
  - » the LDPC code proposal relates to Section 9.2.2 “Core Encoders” in [1].
  - » We propose adding a new section 9.2.2.3 “LDPC Codes”

Introduction to Flexible-LDPC code

- *Benefits from LDPC Codes*
- *Features of F-LDPC Codes*
- *Dual diagonal structure*
- *Matrix-Dividing & Row-combining*
- *Encoding & Decoding*

Benefits of F-LDPC Codes

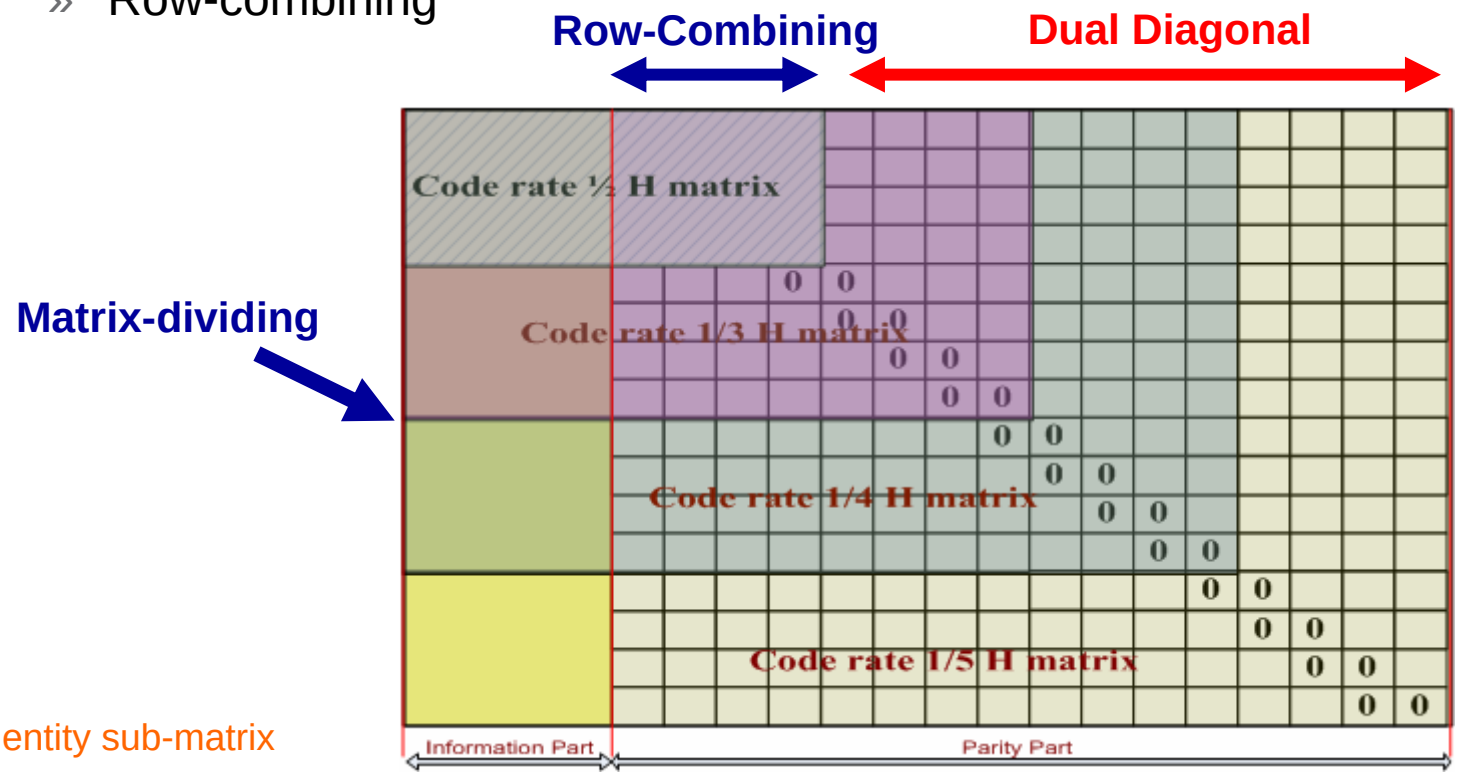
- High Decoding Performance
  - » Because F-LDPC codes does not require puncturing, F-LDPC codes show better performance at high code rate.
- High Decoding Throughput
  - » With the structure supporting parallel processing, F-LDPC codes easily increase decoding throughput.
- Low Complexity
  - » Simple decoding structure enables F-LDPC codes to reduce the amount of computation.
- High spectral efficiency
  - » Because CRC is not required, F-LDPC codes can enhance spectral efficiency.

Features of F-LDPC Codes

- Code rate
  - » Any code rate can be supported from 1/5 to 1 with one mother matrix.
- Size
  - » Various codeword length is supported by expanding sub-matrices.
- HARQ
  - » Both Incremental Redundancy and Chase Combining are supported.
- Fast encoding
  - » Due to dual diagonal structure, encoding is simple and fast.
- Parallel processing
  - » Parallel processing in encoding/decoding increase decoding throughput, resulting in high data rate transmission.

Structure of F-LDPC Codes

- Simple encoding & HARQ-IR support
  - » Dual diagonal structure
  - » Matrix-dividing
  - » Row-combining



Where
0 : Identity sub-matrix

Dual Diagonal Structure

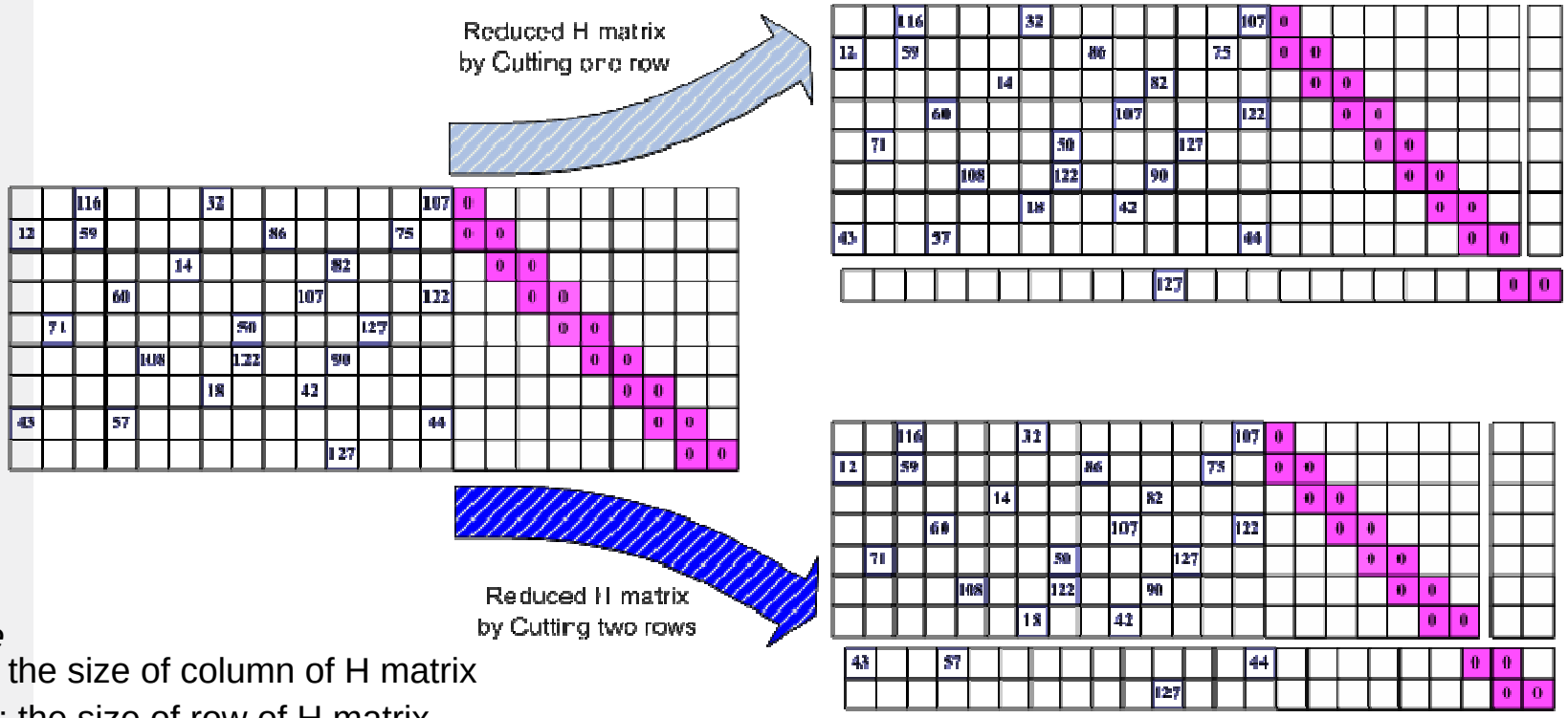
- Easy to encode & HARQ-IR support
  - » Parity bits are generated successively
  - » A retransmission needed, the encoder continues to generate additional required parity bits from the last parity bits of the previous transmission.

Average Variable Node Degree each code rate

Code rate	Avg Var Degree
1/2	3.15
1/3	3.47
1/4	3.60
1/5	3.68

Matrix-Dividing

- Code rate of LDPCC is determined by the size of H matrix $r = \frac{n_b - m_b}{n_b}$
- To support high code rate, F-LDPCC uses matrix-dividing
- Matrix-diving eliminate rows of H matrix, inducing the reduced H matrix for higher code rate.



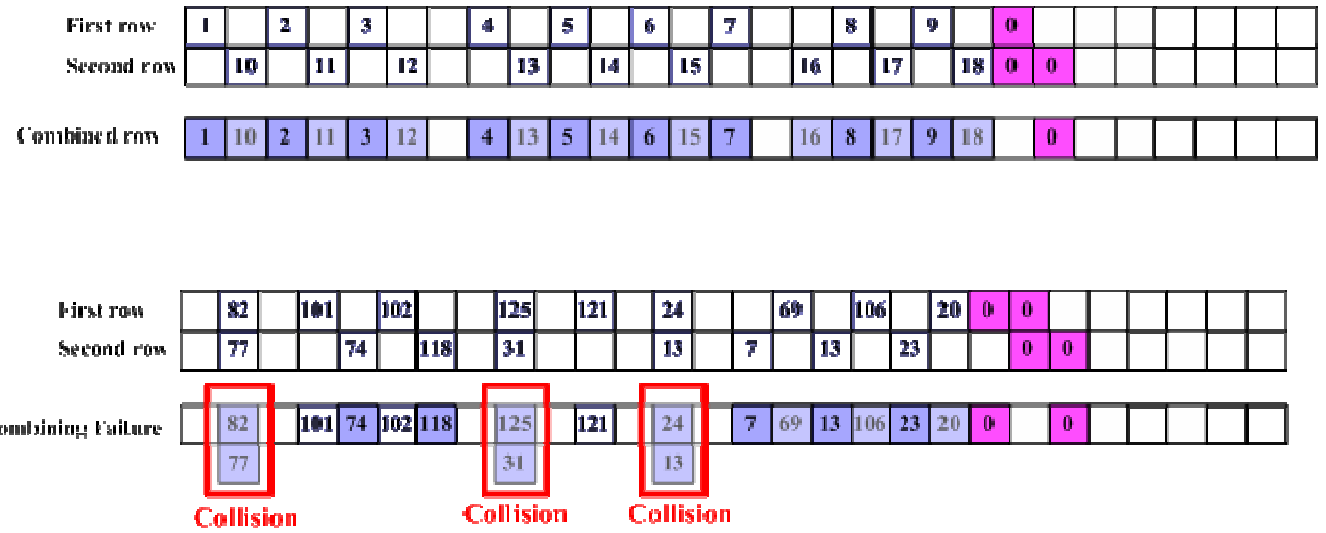
Where

n_b : the size of column of H matrix

m_b : the size of row of H matrix

Row-Combining(1/2)

- Row-combing to support Higher code rate
  - » If two rows of H matrix do not have weight in the same column, the two rows can be combined to reduce the number of rows.
- Example



Row-Combining(2/2)

- Example of reducing the size of H matrix for higher code rate
  - » Code rate : 4/5 -> 5/6

Disappeared Column because of even weights

Size : 5x25

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
1	10	82	122	101	9	102		85	125	56	121	58	24	82		69	58	106	5	20	0				
2	37	77		61	74	114	118	90	31		86		13	5	7	47	13	90	23		0	0			
3	5	54	53	26		104	6	24	116	104	36	84	32		107		41	12		107		0	0		
4		43		49			12		59			14			86		82		75				0		127
5	38		43		0			71		60				50		107		127		122				0	127

Row Combining

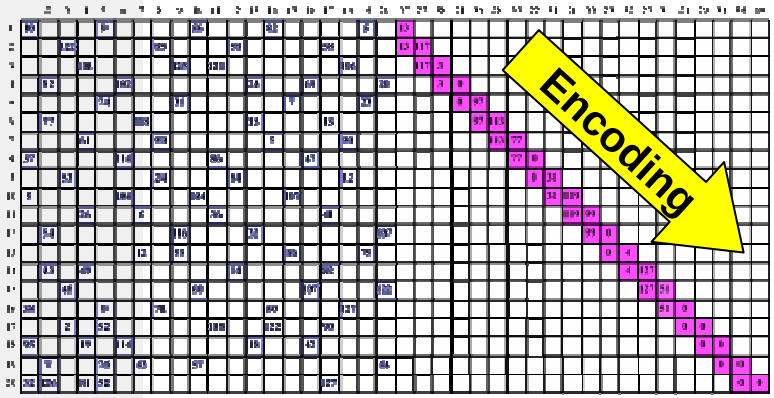
Size : 4x24

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	10	82	122	101	9	102		85	125	56	121	58	24	82		69	58	106	5	20	0			
2	37	77		61	74	114	118	90	31		86		13	5	7	47	13	90	23		0	0		
3	5	54	53	26		104	6	24	116	104	36	84	32		107		41	12		107		0	0	
4	38	43	43	49	0		12	71	59	60		14		50	86	107	82	127	75	122			0	0

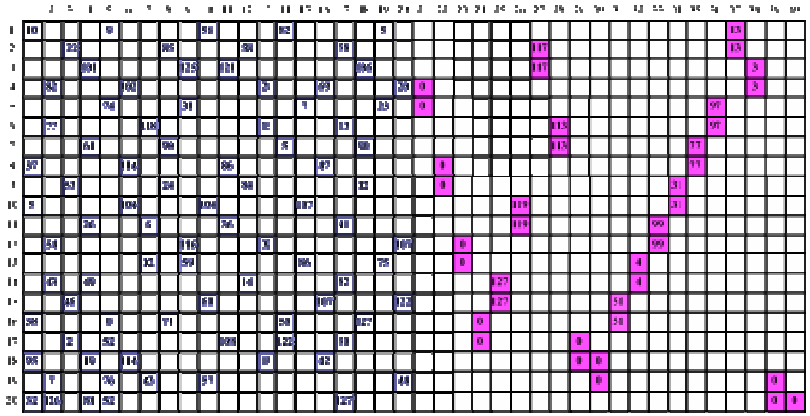
Encoding

- Step 1 :
  - » In F-LDPCC, blocks of parity bits are generated successively.
- Step 2:
  - » Blocks of parity bits are reordered to support HARQ-IR

H matrix for Encoding



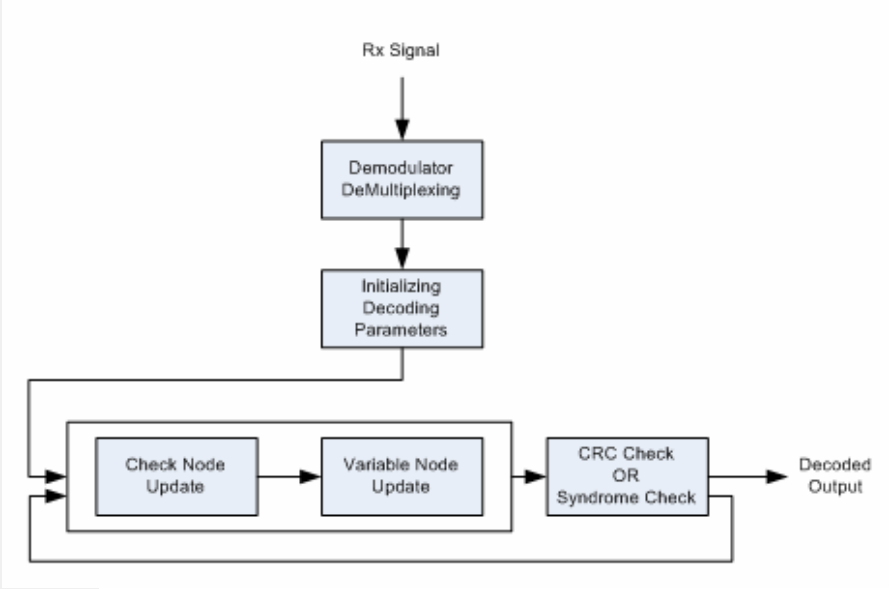
H matrix for Decoding



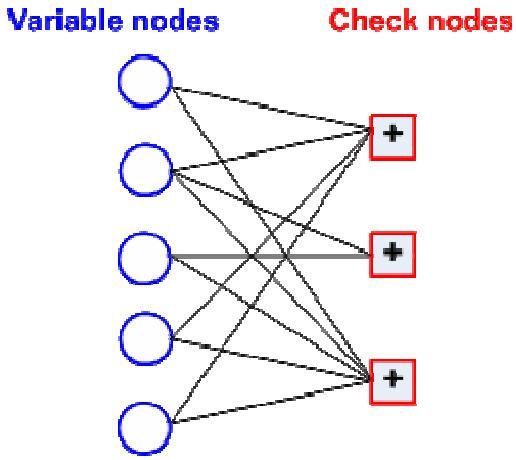
Reordered Parities (Equivalent matrices)

Decoding

- Received bits are decoded using iterative decoding algorithm.
- Message passing algorithm in Factor graph is used for decoding.



Block Diagram of LDPC decoder



Factor graph for LDPC decoding

Simulation Results

Parameters for Link performance

Link Performances per PFI (Packet Format Index)

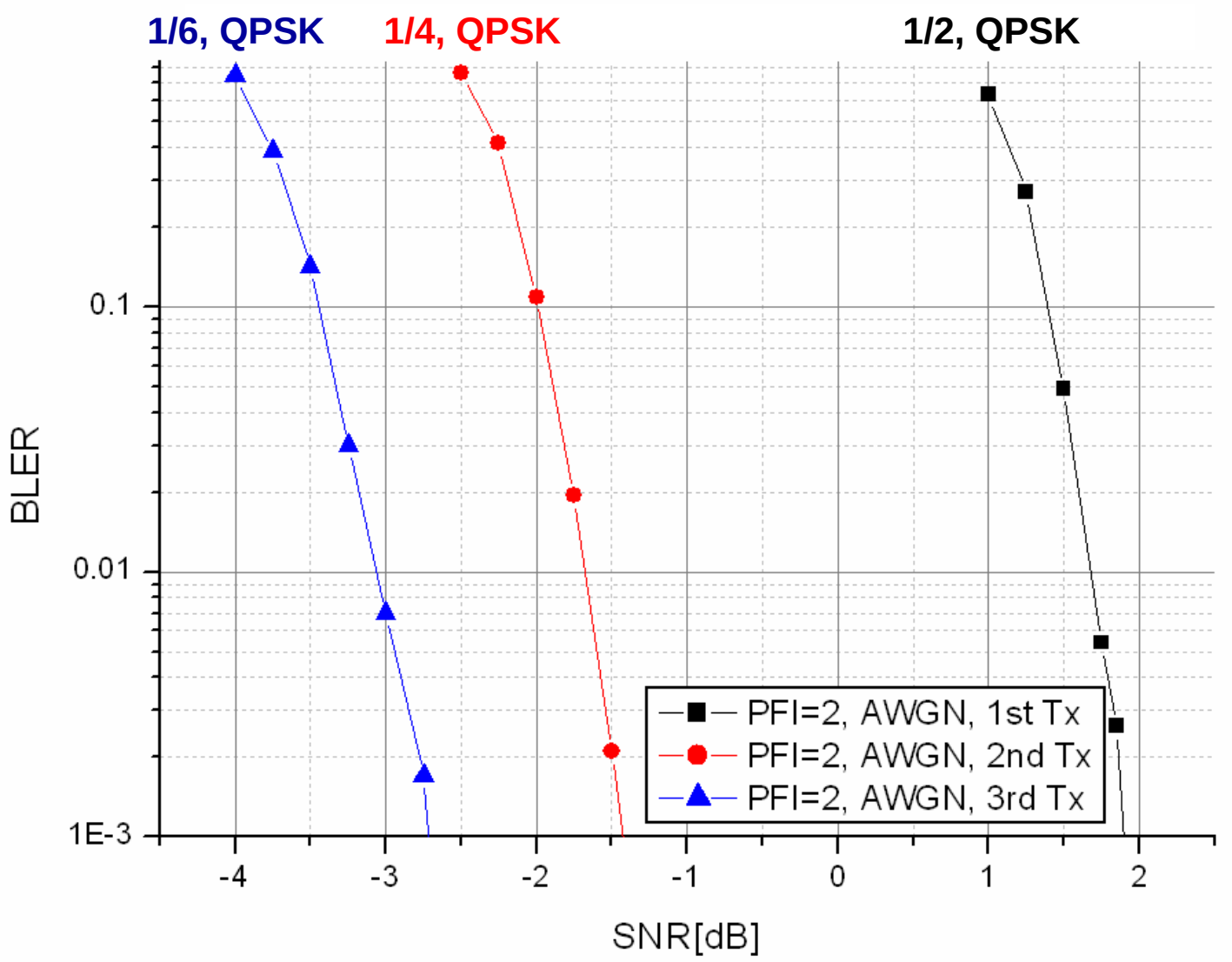
Parameters for Link Performance

Decoding Algorithm	Log-scale Belief Propagation (Log BP)
Number of Iteration (NI)	25,50
Effective code rate & modulation	1/6~11/12 & QPSK,8PSK,16QAM, and 64 QAM Specified in the following page
HARQ	Incremental Redundancy 3 retransmission
Channel	AWGN
Codeword length	880 modulated symbols

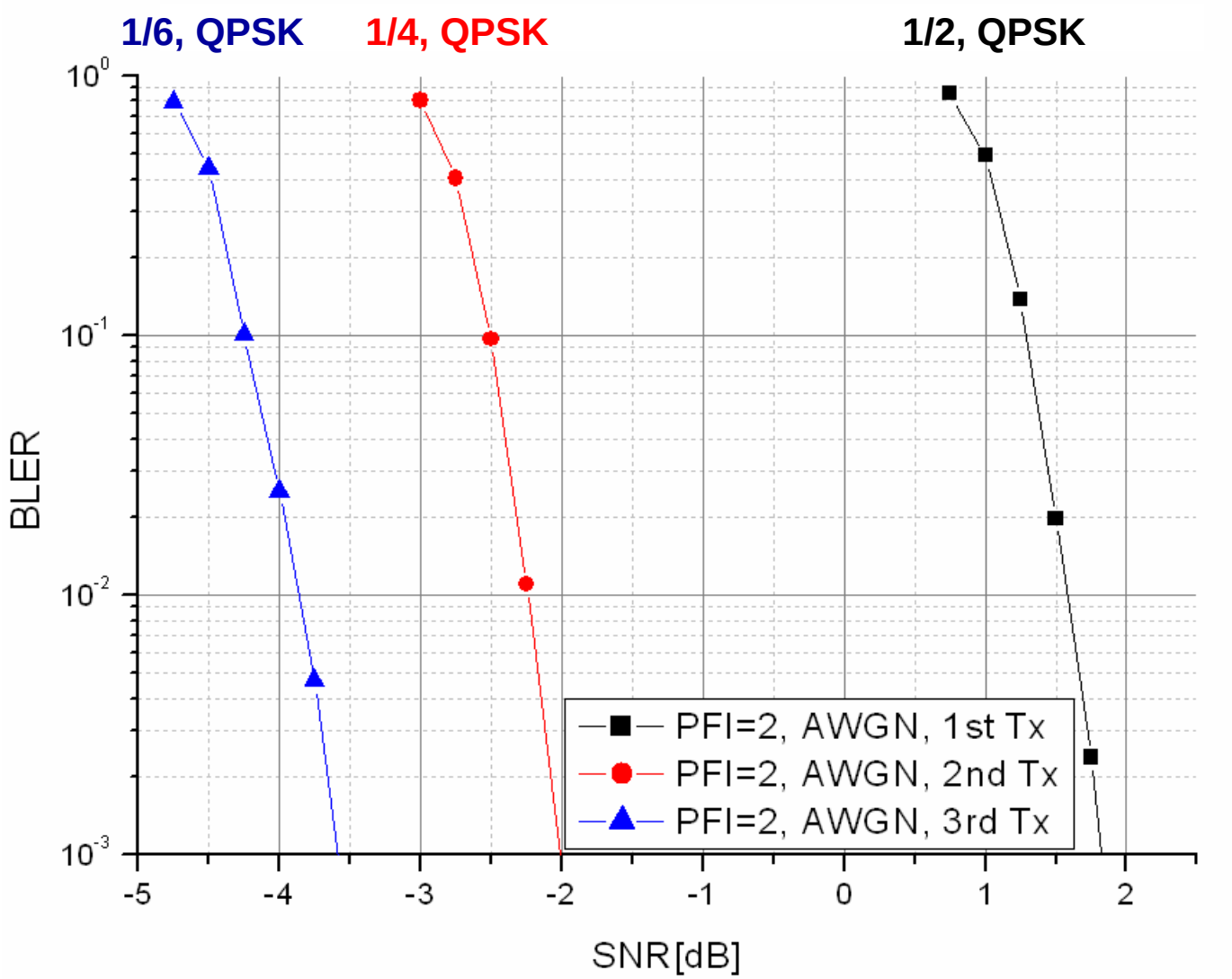
Effective code rate and modulation for simulation

Packet Format Index	1st Tx.	2nd Tx.	3rd Tx.	4th Tx.
PFI 2	1/2 QPSK	1/4 QPSK	1/6 QPSK	N/A
PFI 4	1/2 16QAM	2/7 8PSK	1/5 8PSK	N/A
PFI 8	5/6 64QAM	5/12 64QAM	5/16 16QAM	N/A
PFI 14	11/6 (Non Decodable) 64QAM	11/12 64QAM	11/18 64QAM	11/24 64QAM

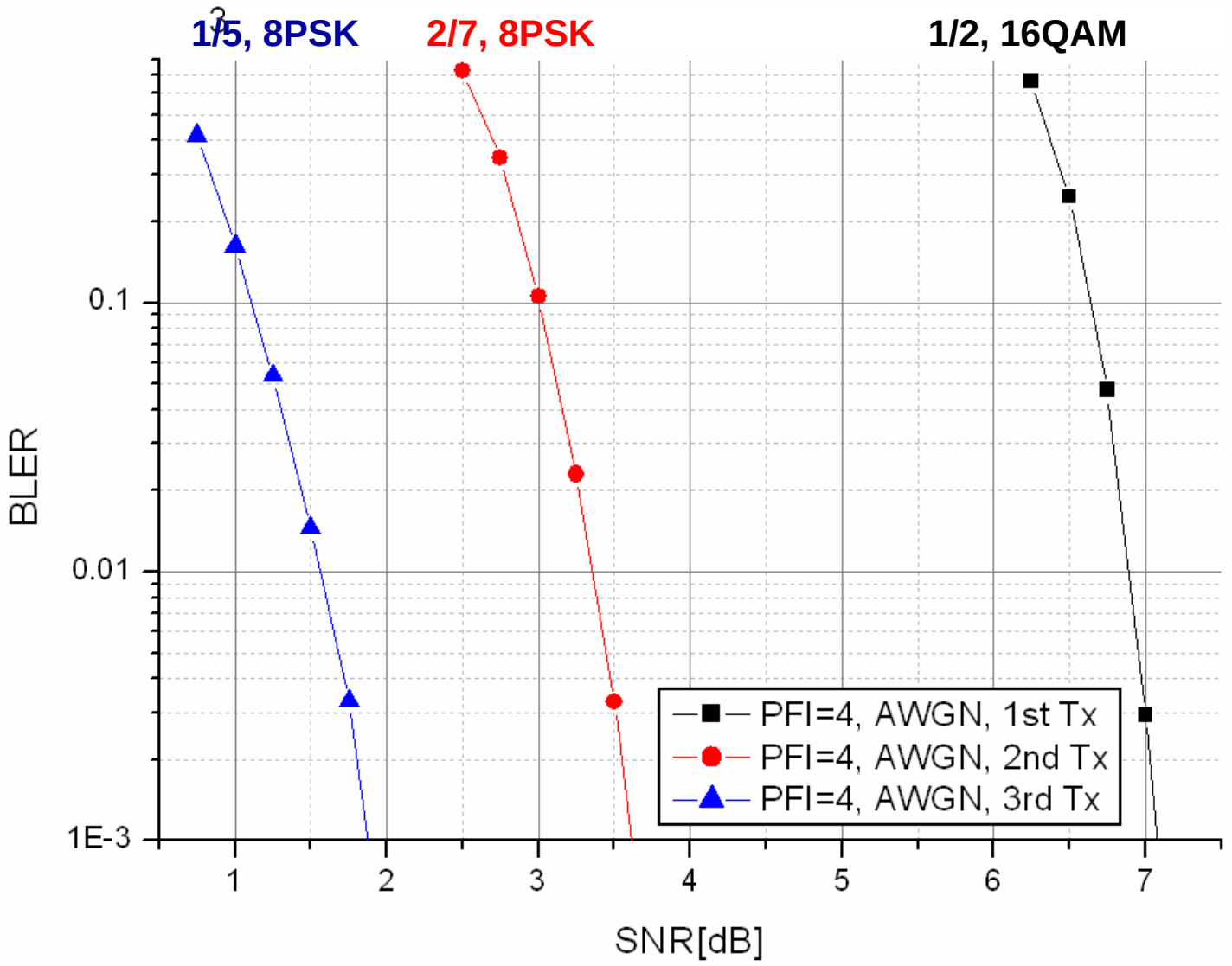
PFI 2, Iteration 25



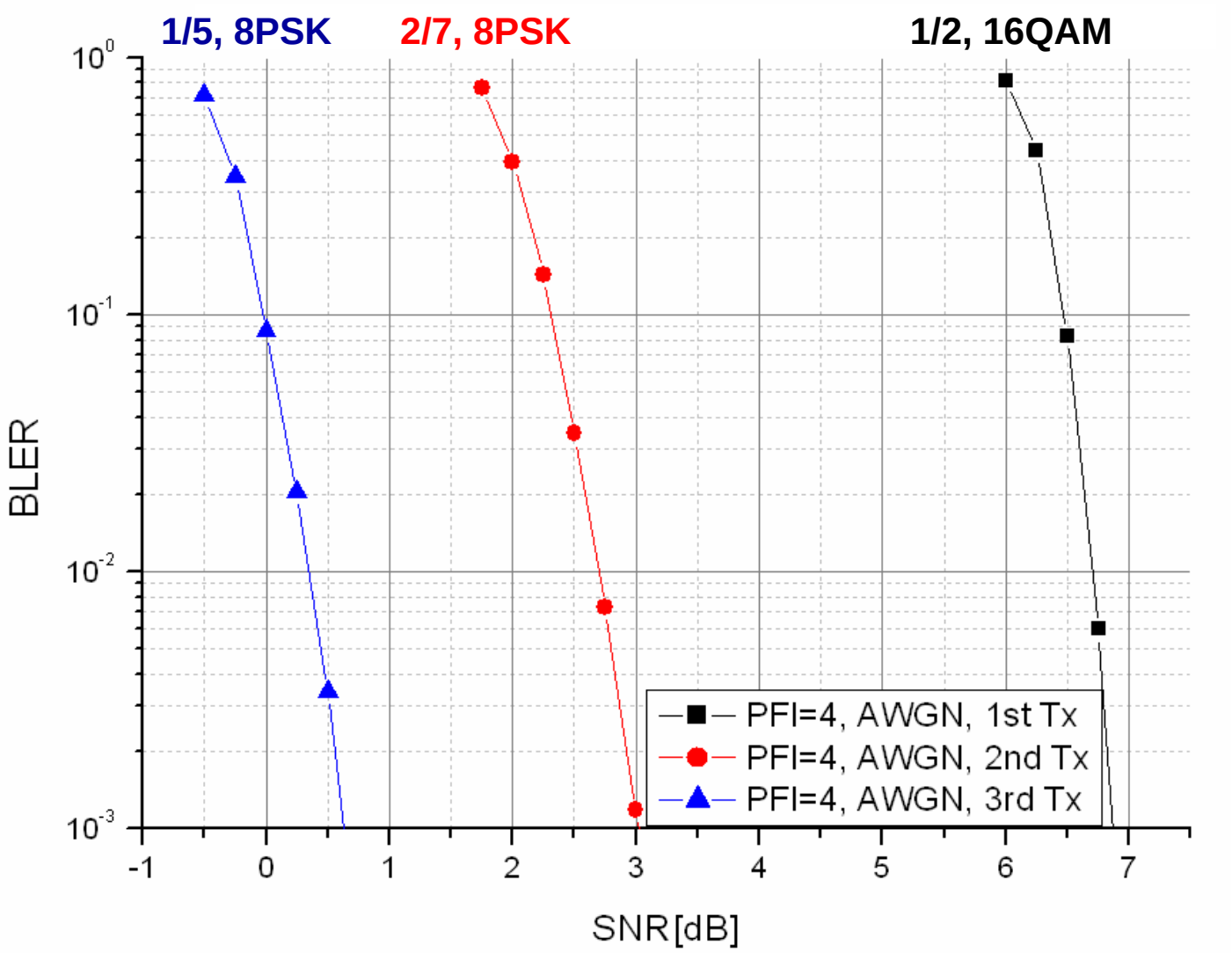
PFI 2, Iteration 50



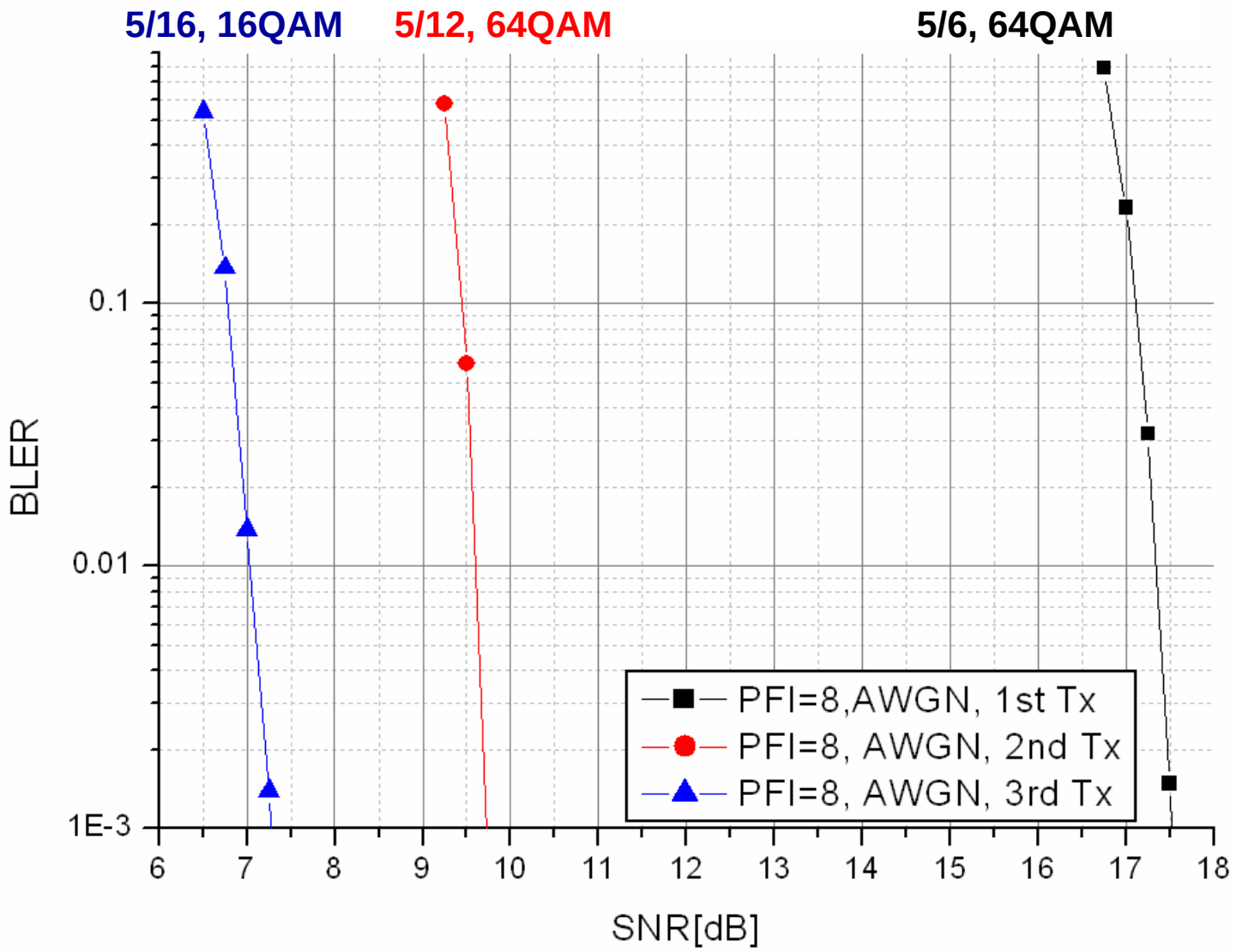
PFI 4, Iteration 25



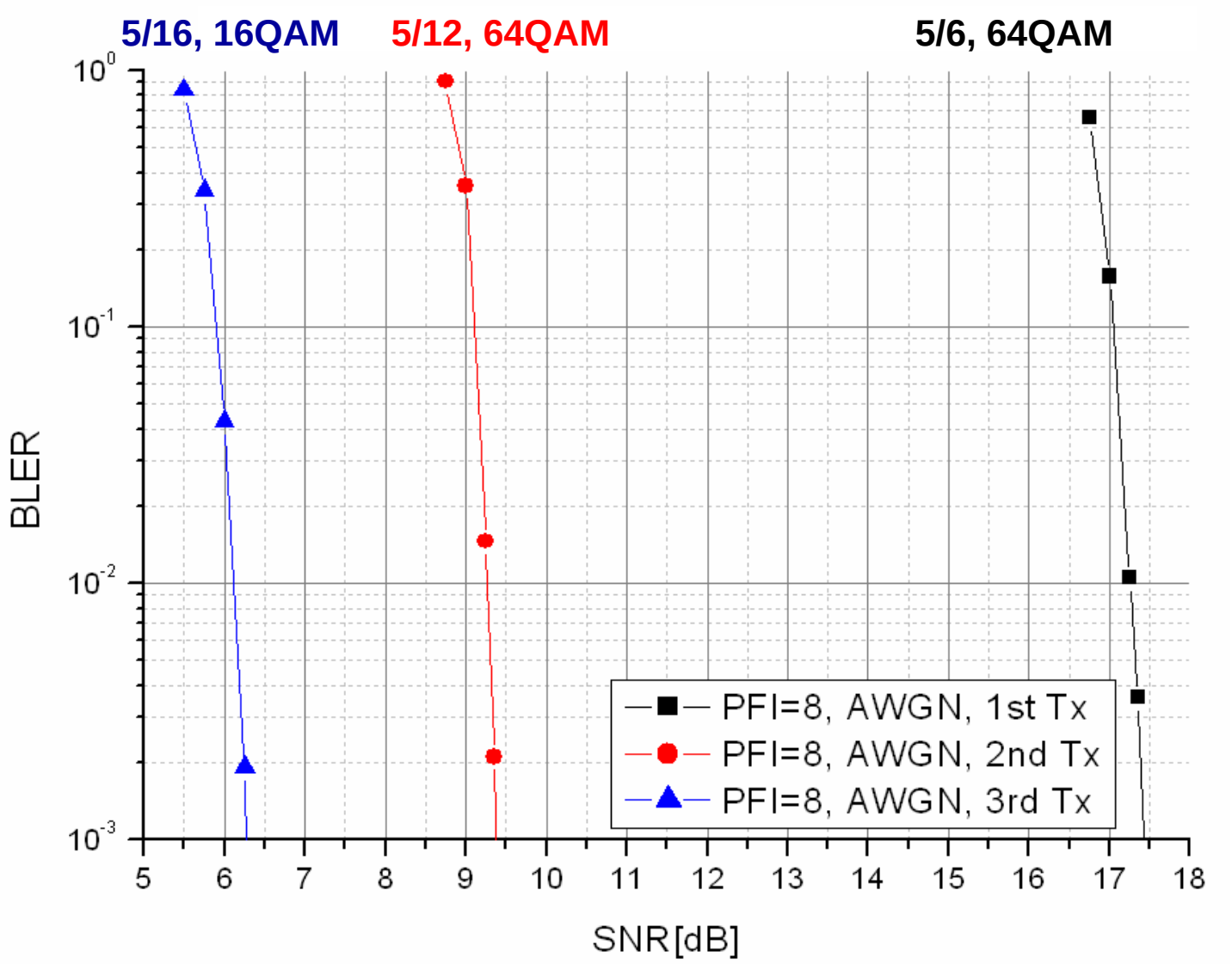
PFI 4, Iteration 50



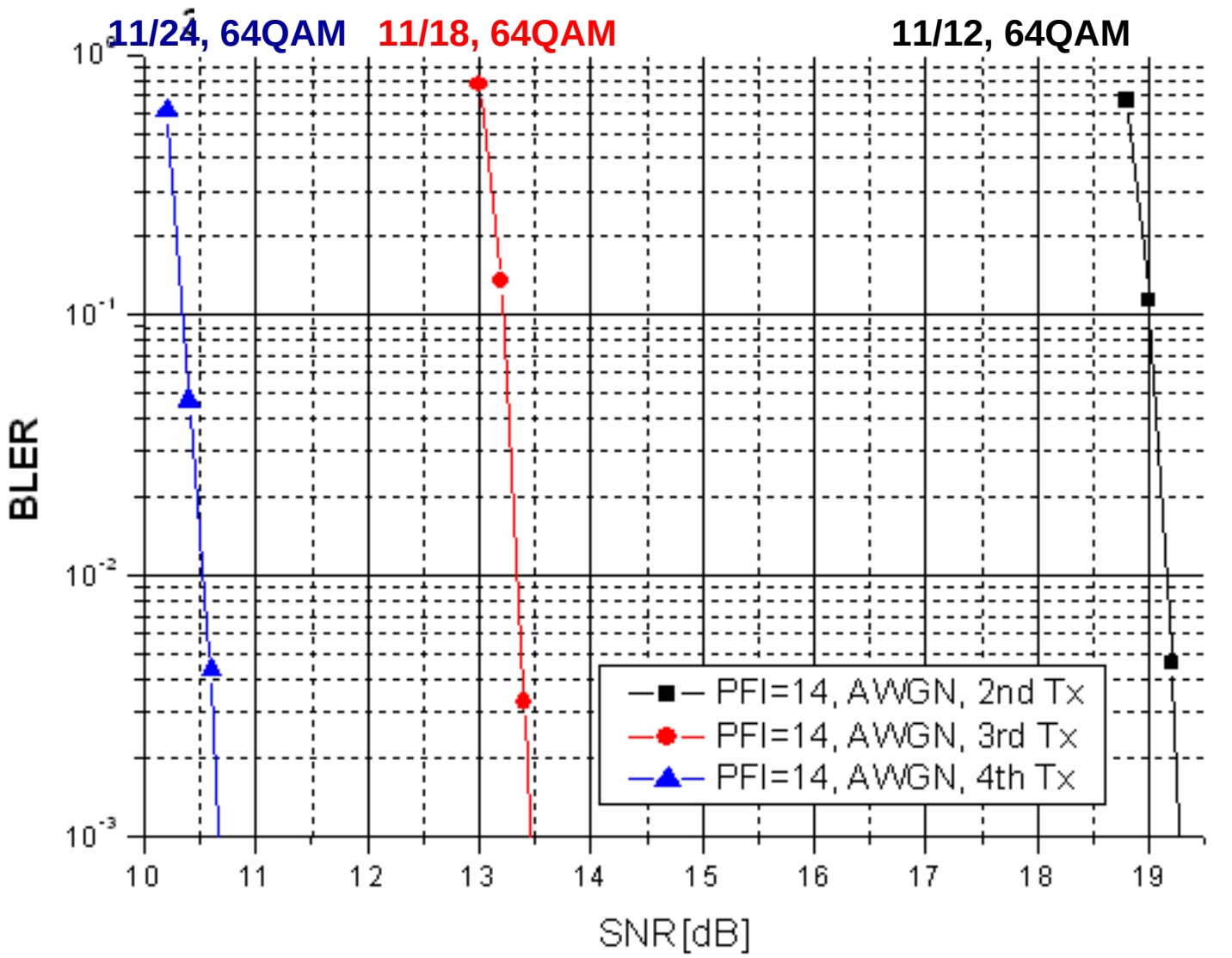
PFI 8, Iteration 25



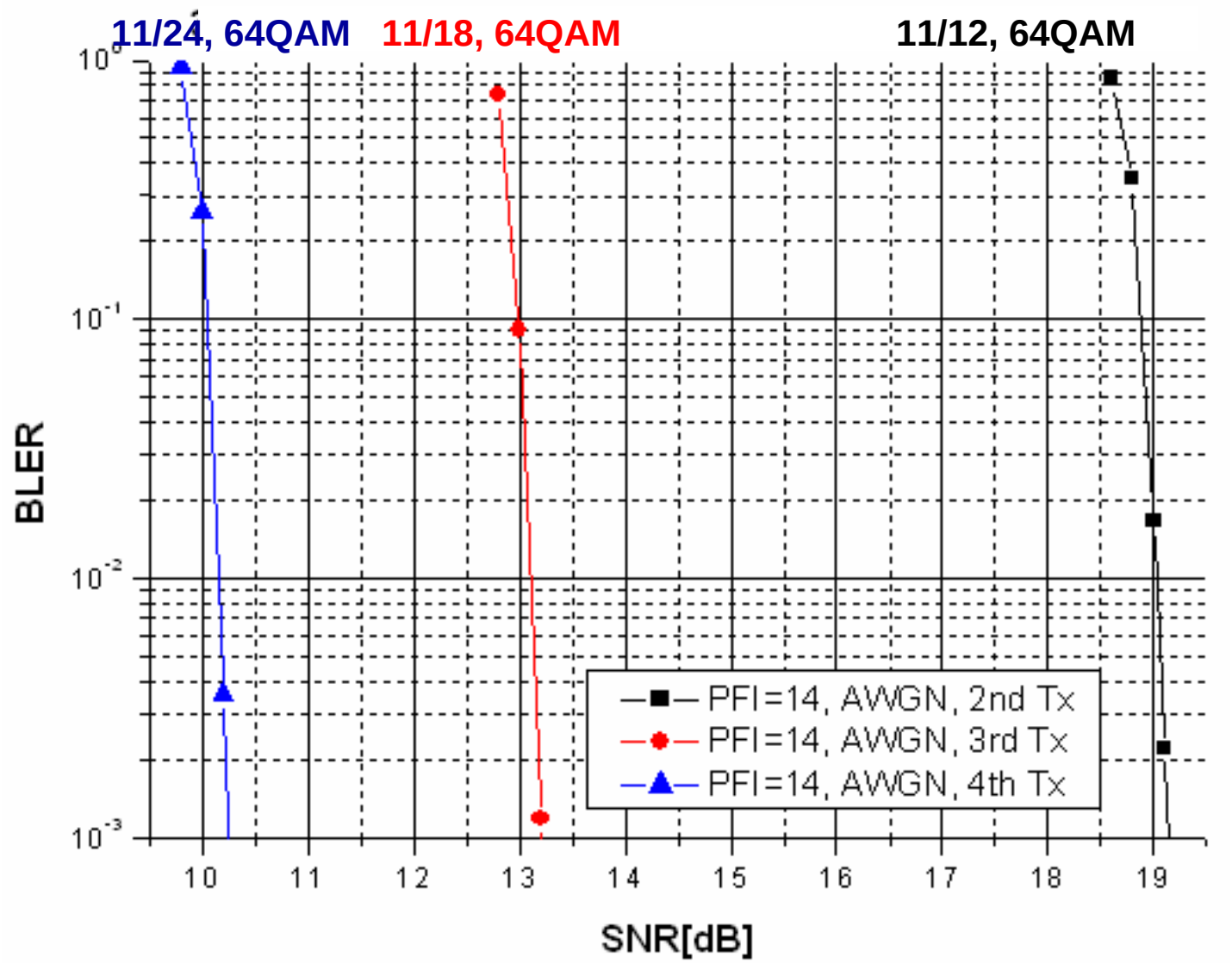
PFI 8, Iteration 50



PFI 14, Iteration 25



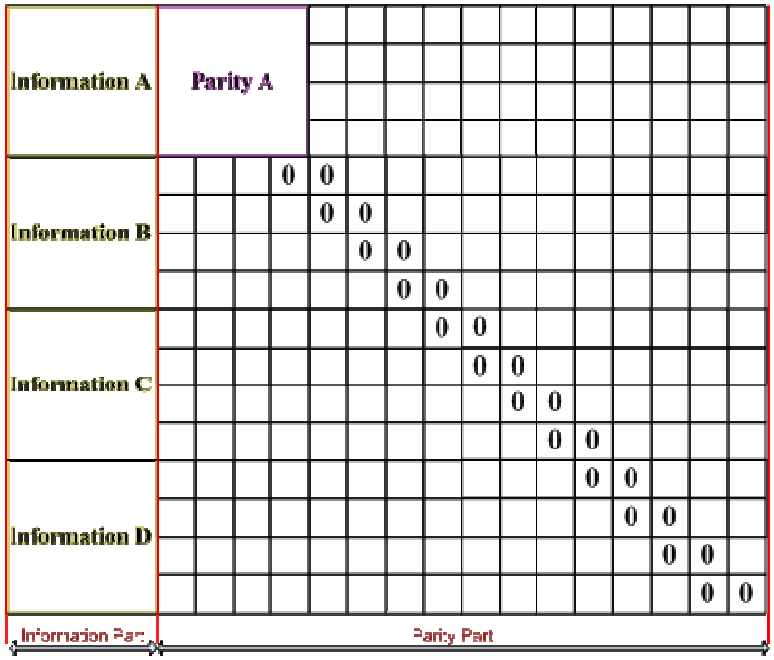
PFI 14, Iteration 50

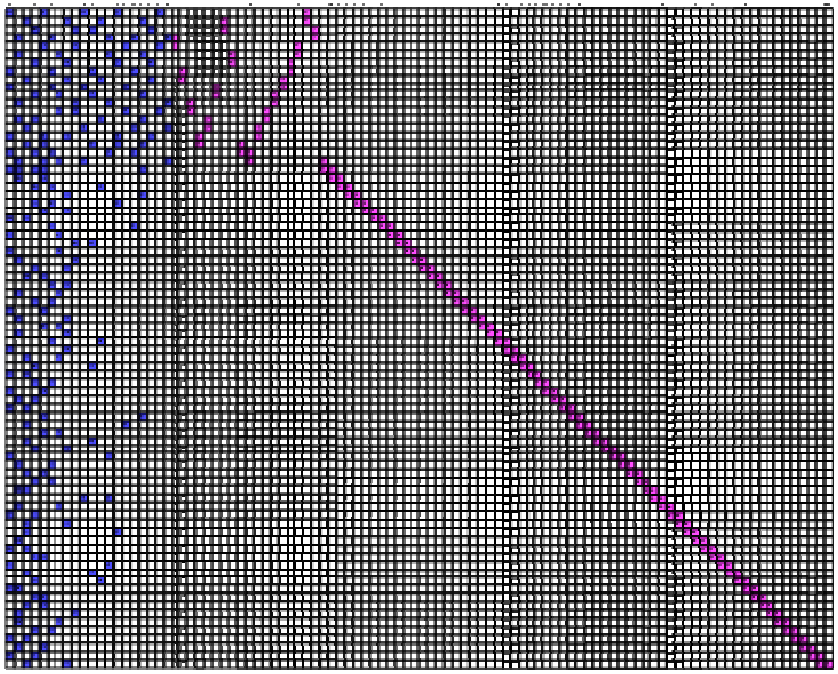


H matrix for simulation

One mother H matrix

- H matrix used for simulation will be added on this page, as agreed on LDPC AdHoc meeting.
- Right figure is the practical mother H matrix.
- Left figure represents Right figure.





One mother H matrix (2/4)

- Information A

1	40				36					224				328					20	
2			488					340				232					232			
3				404					500		484							424		
4		328				408							96			276				80
5					296				124						28				92	
6		308					472						52				52			
7				244				360						20				360		
8	148					456					344					188				
9			212					96				336						48		
10	20					416				416					428					
11				104			24				144						164			
12		216							464				128							428
13							48		236						344				300	
14		172		196								56					328			
15			184							240						428				488
16	152				0			284						200				508		
17			8		208						432			488			360			
18	380			76		456							72			168				
19		28			304		172			228										176
20	128	504		324	208												508			

- Information B

21		416			160															
22				416		160						124								
23								352									180			
24				96		432								100						
25					360			296												
26	400		96																	
27						152											72			
28	108						24													
29								416		180										
30	80						480													
31		228							96											
32				68				68												
33			440		372															
34						496		208												
35		372					368													
36				288		212														
37	284				72															
38		120						64												
39					468		456													
40		100						480												

One mother H matrix (3/4)

- Information C

41						72						160							
42	372							360											
43			136				36												
44				420							328								
45	84		484																
46				324		308													
47	212				80														
48		216		176															
49	56		300																
50					164												380		
51			380												256				
52					340		96												
53			508								364								
54				228				104											
55	192												508						
56		124				224													
57			108		360														
58				340		376													
59		400	332																
60										200			64						

- Information D

61		240					340												
62	68			328															
63			492					52											
64			180											180					
65		480			296														
66	16		384																
67				32	176														
68	72												244						
69			160							196									
70			316	76															
71	104	488																	
72				64	144														
73			168		336														
74		256						496											
75	308					152													

One mother H matrix (4/4)

- **Parity A**

21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
																52			
						468										52			
						468											12		
0																	12		
0															388				
							452								388				
							452							308					
	0													308					
	0												124						
					476								124						
					476							396							
		0										396							
		0									16								
				508							16								
				508						204									
			0							204									
			0					0											
								0	0										
									0									0	
																		0	0

Result of row combining

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
1	40				36					224				328					20																			52			
2			488					340			232						232									468											52			
3				404					500		484							424									468												12		
4		328				408							96			276				80	0																		12		
5					296				124						28				92		0																	388			
6		308					472						52				52											452									388			
7				244				360						20				360										452								308				
8	148					456					344					188						0													308					
9			212					96				336						48				0												124						
10	20					416				416				428											476									124						
11				104			24				144						164								476								396							
12		216							464				128							428			0										396							
13							48		236						344				300				0									16								
14		172		196								56					328							508							16								
15			184							240						428				488				508								204								
16	152				0			284						200				508					0								204								
17			8		208						432			488				360					0					0												
18	380			76		456						72			168													0	0										
19		28			304		172			228										176									0									0	
20	128	504		324	208												508																				0	0

Row Combining

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	40	328	488	404	36	408		340	500	224	484	232	96	328		276	232	424	20	80	0			
2	148	308		244	296	456	472	360	124		344		52	20	28	188	52	360	92		0	0		
3	20	216	212	104		416	24	96	464	416	144	336	128		428		164	48		428		0	0	
4	152	172	184	196	0		48	284	236	240		56		200	344	428	328	508	300	488			0	0

Conclusion

- F-LDPC Codes with simple encoding and decoding
  - » **Dual-Diagonal Parity Structure**
  - » **Matrix Dividing and Row Combining**
    - Reducing rows and columns in H matrix for supporting Higher code rate
- LDPC Codes fulfill the requirement of IEEE802.20 in terms of…
  - » **Performance** – higher coding gain at higher code rate
  - » **Throughput** – parallel decoding structure enables high decoding throughput without performance degradation.
  - » **Complexity** – lower decoding complexity
- Proposed LDPC Codes supports H-ARQ scheme, both IR and CC
- F-LDPC Codes can be considered an channel coding scheme in IEEE802.20.

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Annex

Encoding Method for LDPCC

Size adaptation

Notation

- R : Code rate. $R = K/N$ in general; $R = (n_b - m_b)/n_b$ for LDPC;
- N : Number of codeword bits in a block; $N = n_b \times z$ for LDPC;
- K : Number of information bits in a block; $K = (n_b - m_b) \times z$ for LDPC;
- M : Number of parity bits in a block; $M = m_b \times z$ for LDPC;
- m_b : Number of rows in the base matrix of the LDPC code;
- n_b : Number of columns in the base matrix of the LDPC code;
- k_b : Number of information in the base matrix of the LDPC code;
- z : Expansion factor of the LDPC code;
- d_v : Average column weight of the LDPC code;
- d_c : Average row weight of the LDPC code;
- $d_{v,max}$: Largest column weight of the LDPC code;
- W : Base matrix weight ($W = Nd_v = Md_c$);

Encoding Method for LDPC(1/2)

- Encoding
  - » the process of determining the parity sequence **p** given an information sequence **s**
- To encode…
  - » **s** is divided into $k_b = n_b - m_b$ groups of z bits
  - » Let this grouped **s** be denoted **u**, $u = [u(0)u(1)\ldots u(k_b - 1)]^T$
  - » where each element of **u** is a column vector, $u(i) = [s_{iz}\, s_{iz+1} \ldots s_{(i+1)z-1}]^T$
  - » Using the **H** matrix, the parity sequence **p** is determined in groups of z. Let the grouped parity sequence **p** by denoted **v**,

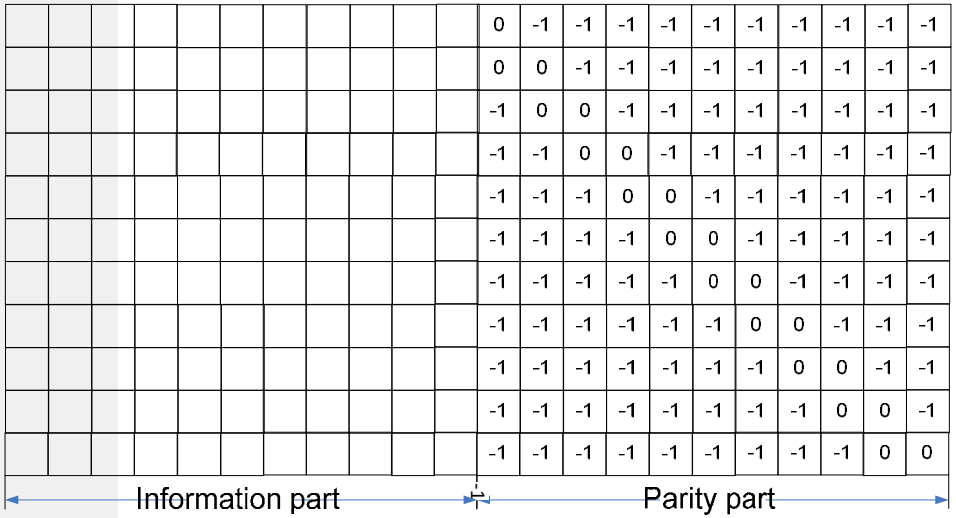
$$v = [v(0)v(1)\ldots v(m_b - 1)]^T$$

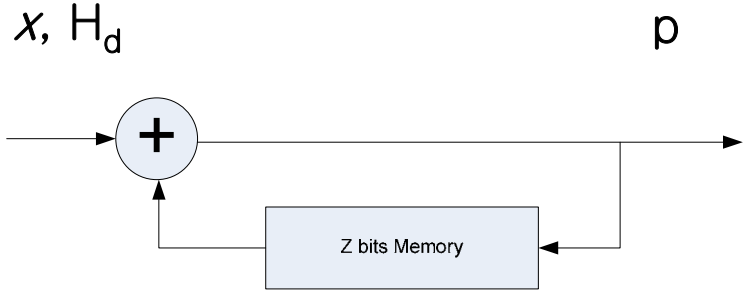
  - » where each element of **v** is a column vector,

$$v(i) = [p_{iz}\, p_{iz+1} \cdots p_{(i+1)z-1}]^T$$

Encoding Method for LDPC(2/2)

- Parity blocks are generated successively
  - » $v(0) = \sum_{j=0}^{k_b - 1} \left(P_{p(0,j)} u(j) \right)$
  - » $v(i) = \sum_{j=0}^{i} \left(P_{p(i,k_b+j)} v(j) \right) + \sum_{j=0}^{k_b - 1} \left(P_{p(i,j)} u(j) \right) \qquad i = 1, \cdots, m_b - 1$
  - » $P_{p(i,j)}$: shifted version of identity matrix





Size Adaptation(1/2)

- With ONE H matrix, various sizes of codeword are supported.
- Scaling and Expansion
  - » Step 1 : derive a shift number for a codeword size by scaling

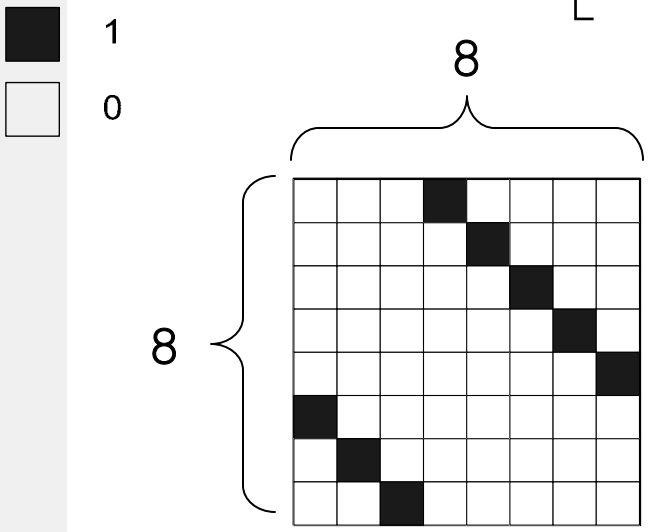
$$p(f,i,j) = \begin{cases} p(i,j), & p(i,j) \le 0 \\ \left\lfloor \dfrac{p(i,j) z_f}{z_0} \right\rfloor, & p(i,j) > 0 \end{cases}$$

  - » Step 2 : expand sub-matrix and shift the columns

Size Adaptation(2/2)

- Example (p(i,j)=10, z_f=8, z_0=24)
  - » p(i,j) : The shift number for original sub-matrix
  - » z_0 : The size of original sub-matrix
  - » z_f : The size of target sub-matrix
  - » The shift number for target sub-matrix

$$p(f,i,j) = \left\lfloor \frac{p(i,j)z_f}{z_0} \right\rfloor = \left\lfloor \frac{10 \times 8}{24} \right\rfloor = \lfloor 3.\dot{3} \rfloor = 3$$



Sub-matrix = 8x8 identity matrix

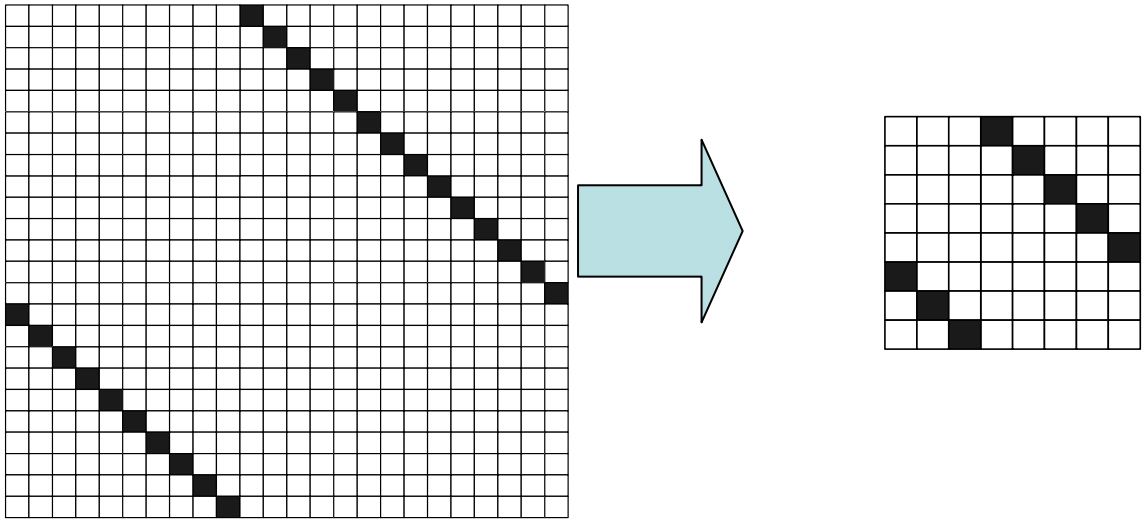
Shift the identity matrix by 3

3

Size Adaptation(2/2)

- Example (p(i,j)=10, z_f=8, z_0=24)
  - » p(i,j) : The shift number for original sub-matrix
  - » z_0 : The size of original sub-matrix
  - » z_f : The size of target sub-matrix

24x24 matrix is changed to 8x8 matrix



Comparisons between TC and LDPC

Computational Complexity

Memory Requirement

Decoding Throughput

Link Performance

Parameters for comparison

	TC	LDPC
Decoding Algorithm	MAX-LOG-MAP	Layered Offset-MIN SUM
Computational Complexity	Forward & Backward State Metric	Message Passing
Number of Iteration (NI)	8	20
Mother Code Rate	1/5, 1/3	1/5 ~ 1
Channel / Modulation	AWGN / QPSK	

Computational Complexity

- LDPC
  - » The amount of computation is proportional to K (size of information) and the size of H matrix

Code Rate	1/3	1/2	2/3	3/4
H matrix size	40x60	20x40	10x30	7x27
Computation/iteration	51K	27.6K	19.9K	15.3K
Avg. Column degree	4.08	3.73	3.23	2.81

- TC
  - » The amount of computation for TC is proportional to K regardless of code rate
- Comparison

Code Rate	1/3	1/2	2/3	3/4
Turbo codes	166K * 8= 1,328K			
LDPC codes	51K *20 = 1,020K	27.6K *20 = 552K	19.9K * 20= 398K	15.3K *20= 306K
LDPC/TC	77%	42%	30%	23%

Memory Requirement

- Comparison

Code Rate	1/3	1/2	2/3	3/4
LDPCC	18.24K	11.46K	7.85K	6.41K
TC	4K+8W	4K+8W	4K+8W	4K+8W
LDPCC/TC	4.5	2.8	1.9	1.6

  - » K : size of information
  - » W : size of sliding window for TC (32 or 64)

Decoding Throughput

- LDPC

$$F_{dec} = \frac{F_{\text{int}} \cdot K}{NI \cdot (z/l) + 1} = \frac{F_{\text{int}} \cdot (n_b - m_b) \cdot l}{20 + l/z} = \frac{100 \cdot k_b \cdot l}{20 + (l/z)} \approx 5 k_b l$$

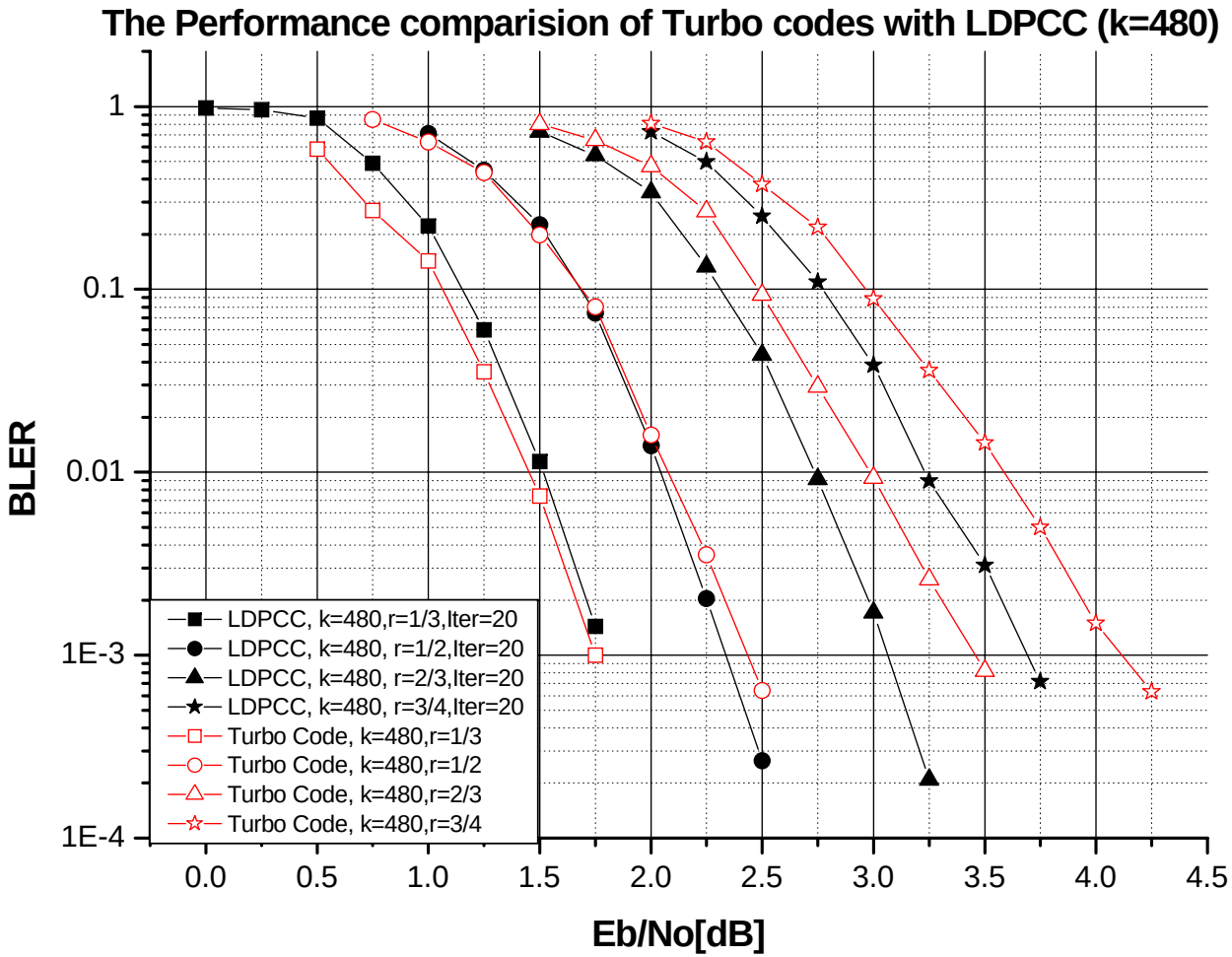
  - / : parallel factor
  - *NI* : the number of iteration
  - F_{int} : internal clock rate
  - F_{dec} : the information data throughput

- Throughput comparison between LDPCC and TC
  - » (code-rate=1/3, F_{int} = 100MHz)

	LDPCC	TC
Throughput	100 Mbps	6.17 Mbps

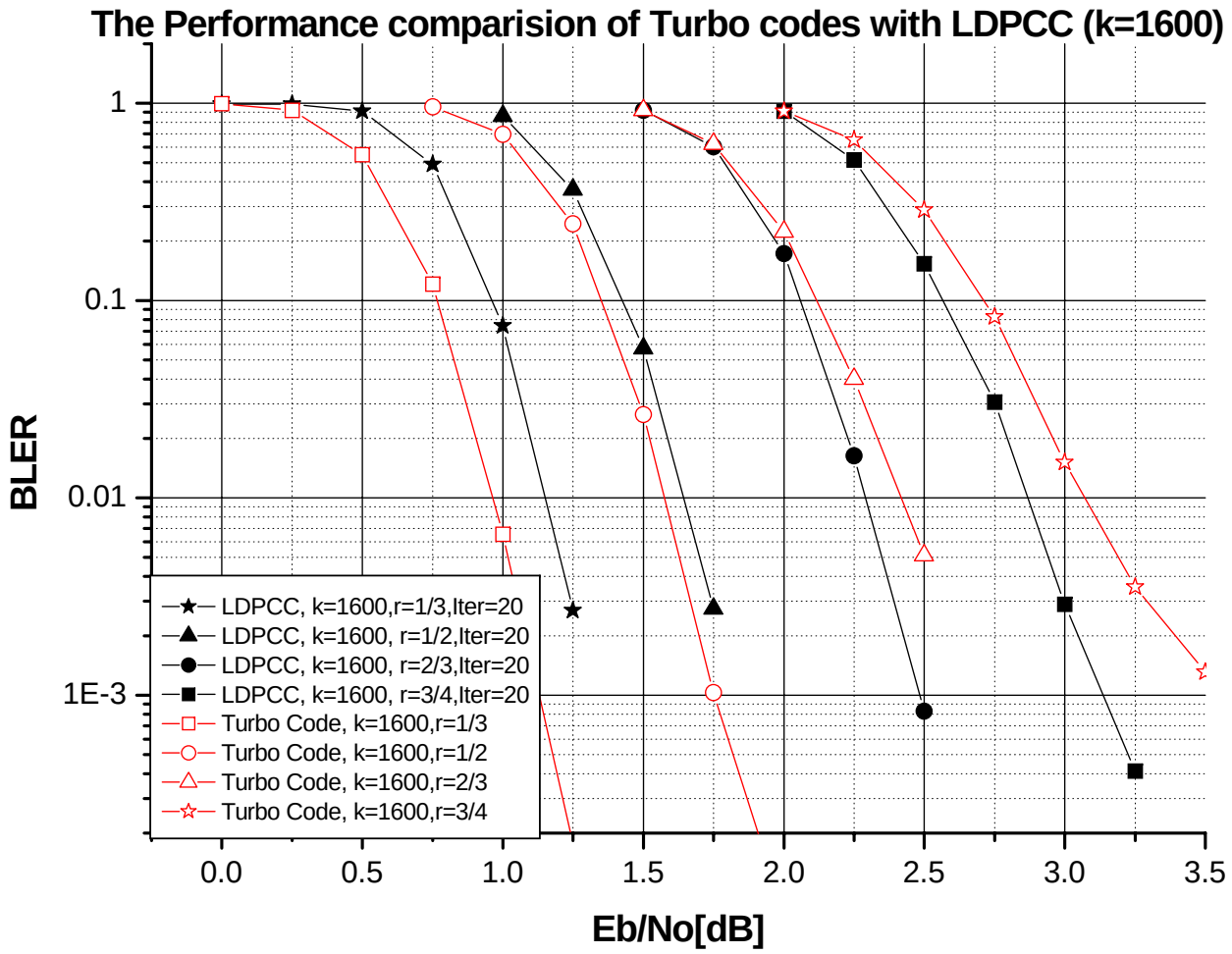
Link Simulation

- K = 480



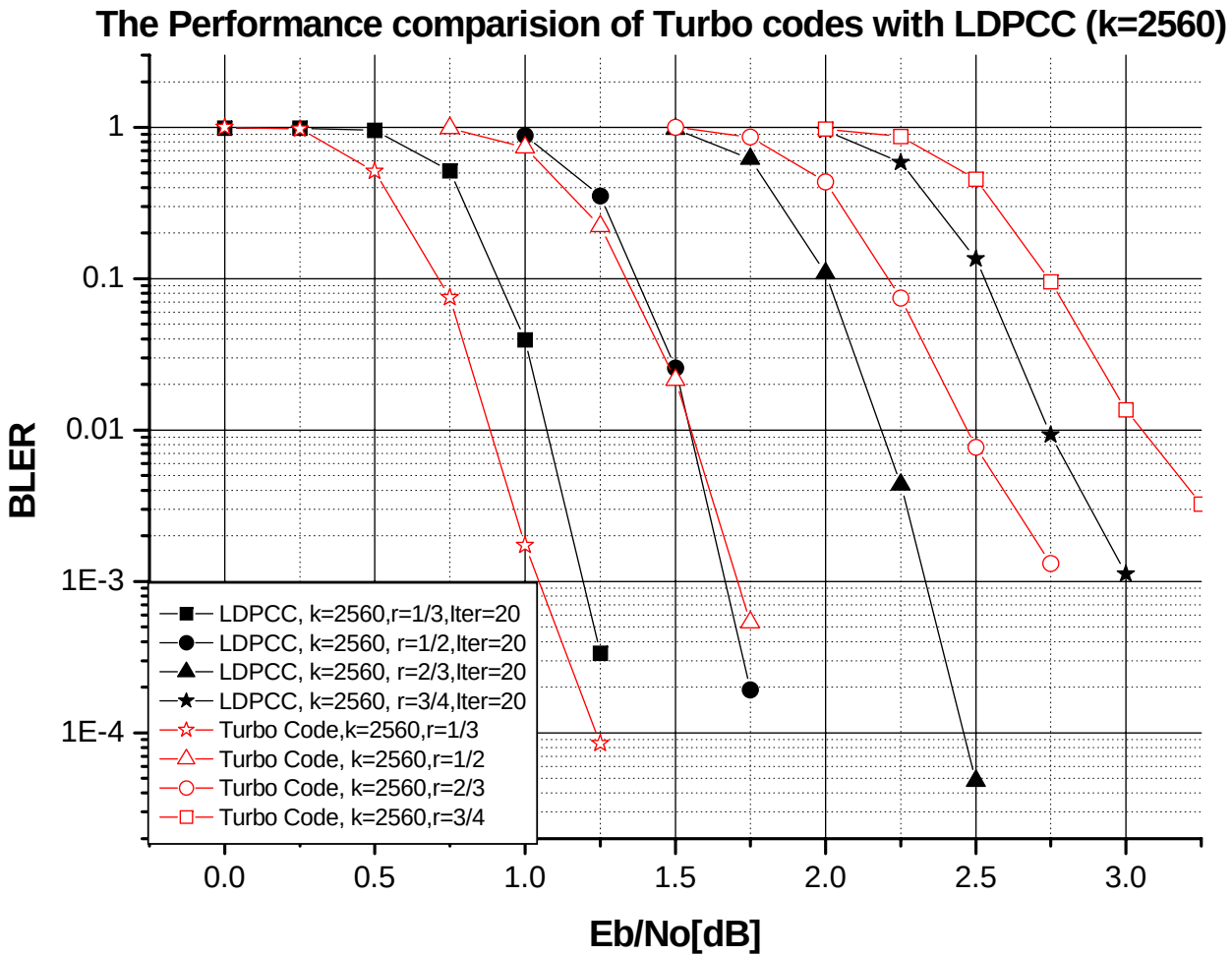
Link Simulation

- K = 1600

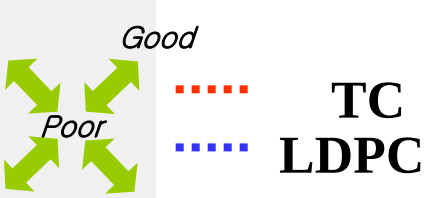


Link Simulation

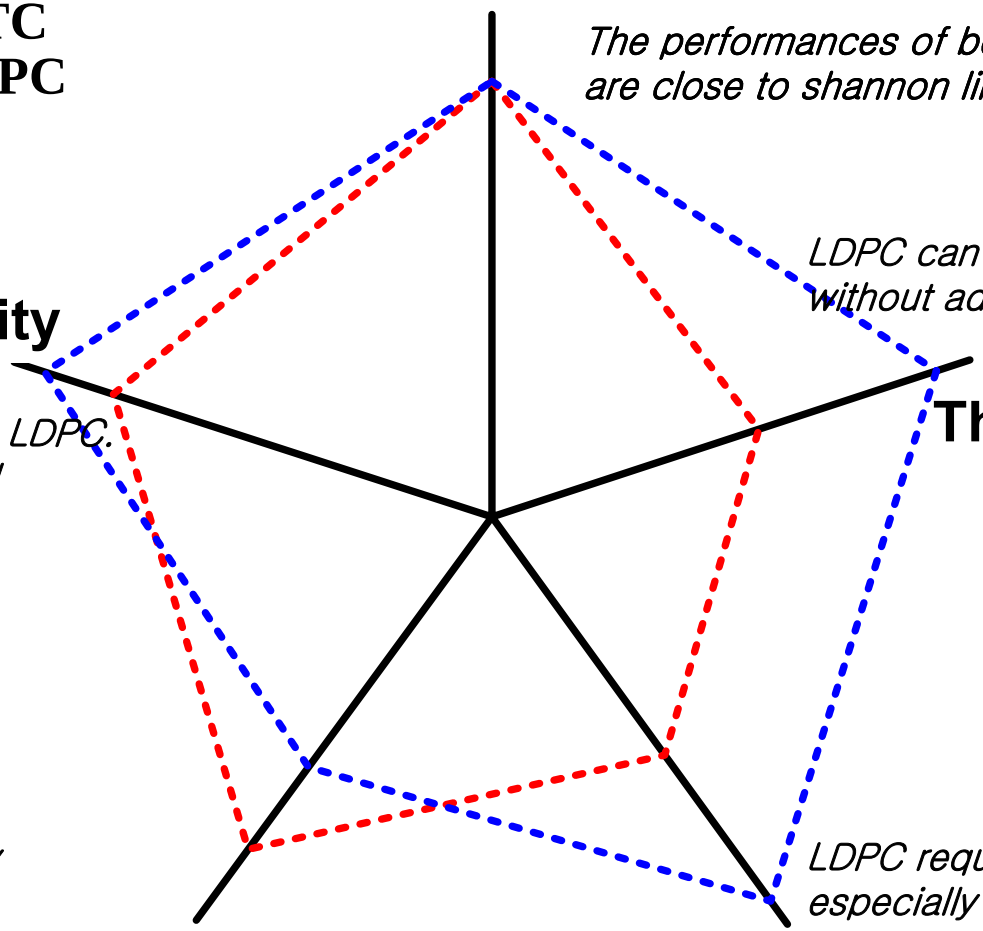
- K = 2560



Overall Comparison



TC
LDPC



The performances of both channel coding schemes are close to shannon limit.

LDPC can achieve more than100Mbps without additional complexity.

No CRC, No tail bits in LDPC. LDPC supports parallel processing structure.

TC needs less memory at lower code rate.

LDPC requires less computations especially at higher code rate.

MIMO - Space Time Transmit Diversity (STTD) + Antenna Selection

MIMO Design Objectives

- To design MIMO-OFDM / MC-CDMA transmission architectures that efficiently combines multi-carrier operations with multiple transmit antenna configurations
- To try to utilize the resources in time, frequency, and spatial domains efficiently in order to maximize the throughput and/or coverage
- To reduce the receiver (AT) complexity to generate feedback information
- To support a wide range of user mobility
- Relates to Section 9.3.2.3 “Multiple Antennas”
  - » Could be added as a new section before Section 9.3.2.6.4.3 “MIMO MCW mode”

Assumptions

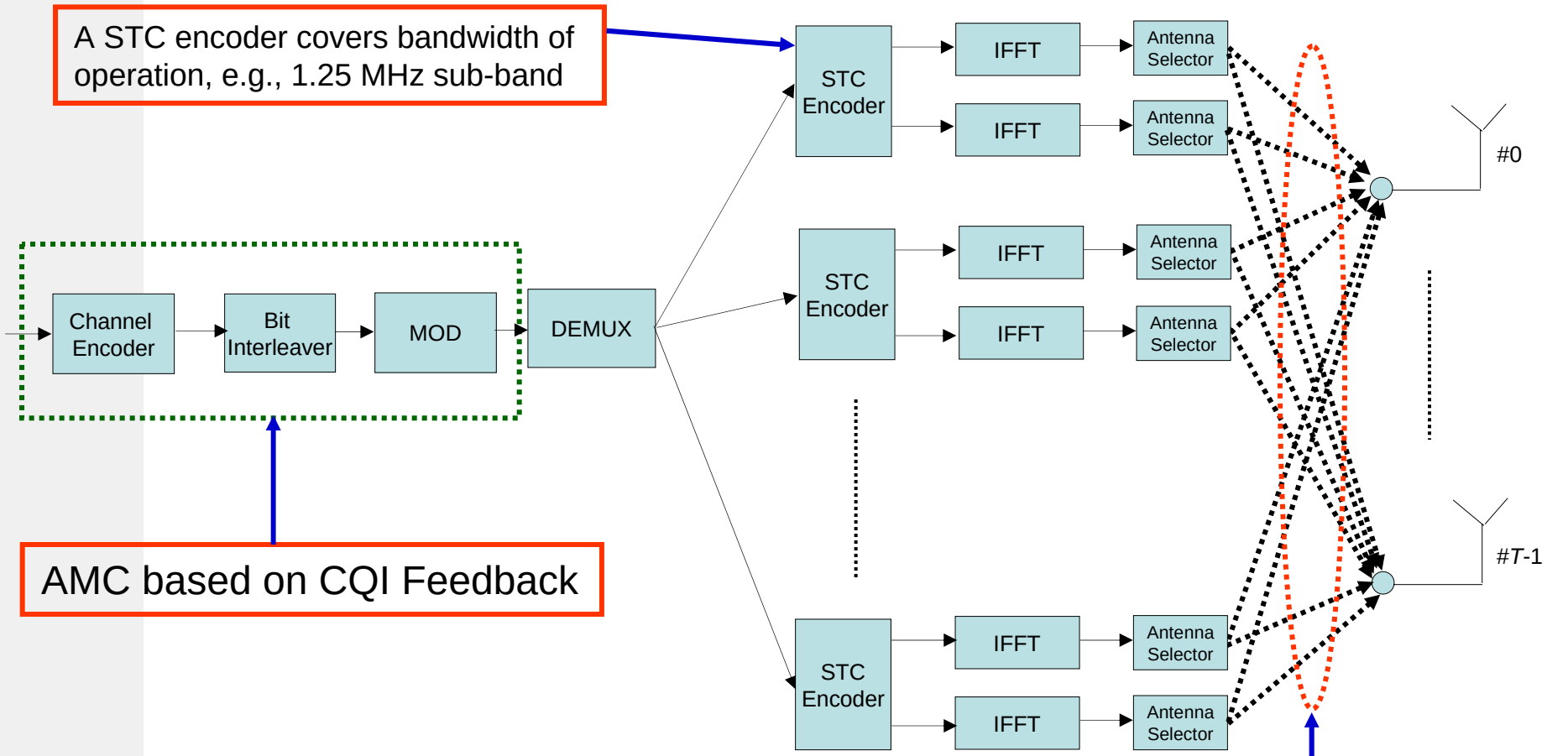
- Downlink High-Speed Packet Data Transmission
- Orthogonal Frequency Division Multiplexing
- Feedback is available → Closed loop operation
- Feedback is per unit bandwidth of operation, e.g., 1.25 MHz sub-band
- Number of transmit antennas (*T*) is greater than the output of the STC encoder
- Receiver (Access Terminal (AT)) is equipped with more than one antenna element to provide spatial multiplexing gain or additional diversity gain

Multiple Transmit Antenna Designs

- Transmit Diversity with Joint Antenna Selection
  - » Antenna Selection based on the feedback and Transmit Diversity applied over subset of antenna elements selected
  - » Antenna selection is dominant source of gain for low mobility and transmit diversity provides gain even for relatively high mobility in terms of received signal-to-interference-plus-noise (SINR)

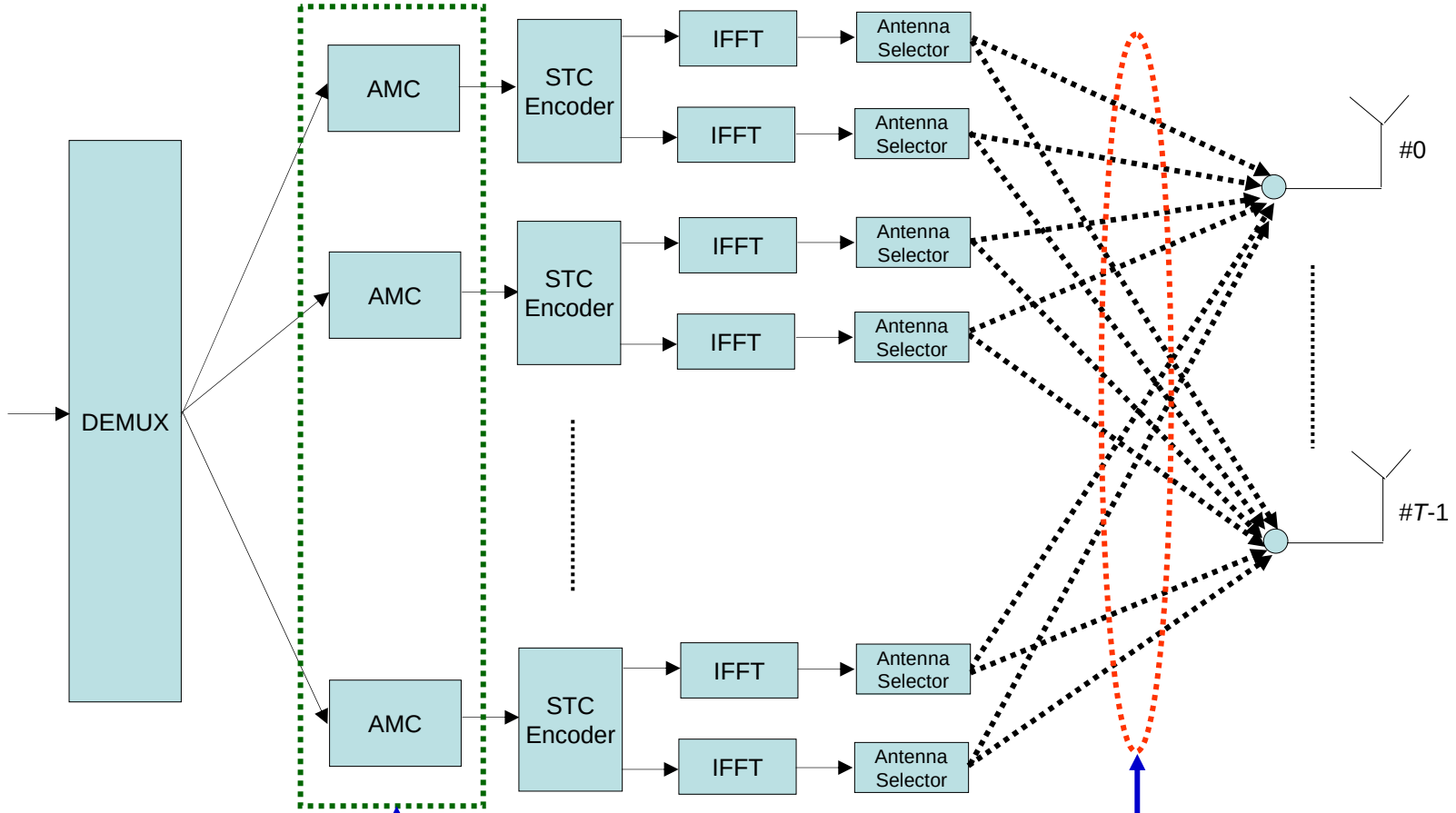
- Spatial Multiplexing with Joint Antenna Selection
  - » Antenna Selection based on the feedback and Spatial Multiplexing applied over subset of antenna elements selected to increase the transmit data rate
  - » Non-orthogonal Space Time Block Code (NO-STBC) is possible choice due to its simple implementation
  - » AT is required to equip with more than one antenna element

Transmit Diversity with Joint Antenna Selection – Architecture 1

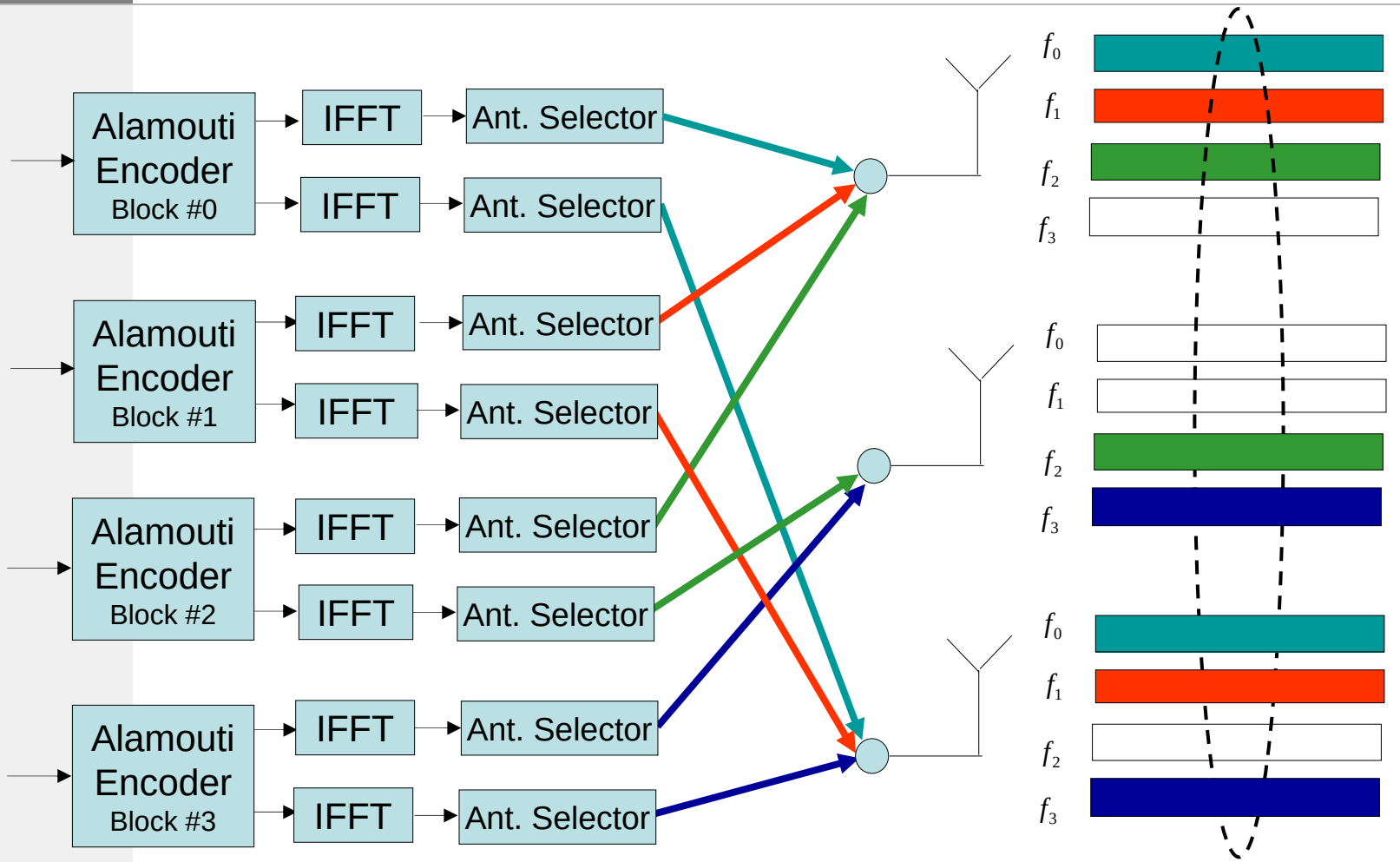


- **Note: If STC encoder is replaced with Non-orthogonal space time block code (NO-STBC) encoder, the same architecture is used as Spatial Multiplexing with Antenna Selection**

Transmit Diversity with Joint Antenna Selection – Architecture 2



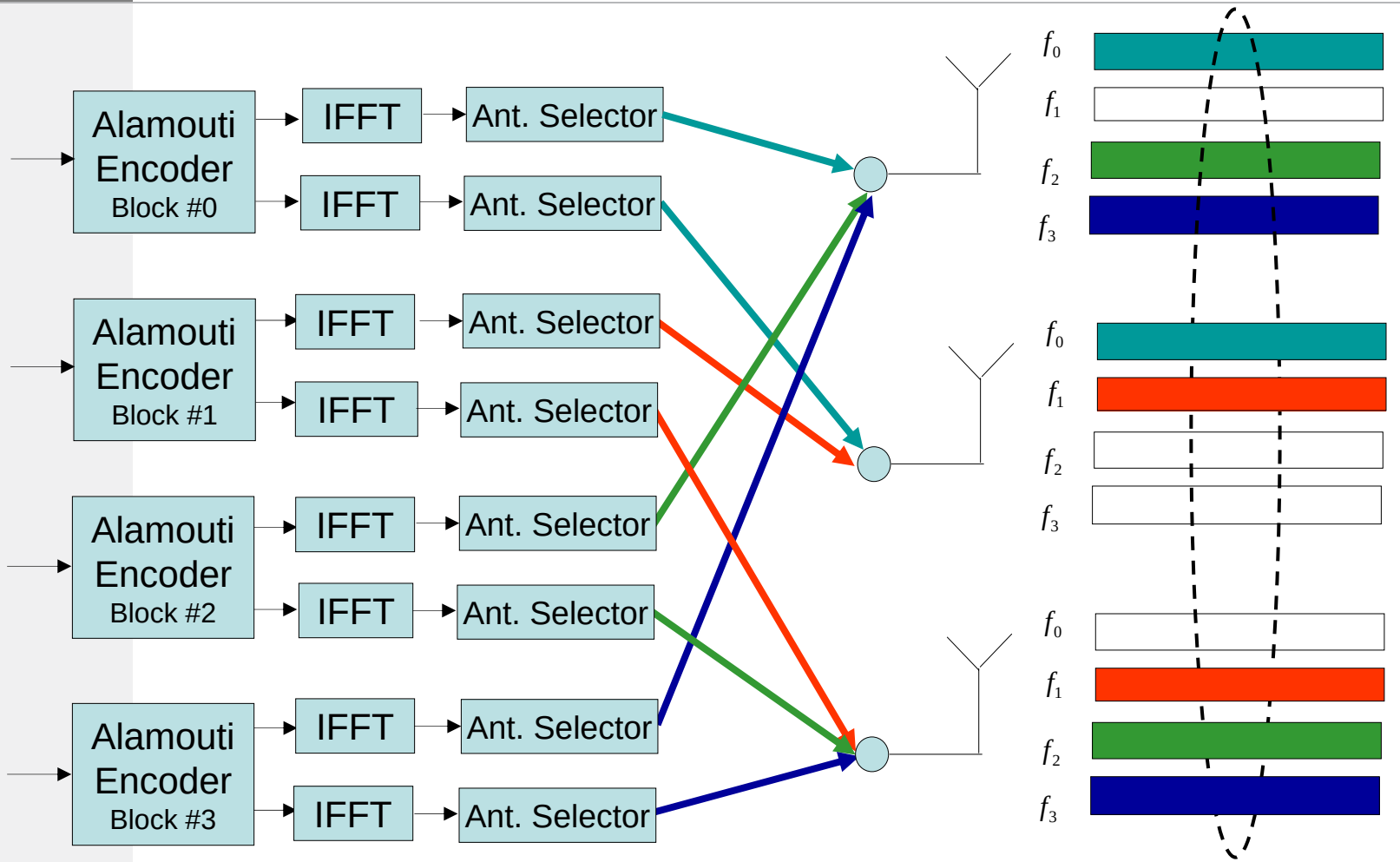
Example Operation 1/2



- **Example *N* = 4 (Bandwidth of Operation) & *T* = 3**

Frequency allocation is maintained at least two consecutive OFDM symbol intervals

Example Operation 2/2



- **Example *N* = 4 (Bandwidth of Operation) & *T* = 3**

Frequency allocation is maintained at least two consecutive OFDM symbol intervals

Transmit Diversity with Joint Antenna Selection (1/2)

- The number of transmit antennas is greater than the number of STC encoder outputs
- This can be considered as Antenna Selection + Transmit Diversity
- Feedback → (Sector ID, Carrier Index, Antenna Indices Selected, Average SINR Achievable, etc)
- Selected antenna indices may be transmitted using bitmap in control or overhead channels (or signaling)

Transmit Diversity with Joint Antenna Selection (2/2)

- How to measure the average SINR per transmit antenna combination?
  - » Pre-detection:
    - Insert antenna-specific known pilot sequence before OFDM block (TDM)
  - » Post-detection:
    - Use antenna specific common or dedicated pilot pattern in OFDM block
- What kind of information should be accompanied with the transmission?
  - » MAC Index for selected user, BW of operation (sub-band) Index, Antenna Indices, AMC Index, etc
  - » H-ARQ related information can be transmitted if the retransmissions uses different carriers or is asynchronous

Benefits

- Easily extends multicarrier operation to multiple antenna case
- Easy accommodation of adaptive operation based on the channel feedback
- Exploits multi-user diversity not only in time domain, but also in frequency and spatial domains

Interlace Switching

Interlace-Switching – Introduction

- We can support low-rate delay sensitive applications such as VoIP efficiently by
  - » Grouping such users based on certain criterion, e.g. channel conditions
  - » Assigning the group a set of time-frequency resources
  - » Using bitmap signaling to allocate resources in each application frame
- Interlace in the time domain is assigned to the group
- First subpacket transmission from an AT in the group is distributed over the interlace offset
  - » Distribution of traffic load
- Relates to:
  - » Section 6.4.6.3 “SelectedInterlaceRequest” and
  - » Section 6.4.6.4 “SelectedInterlaceAssignment”

Things to Ponder (1/2)

- In order to reflect variation of channel condition, e.g. due to mobility, we need to support the group change during VoIP call
  - » Ex: An AT was allocated to 16 QAM group due to its proximity to the center of the cell, but it escapes away to the edge of the cell
  - » We need to assign it to a group supporting robust modulation, e.g. QPSK
- In order to support efficient utilization of traffic resources we need to support interlace offset change during VoIP call even within a subgroup

Things to Ponder (2/2)

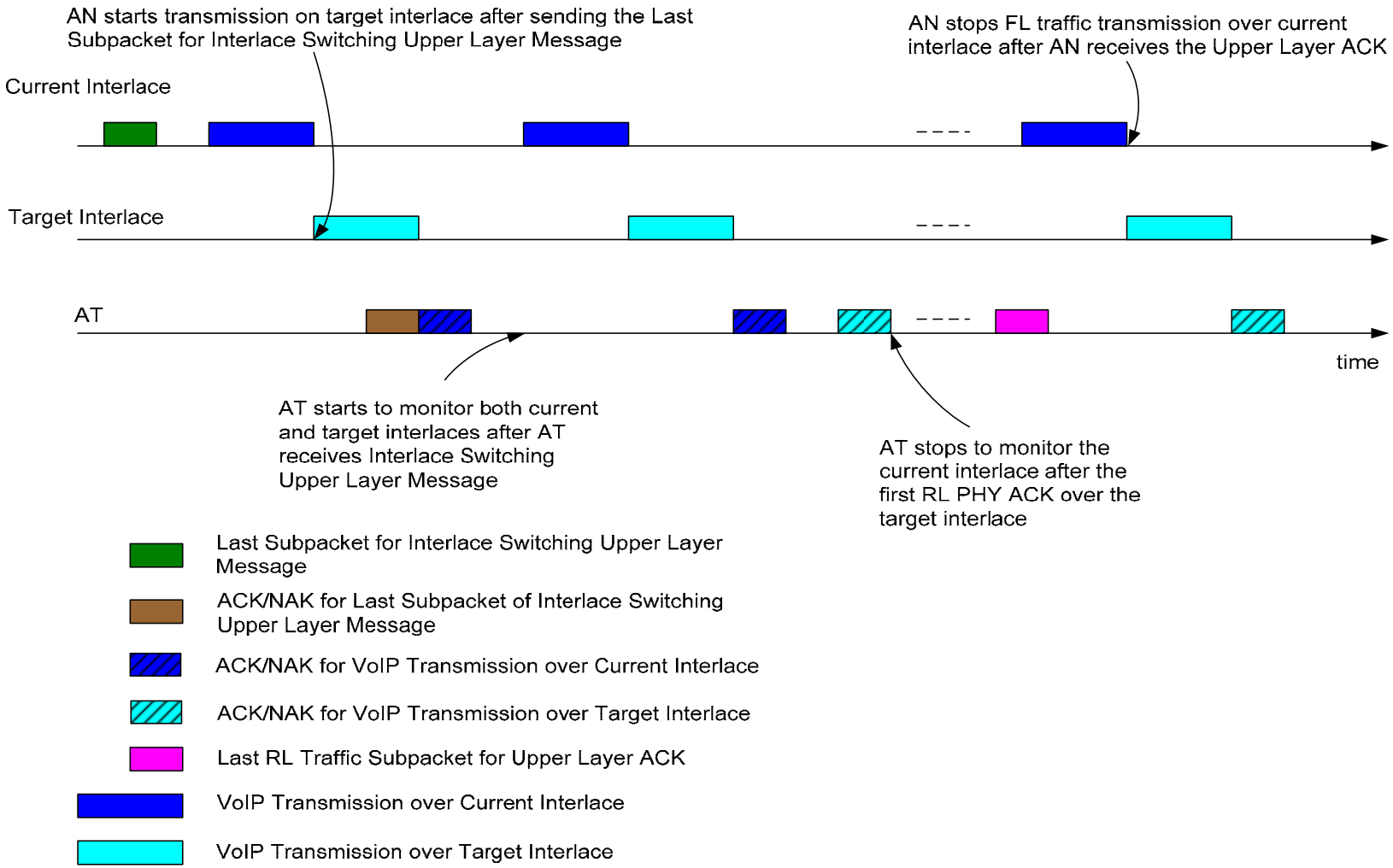
- Initially the transmission from ATs in a group was distributed over the interlace offsets → Load Balancing
- Due to the nature of voice calls some interlace offsets will be lightly loaded and some will not as time goes on
- Best effort traffic and/or other VoIP traffic (new or on-going) can be assigned to lightly loaded interlace offsets
- We focus on the reassignment of on-going VoIP traffic in an interlace offset to different offset

- We propose here:
  - Interlace Switching
  - Interlace Offset Switching
  - Both are intended for efficient resource utilization and load balancing

Approach 1 (1/2)

- This approach is mainly intended for interlace switching with the same or different interlace offset
- Transmission over the current and target interlaces and interlace offsets:
  - When the group setup message is transmitted for the purpose of interlace switching, the same VoIP traffic (subpacket) is transmitted over the current and target interlaces/interlace offsets.
  - AT can combine both transmissions and send “ACK” or “NACK” for the purpose of physical layer H-ARQ over the current interlace/offset.
  - After upper layer “ACK” is received at AN, the VoIP traffic is transmitted only over the target interlace/offset.

Approach 1 (2/2)

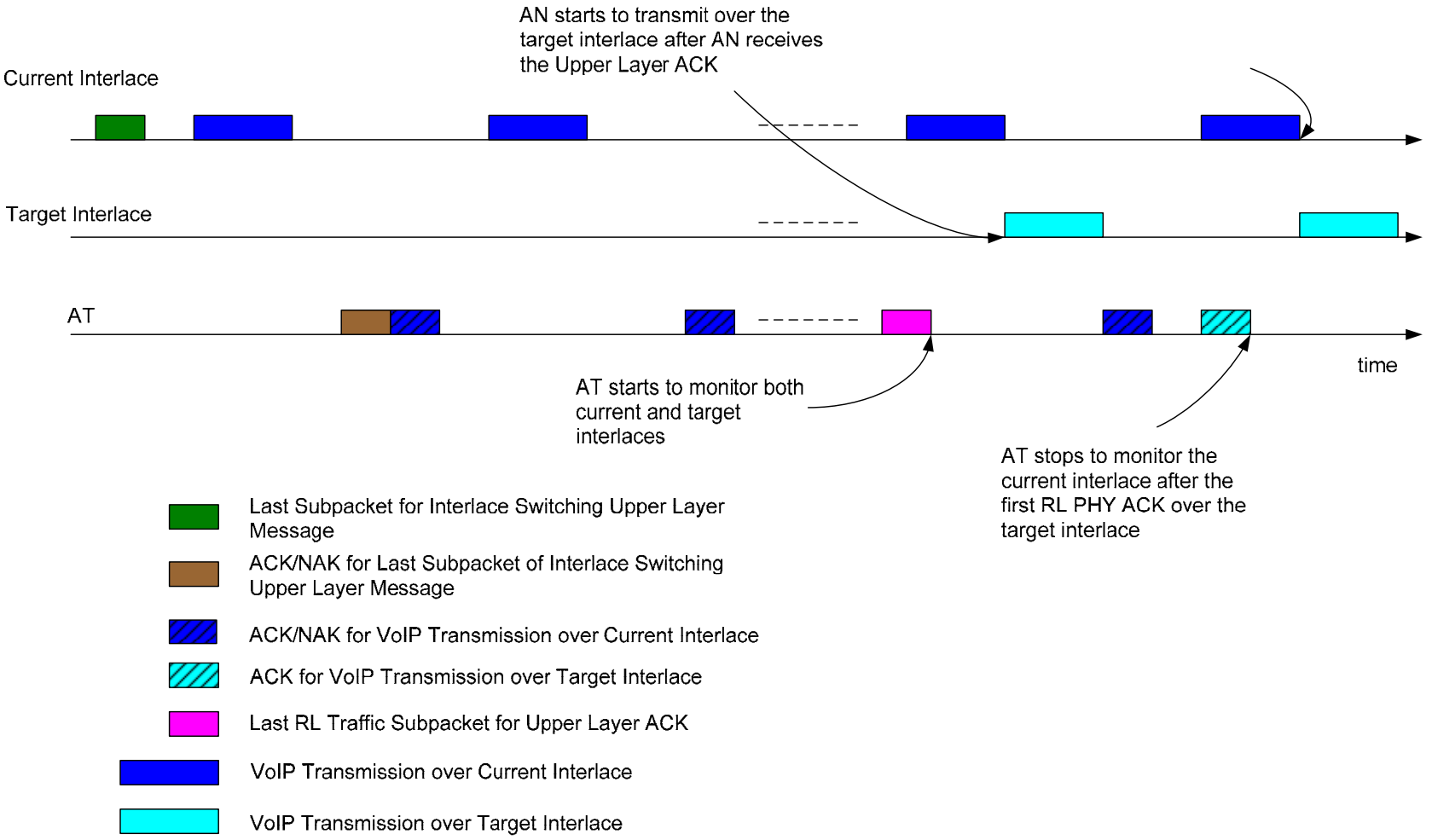


- Timing Illustration of Approach 1

Approach 2 (1/2)

- This approach can be used for interlace and/or interlace offset switching in the same interlace
- Transmission over the current interlace/offset
  - » When the group setup message is transmitted for the purpose of interlace and/or interlace offset switching, the VoIP traffic (subpacket) is transmitted only over the current interlace/interlace offset.
  - » AT sends “ACK” or “NACK” following the normal operation, i.e. over the current interlace/offset.
  - » After upper layer “ACK” is received at AN, the VoIP traffic is transmitted only over the target interlace/offset.
  - » AT monitors both the current and target offsets because the AT doesn’t sure about the transmission time over the target offset.

Approach 2 (2/2)



- Timing Illustration of Approach 2

References

[1] IEEE P802.20 Version D2.1 Draft Standard for Local and Metropolitan Area Networks – Standard Air Interface for Mobile Broadband Wireless Access Systems Supporting Vehicular Mobility – Physical and Media Access Control Layer Specification, May 2006

[2] J. Tomcik, “QFDD Technology Overview Presentation,” C802.20-05-59

Thank you !!!