Project	**IEEE 802.20 Working Group on Mobile Broadband Wireless Access** **<http://grouper.ieee.org/groups/802/20/>**
Title	**Irregular Repeat-Accumulate LDPC Code Proposal – Presentation**
Date Submitted	**2007-03-13 (March 13, 2007)**
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Re:	IEEE 802.20 Call for Proposals
Abstract	This document introduces a new coding scheme based on Irregular Repeat Accumulated (IRA) Codes which is proved to be suitable for small packet lengths produced by VoIP-like applications, and thus proposed to be included into Mobile Broadband Wireless Access Systems as an alternative to Convolutional Codes.
Purpose	For consideration and adoption as a feature for 802.20 standards draft
Notice	
Release	
Patent Policy	

Irregular Repeat Accumulate (IRA) LDPC Code Proposal - for Short Data Block Size

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March 13, 2007

Channel Coding for MBTDD/FDD

- Convolutional coding R-1/3
  - For small data block size, k <128
- Turbo codes, base rate -1/5
  - Parallel Concatenated Convolutional Codes
- Current proposal for consideration:
  - Adopt Irregular Repeat Accumulate Codes in place of the R-1/3 convolutional code

DISTRIBUTION OF PACKET SIZES AS PERCENTAGE OF OVERALL TRAFFIC[1]

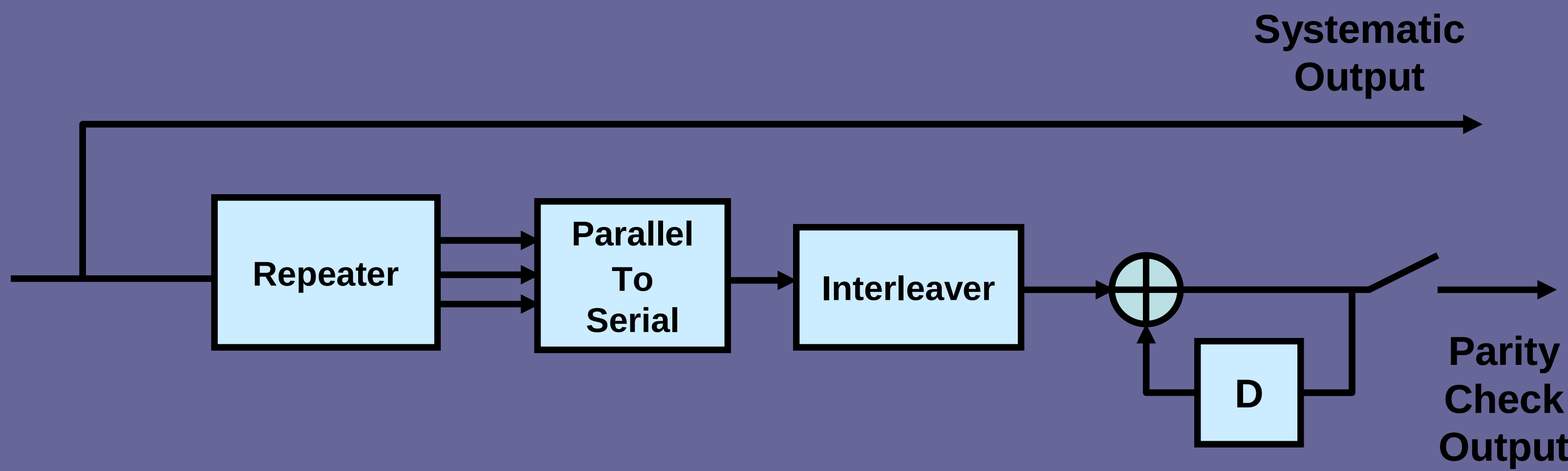
	40 byte	576 byte	1500 byte	Other sizes
HTTP	46.77 %	27.96 %	8,10%	17.17 %
Napster	34.98 %	45.54 %	4.18 %	15.30 %
EMAIL	38.25 %	25.98 %	9.51 %	26.26 %
FTP	40.43 %	18,08%	9.33 %	32.16 %

Source: [1] A. Klemm, C. Lindemann, M. Lohmann, "Traffic Modeling and Characterization for UMTS Networks", Internet Performance Symposium 2001, San Antonio, TX, USA, November, 2001.

Channel Coding of Small Packets

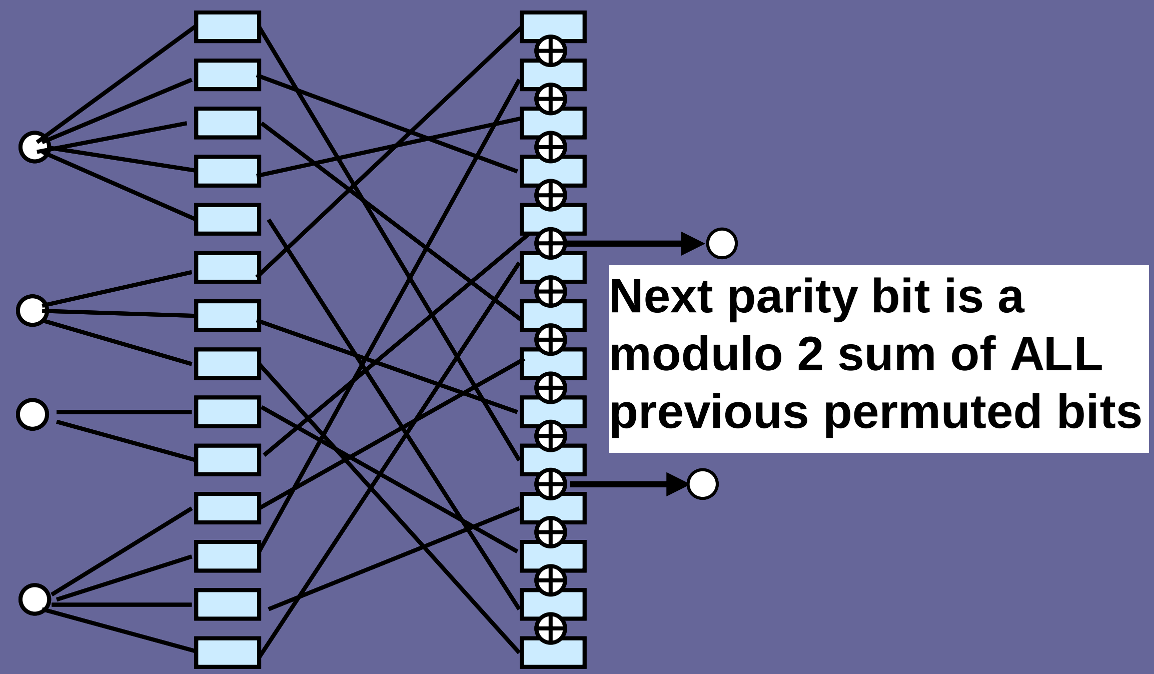
- Irregular Repeat Accumulate Code (IRA)
  - For small packet size, e.g., from 2-40 bytes
  - Example applications:
    - Voice
    - Text messaging
    - Gaming
    - Web browsing
    - ACK
- **Gain of 0.5 dB – 1.0 dB observed from simulation results**

Basic Repeat-Accumulate Encoder Structure



- Serial concatenation of Reptition Encoder and Accumulator, separated by an interleaver
- Accumulator:
  - Rate-1 Convolutional Encoder with polynomial = $\frac{1}{1 + D}$

Tanner Graph of RA Codes



- **Subset of LDPC codes**
- **Variable nodes connecting to Parity nodes via the Edges according to the permutation**
- **Decode through Message-Passing algorithms (Belief propagation)**
- **Efficient implementation using parallel architecture**
- **LDPC codes were discussed in a 2003 Contribution: C802.20-03-02R1 [2]**

S-Random Interleaver - Algorithm A

- Degree distribution at the variable node can be defined as:

$$\sigma(y) = \sum_i \sigma_i \cdot y^{i-1}$$

  - where σ_i is the fraction of variable nodes with degree i

- Define:

$$S_i = f(i)$$

- S-Random Algorithm with “S” adapted to the degree of each variable node, i.e., the repetition factor
- For any two nodes m, n belong to fraction σ_i, condition for permutations P(m), P(n):

$$|m-n| < S_i \Rightarrow |\Pi(m)-\Pi(n) \geq S_i|$$

- Requires memory for storage, cannot be computed on the fly

Algebraic Interleaver - Algorithm B

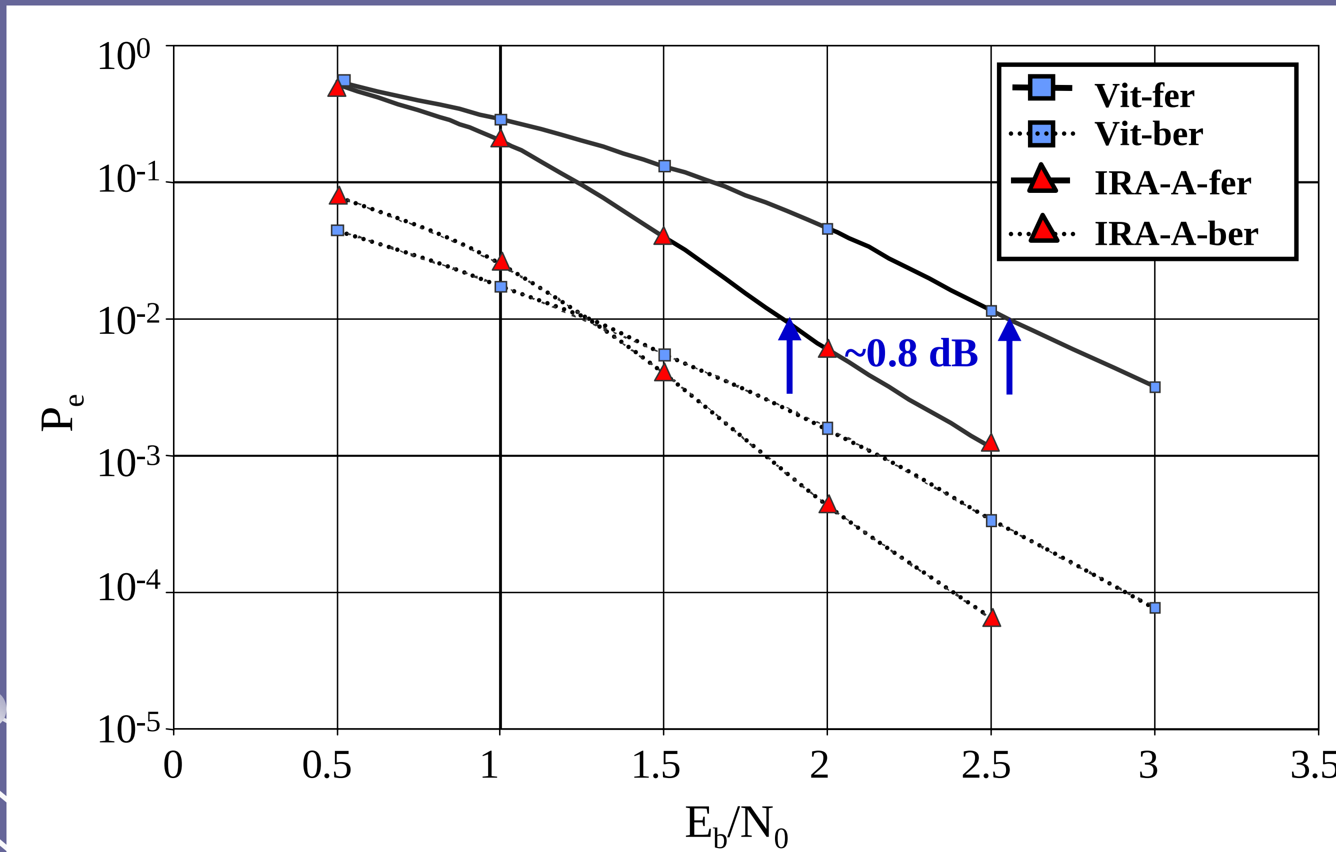
- Circular shifting interleaving
- Advantage: Can be computed on the fly
- Procedure:
  - Randomly drop 24 first numbers (0-23) into rectangular pattern such that only one number shall be placed in each column.
  - Place another number into the column such that the next number in the column is obtained by the following formula,

$$x^{j}_{(i+1)\bmod 4} = (x^{j}_{i} + 72) \bmod 96$$

  - Read the numbers in row-wise order.
  - Check the resulting interleaver with the proposed criteria and define the final group of the interleavers.

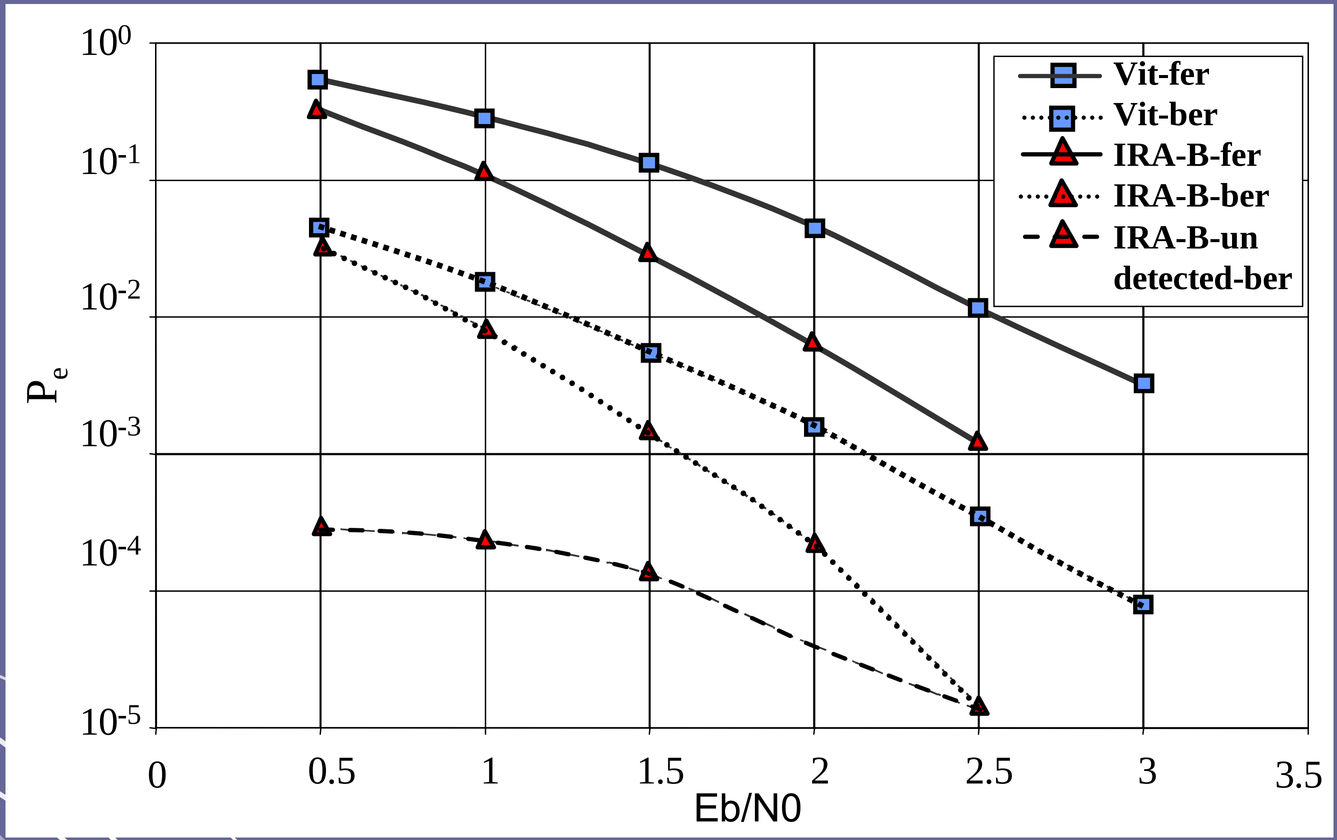
42	89	1	9	40	76	61	19	14	79	45	22	6	50	27	58	48	32	84	63	35	53	71	92
18	65	73	81	16	52	37	91	86	55	21	94	78	26	3	34	24	8	60	39	11	29	47	68
90	41	49	57	88	28	13	67	62	31	93	70	54	2	75	10	0	80	36	15	83	5	23	44
66	17	25	33	64	4	85	43	38	7	69	46	30	74	51	82	72	56	12	87	59	77	95	20

Simulation Results – Algorithm A



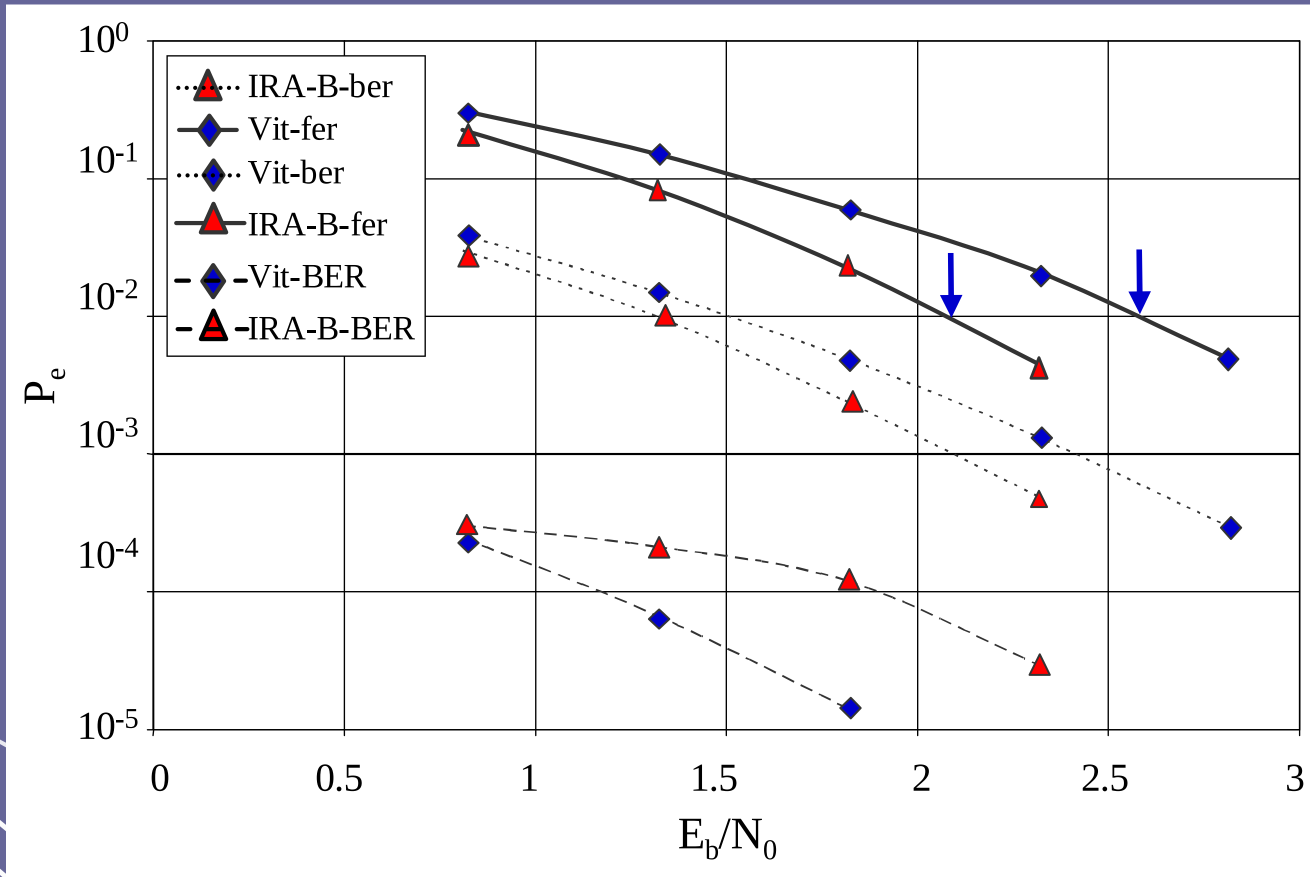
- Full-rate EVRC, 172 bits
- IRA outperforms CC with a gain of 0.8 dB at 10^{-2} frame error rate

Simulation Results – Algorithm B



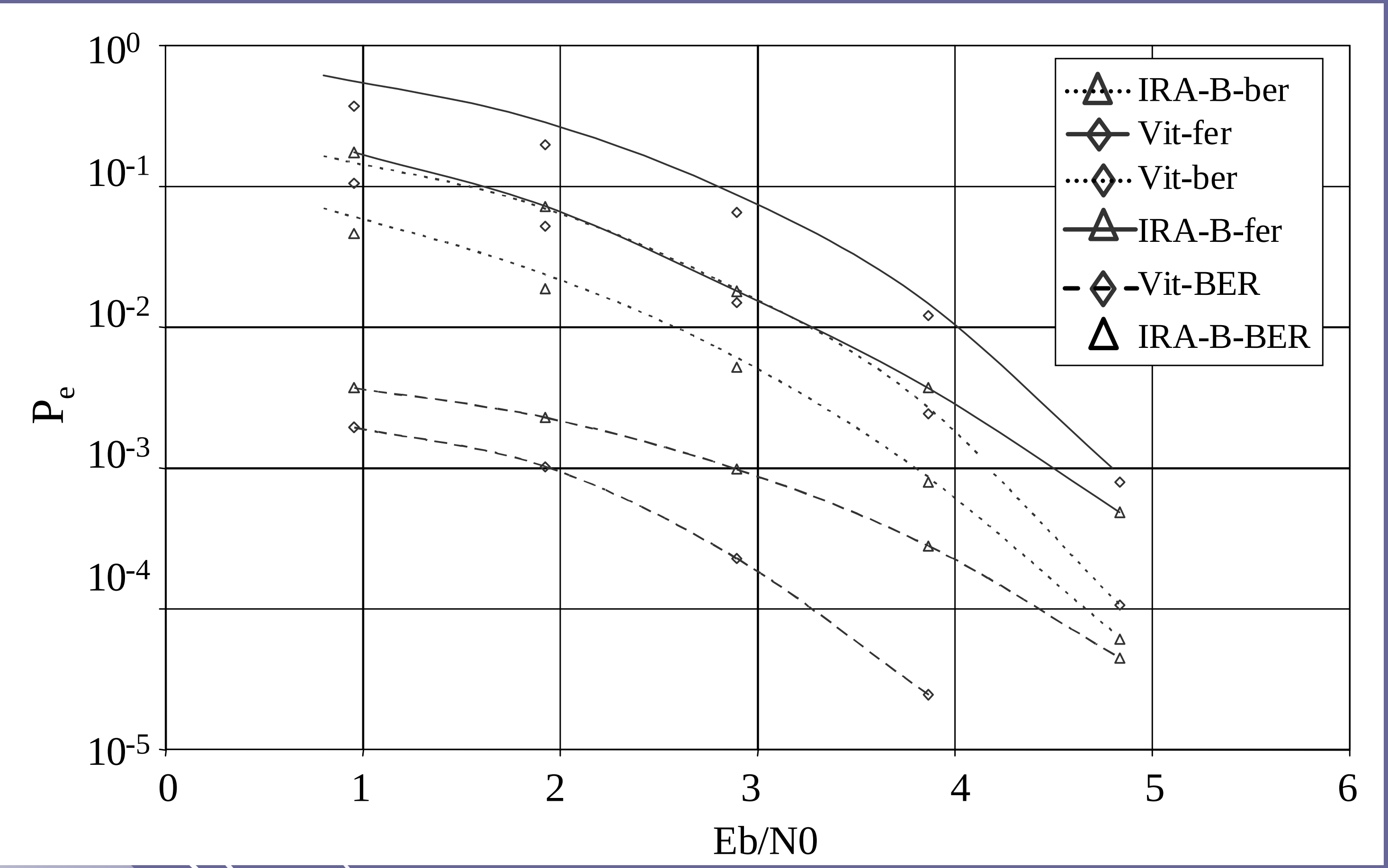
- Full-rate EVRC, 172 bits
- IRA outperforms CC with a gain of 0.8 dB at 10^{-2} frame error rate

Simulation Results – Algorithm B



- Half-rate EVRC, 80 bits
- IRA outperforms CC with a gain of 0.5 dB at 10^{-2} frame error rate

Simulation Results – Algorithm B



- Half-rate EVRC, 80 bits
- IRA outperforms CC with a gain of 0.7 dB at 10^{-2} frame error rate

Conclusion

- IRA LDPC codes for short packet size outperforms convolutional codes by 0.5 – 1 dB
- Consider IRA LDPC codes for adoption as channel encoding scheme in place of the R-1/3 convolutional encoder in the MBTDD/MBFDD proposal

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