

Remaining gaps for EEE in 40/100G

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IEEE P802.3bj
November, 2012

With thanks...

With thanks to –

all those who participated in conference call reviews

Agenda

- ▶ Clause 74 FEC compatibility (still)
- ▶ Timing TBDs
- ▶ LLDP support
- ▶ Questions...

D-1.1 – Comment #68, 69

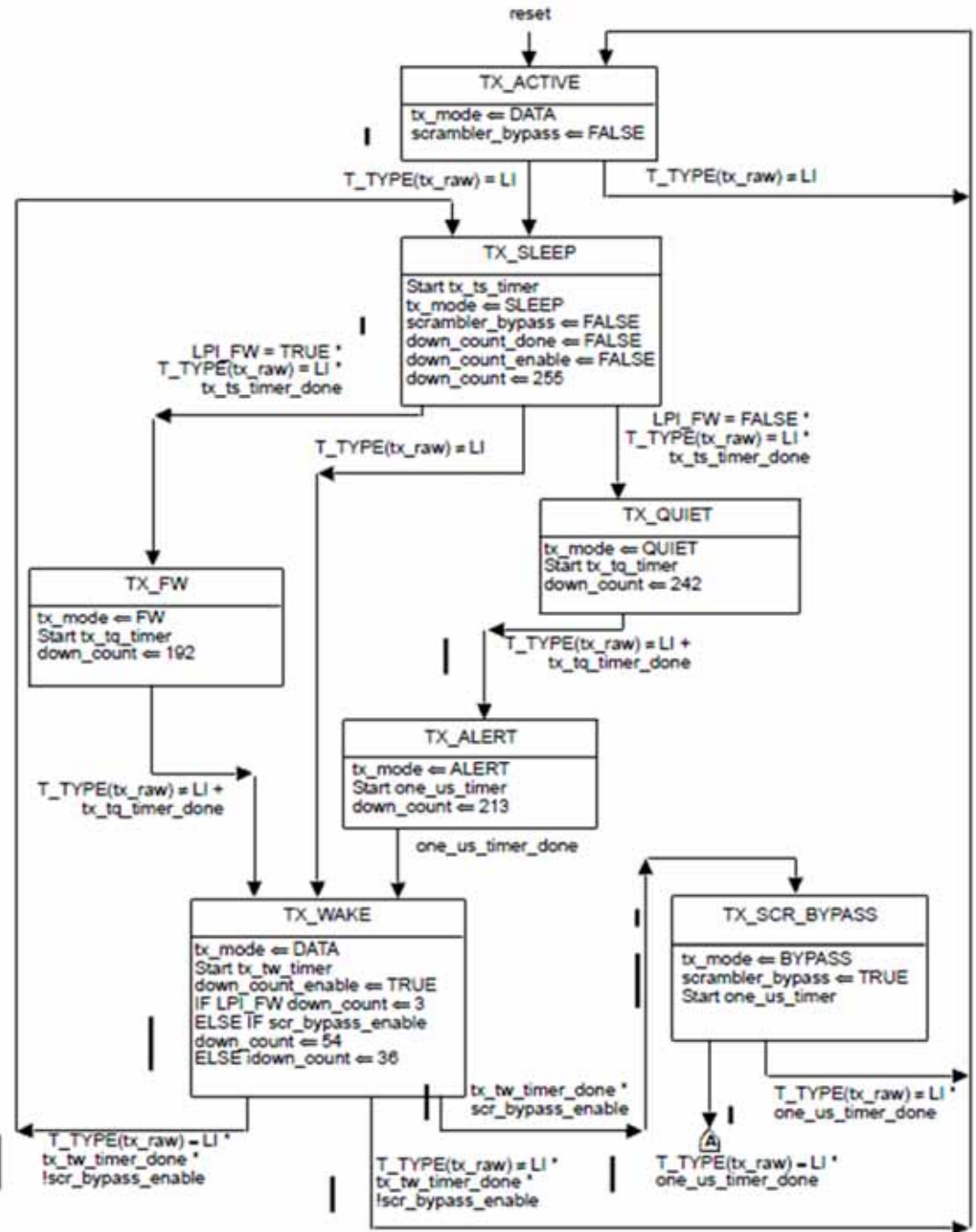
- ▶ A proposal that Clause 74 should be changed to require FEC to resynchronize based on RAMs was rejected...
 - It was preferred to keep existing FEC implementations unchanged
- ▶ Therefore scrambler bypass must be used as defined in Clause 49.
- ▶ This will add 2uS to normal wake with FEC.
 - This is acceptable because FEC latency is slow anyway; Fast Wake is available; & such implementations are rare anyway

Clause 74 FEC with 10GBASE-KR

- ▶ FEC relies on scrambler_bypass for rapid lock
 - Pre-determined data contents for 1uS during wake
 - 74.7.4.8 FEC rapid block synchronization for EEE (optional)
- ▶ Extra state for scrambler bypass in Tx LPI s/m
 - No change for Rx state machine (just longer wake time)
- ▶ Also combine with suggested change to eliminate separate states for refresh wake (makes s/m simpler)

Tx LPI state diagram

Delete states for refresh a
Add new state for scramb



Scrambler bypass changes

- ▶ Variable definitions for `scrambler_bypass` and `scr_bypass_enable` in 82.2.18.2.2 (EEE only)
 - Only required with CI 74 FEC
- ▶ Scrambler subclause does not need to change...
 - "The scrambler is identical to the scrambler used in Clause 49"
- ▶ Tx timing unchanged, Rx wake time increases:
 - Table 82-5b, add row with 6.5uS for scrambler bypass
 - Similarly for Table 78-4

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Table 78-2 – Key EEE parameters

- ▶ T_s, T_q, T_r – all TBDs
 - Sleep time, quiet time, refresh width
- ▶ $T_s = 0.9/1.1$ μS (from Table 82-5a)
- ▶ $T_q = 1700/1800$ μS (from Table 82-5a)
- ▶ $T_s = 5.9/6.5$ μS
 - Sum of T_{SL}, T_{WL}, T_{1U} – (all from Table 82-5a)
- ▶ Should not be controversial!

Table 78-4 – LPI timing parameters

- ▶ $T_{w_sys_tx}$, T_{w_phy} , $T_{phy_shrink_tx}$, $T_{phy_shrink_rx}$,
 $T_{w_sys_rx}$
 - All TBDs
 - Figure 78-4 explains parameter relationships
- ▶ $T_{w_sys_tx}$ Time transmitter must hold back data
- ▶ T_{w_phy} Wake time for transmitter (PHY)
- ▶ $T_{phy_shrink_..}$ Difference (wake time – data delay)
- ▶ $T_{w_sys_rx}$ Remaining wake time for Rx @ MAC
- ▶ Require some assumptions...

$T_{w_sys_rx}$ key parameter for system

- ▶ Determines warning MAC components get
 - 2.88uS for 10Gbps PHYs; 1.76uS for 1Gbps PHYs
 - Needs similar figure for 40G & 100G
 - May be smaller for Fast Wake
- ▶ Suggest: 1.2uS for 40G, 1.0uS for 100G
 - Slightly faster because of newer Si capabilities
- ▶ Suggest: 0.25uS for Fast Wake (40G & 100G)
 - Effectively driven by delays through PHY
- ▶ NB – discussion needed for these

T_{w_phy} , $T_{phy_shrink_tx}$, $T_{phy_shrink_rx}$

- ▶ T_{w_phy} Related to PHY wake time
 - Suggest: 5.5uS; 0.30uS Fast Wake
- ▶ $T_{phy_shrink_tx}$ 2uS – allow for ALERT + other delays
- ▶ $T_{phy_shrink_rx}$ 3uS – extra for wake recognition
- ▶ $T_{phy_shrink_..}$ Fast Wake – no shrink for Tx/Rx
- ▶ Also needs discussion...

$T_{w_sys_tx}$ critical derived parameter

- ▶ $T_{w_sys_tx}$ - based on PHY wake + Tx shrink
 - Suggest 5.5uS for 40/100G; 7.5uS with scr_bypass
- ▶ Fast Wake = 0.34uS
 - Driven by Tx state requirements
- ▶ This value drives effective Rx wake requirements
 - Dependent on Rx architecture
- ▶ Approx 4.5uS for PHY; 1uS for PCS above FEC
- ▶ Also needs discussion...

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LLDP exchange of Fast Wake

- ▶ Add Fast Wake enable to TLV
 - 79.3.5 – Tx & Rx Fast wake enable & echo (all 1 octet)
 - New or extra TLV – decision required
- ▶ New state machines similar to 78-5
 - i.e. changes to Tx_wake or Rx_wake trigger action
 - → similar trigger for local or remote Fast Wake
- ▶ Define variables:
 - LocTxSystemFW; LocTxSystemFWEcho
 - LocRxSystemFW; LocRxSystemFWEcho
 - Definitions self-explanatory

LLDP FW Rx/Tx state machines

- ▶ Watch this space for new FW state machines...

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Questions...

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CISCO