Feasibility Study for:

IEEE 802.3 100GbE Electrical Backplane / Copper Cabling Study Group

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Purpose

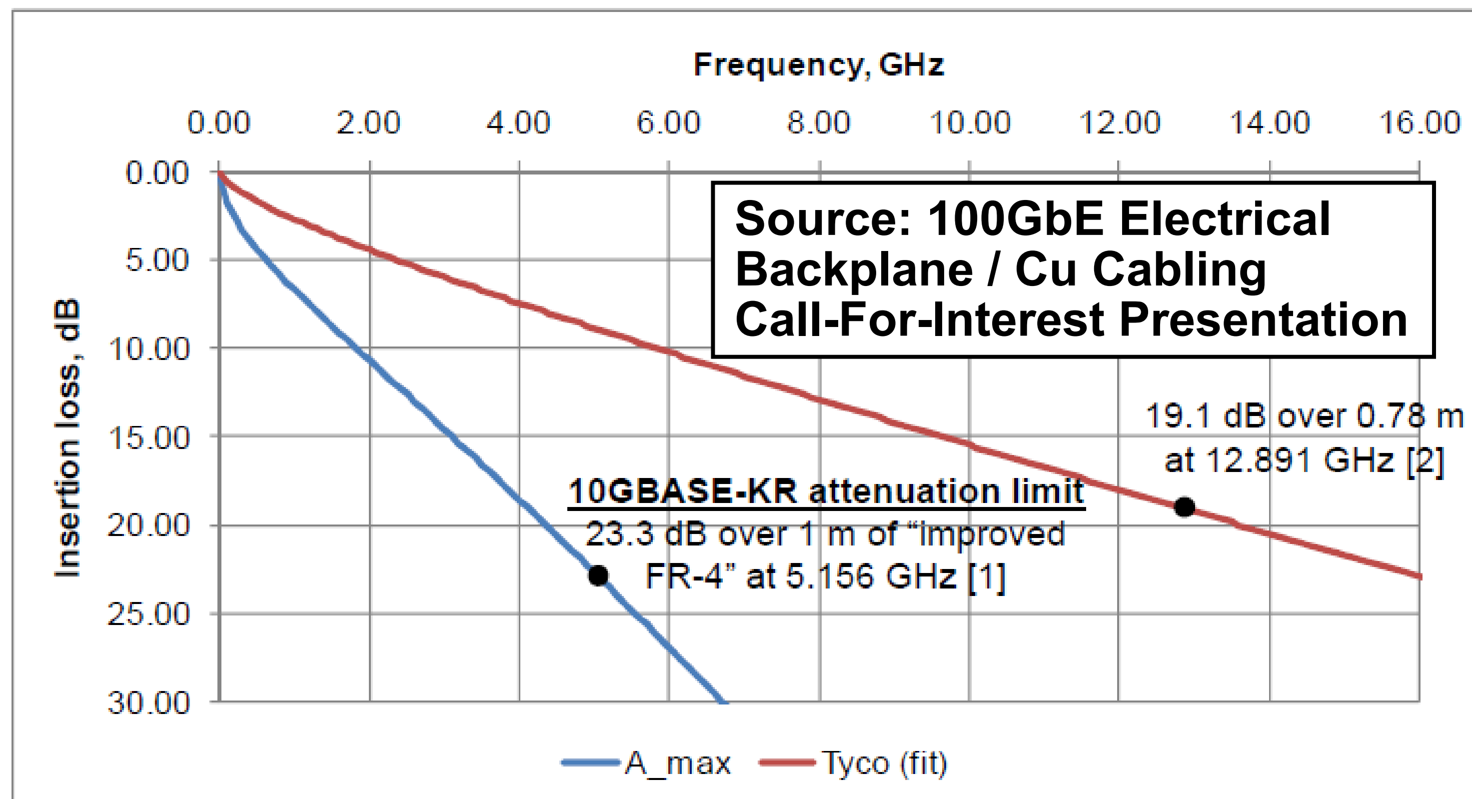
FCI

- To show the possible reach that can be obtained at 25Gbps with low loss boards and a new FCI Connector Concept (CC)
- To show the performance of a short link (15 cm) and a long link (70 cm) consisting of a line card, a switch card, a backplane and two connectors compared to an IEEE 802.3ap spec extrapolated to 25Gbps
- ICN requirements shown here are commensurate with the OIF CEI-25G-LR spec (Nov 16, 2010 revision of OIF2008.161.10)

Typical Backplane Channel Loss

FCI

Backplane channel loss



[1] IEEE Std 802.3TM-2008, 69B.4.2
[2] Source: Tyco Electronics, 0.51 m backplane, two 0.10 m line cards, two 0.035 m ideal connectors, 6-8-6 mil differential stripline, Nelco 4000-13SI dielectric, 1 oz copper

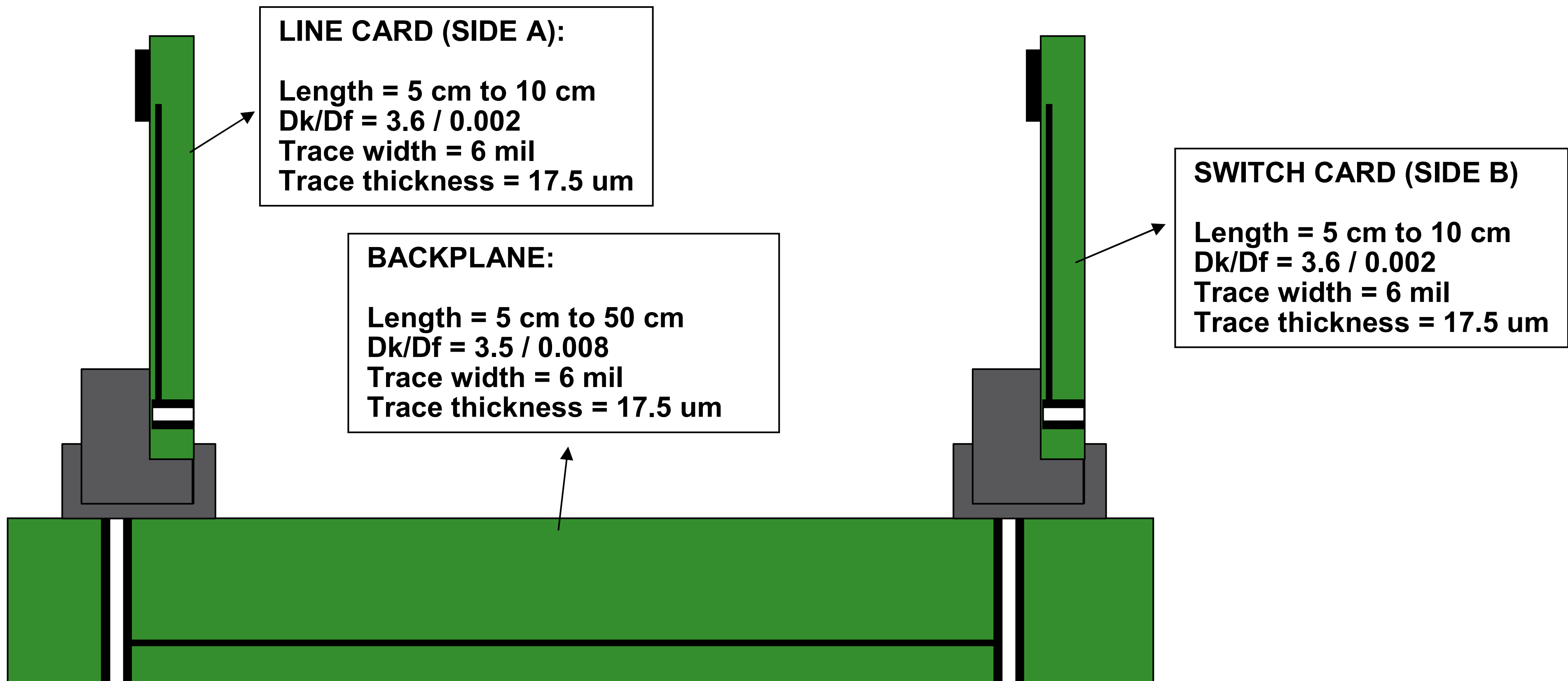
0.7 m of traces on Backplane and two line cards (excluding connector length)

Simulation Settings

FCI

- The FCI Connector Concept (CC) 3D geometry was solved using CST® MWS 2009.7
- Two link cases simulated
  - Short Link: 0.15 m
  - Long Link: 0.70 m
- 8 pairs simulated (4 Tx and 4 Rx)
- Frequency range: 0 to 30 GHz

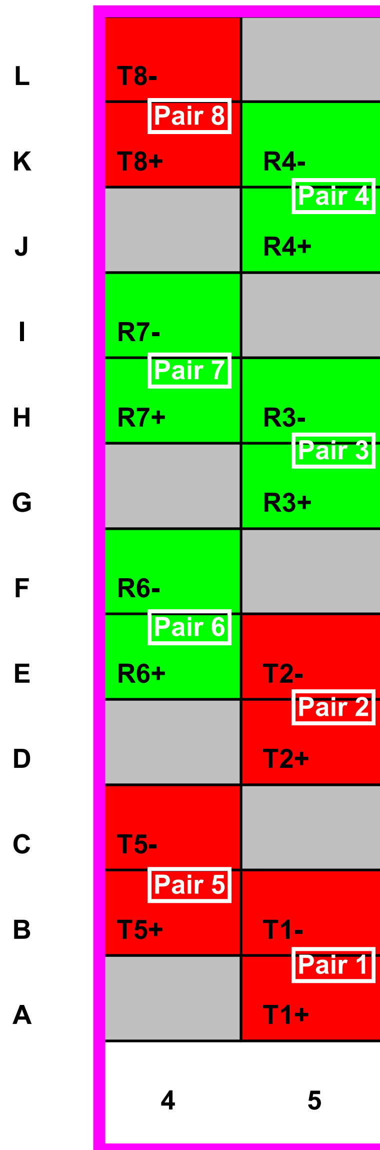
Link Description



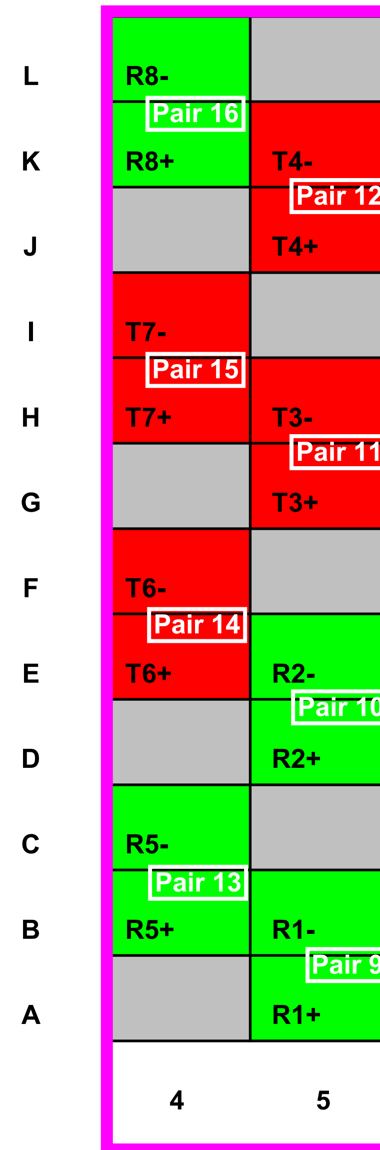
LINK	Length on line card	Length on backplane	Length on switch card	Total trace length
Short Link	5 cm	5 cm	5 cm	15 cm
Long Link	10 cm	50 cm	10 cm	70 cm

TX/RX Configuration

SIDE A LINE CARD



SIDE B SWITCH CARD

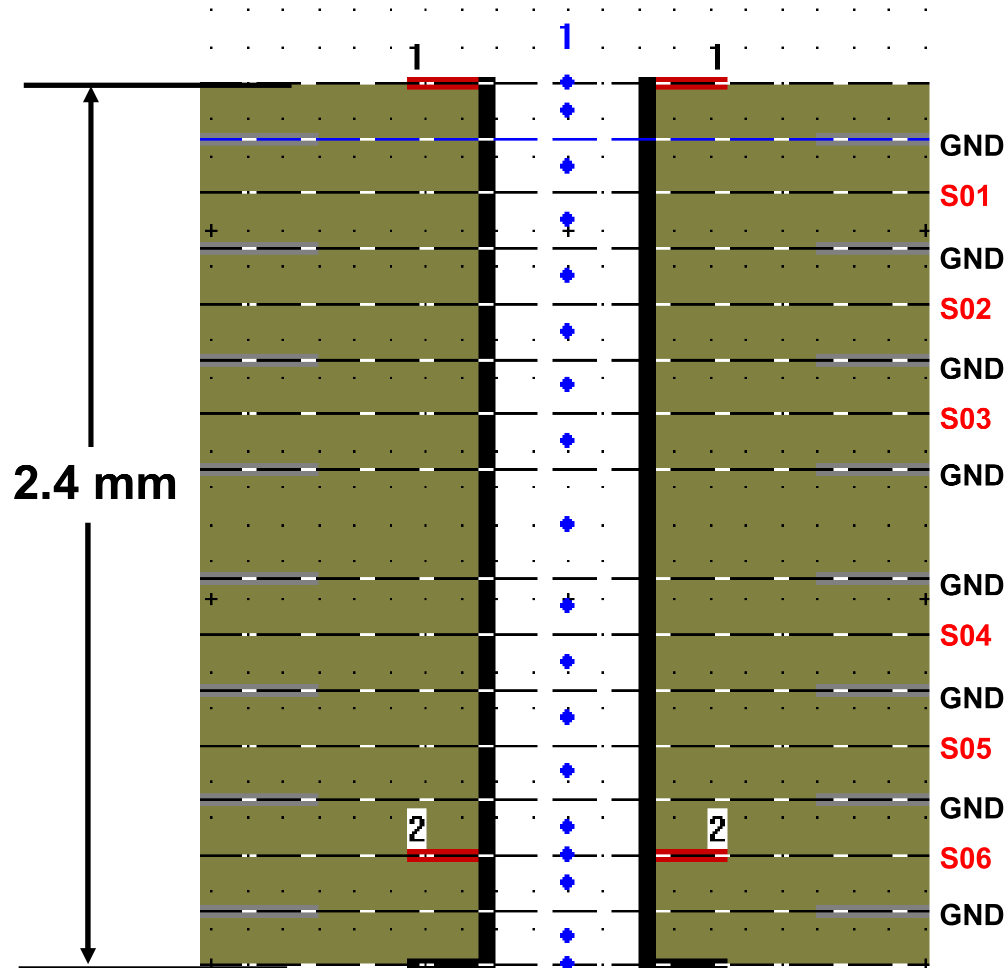


Simulated for columns 4 & 5

Note: Wiring pattern chosen based on optimization for lowest ICN at 10 Gbps

Link Description: Daughter Cards

Board thickness = 2.4 mm
16 layers



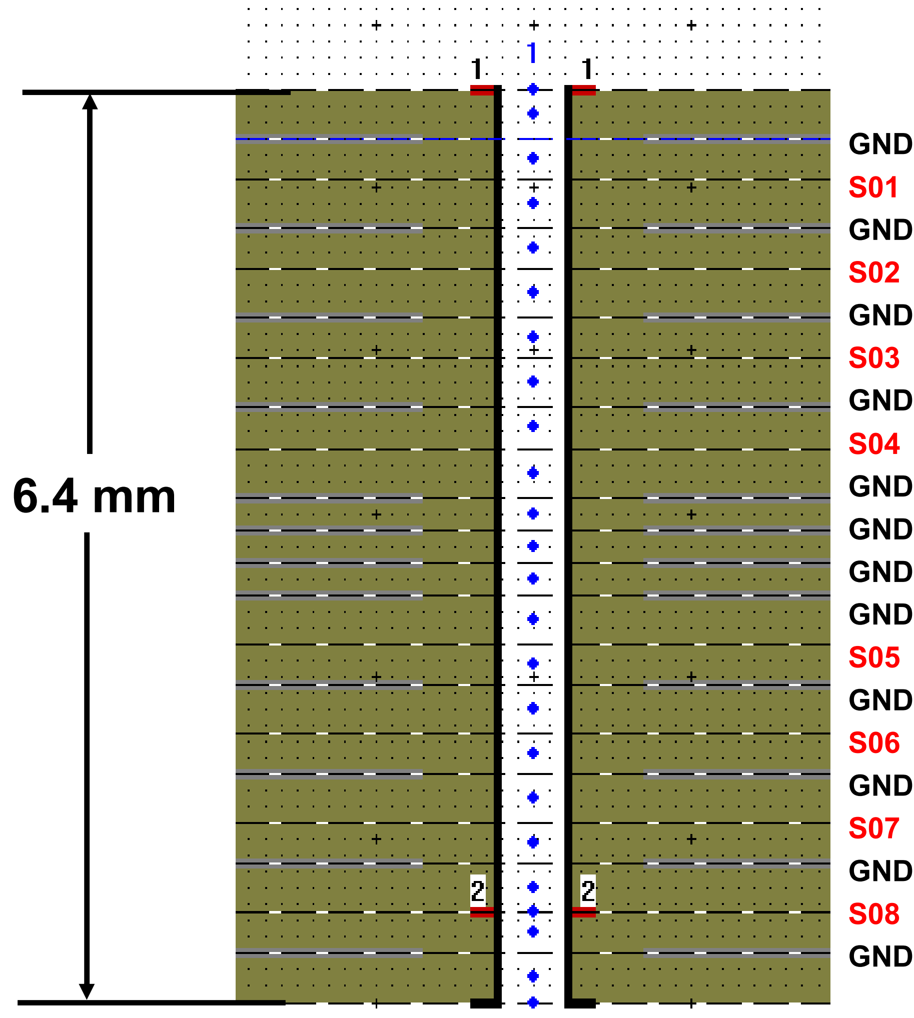
ROUTING

AB: Layer S05
DE: Layer S02
GH: Layer S04
JK: Layer S03
BC: Layer S03
EF: Layer S04
HI: Layer S02
KL: Layer S05

With back-drilling

Link Description: Backplane

Board thickness = 6.4 mm
22 layers



ROUTING

AB: Layer S05
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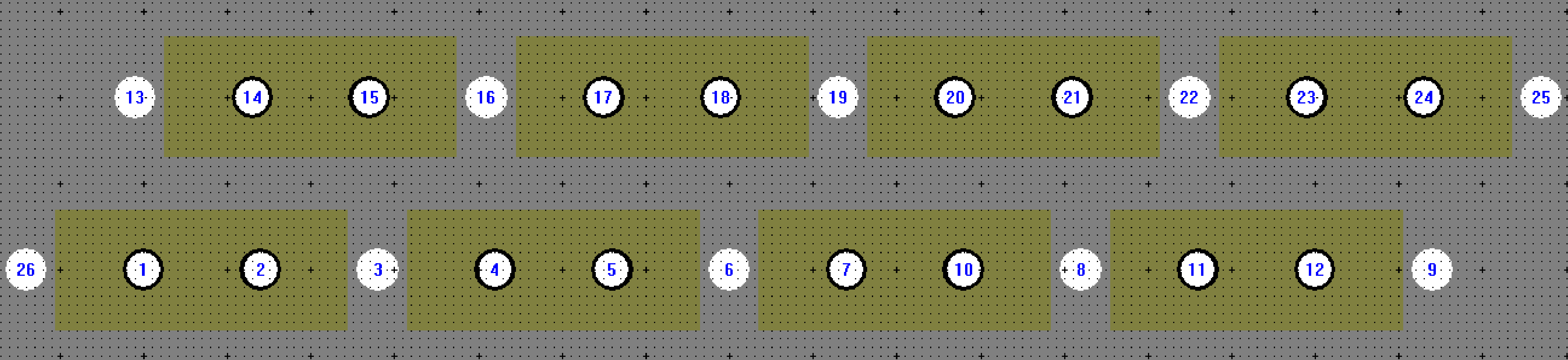
EF: Layer S04
HI: Layer S02
KL: Layer S05

With back-drilling

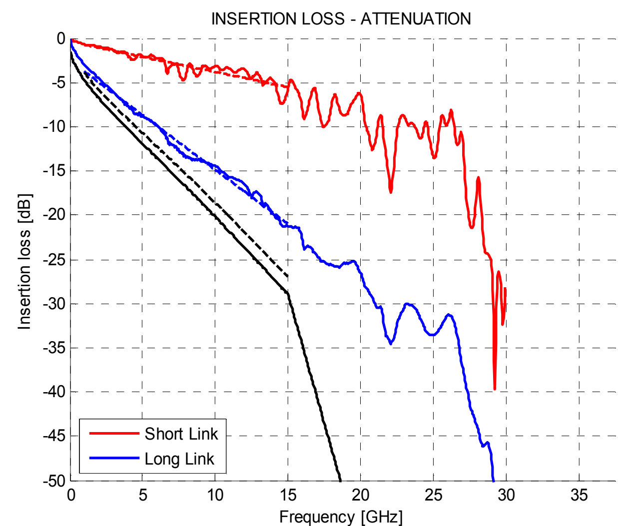
CC Footprint DC & BP

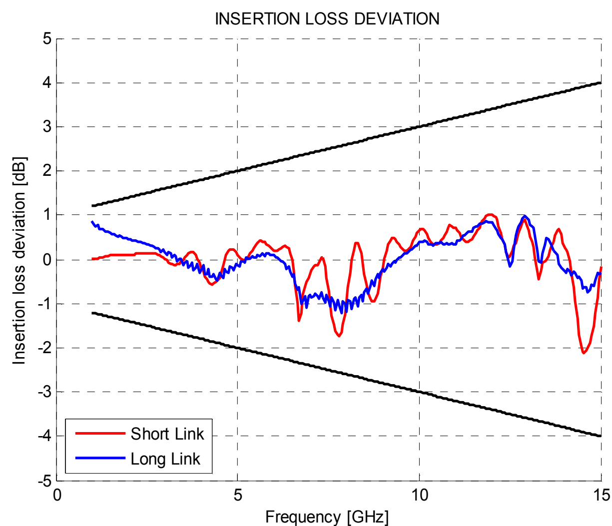


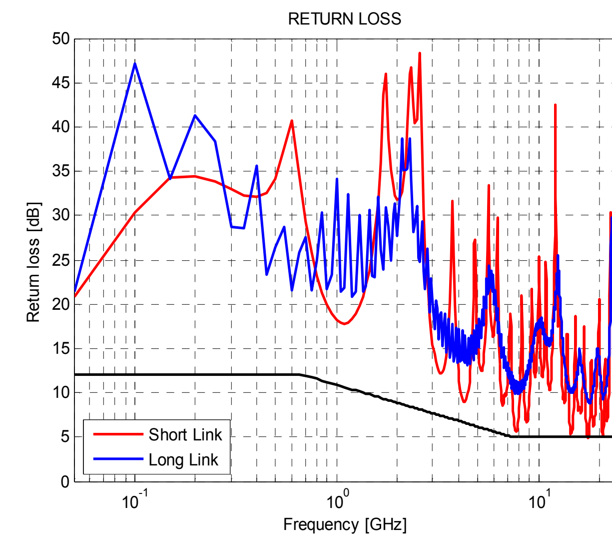
- **Signal vias:**
  - Drilled hole = 0.5 mm
  - Finished hole = 0.4 mm
  - Pad size = 0.7 mm
- **Ground vias:**
  - Drilled hole = 0.6 mm
  - Finished hole = 0.5 mm
  - Pad size = 0.8 mm
- **Antipad:**
  - 3.5 x 1.4 mm

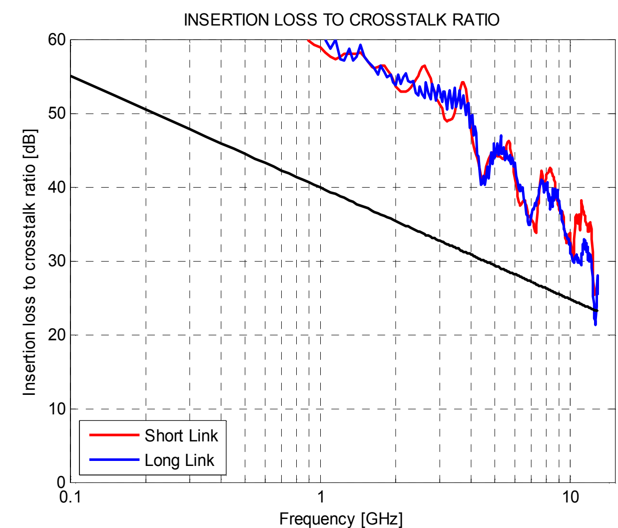
Via models solved with VisualViaCad (FCI proprietary Quasi-Static solver)

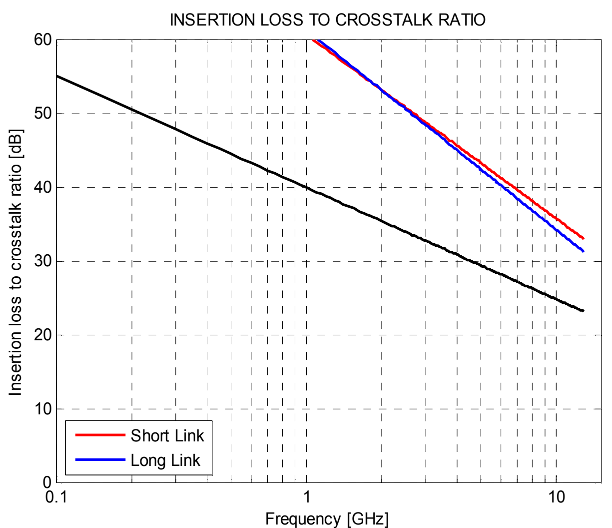
25 Gb/s - CC - AB5(A) TO AB5(B)

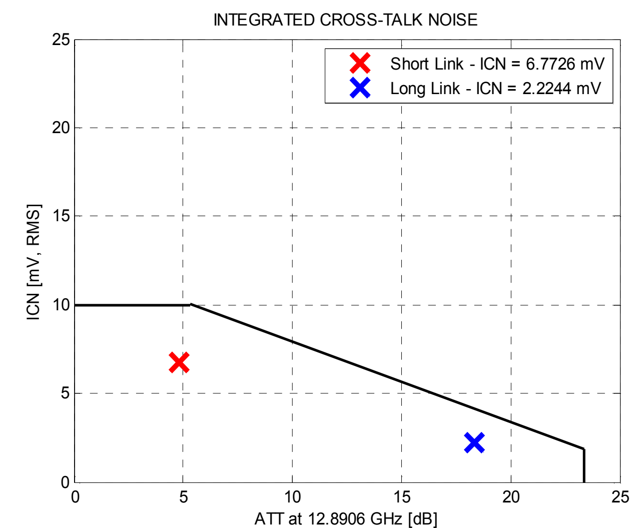




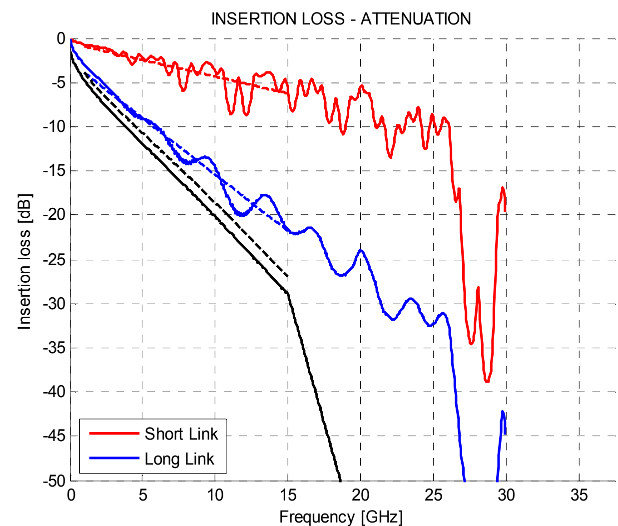


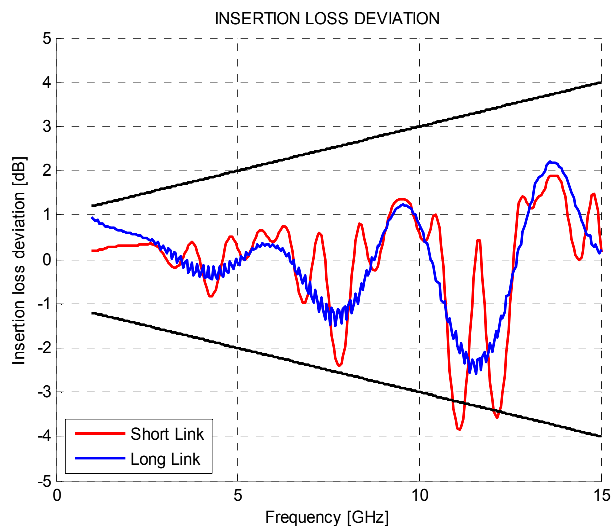


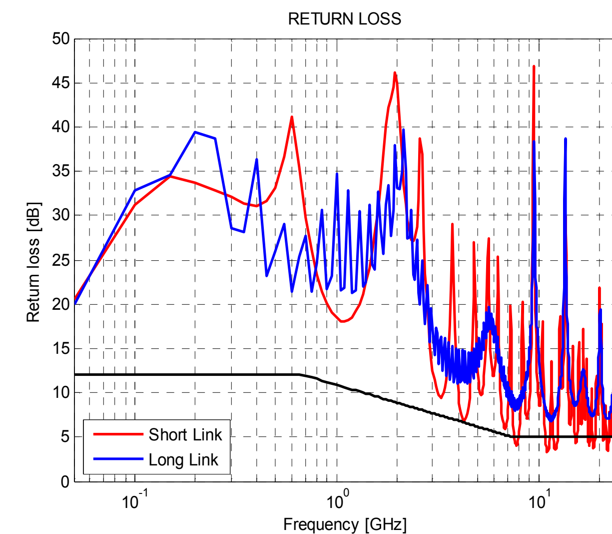


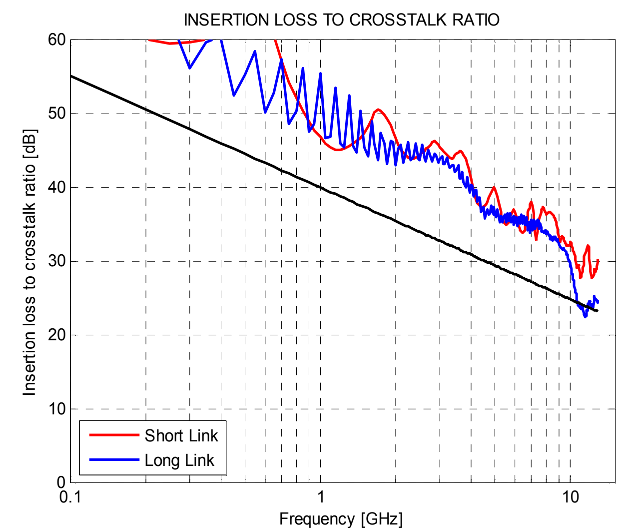


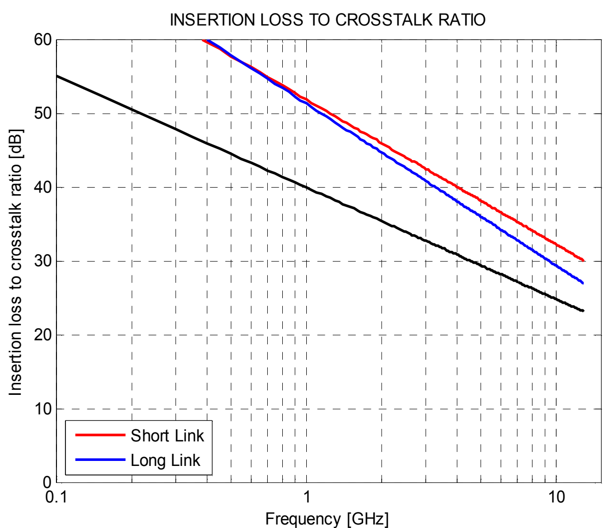
25 Gb/s - CC - DE5(A) TO DE5(B)

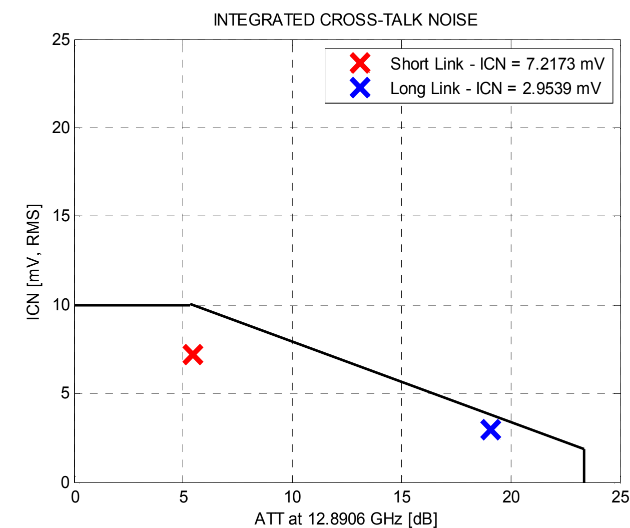






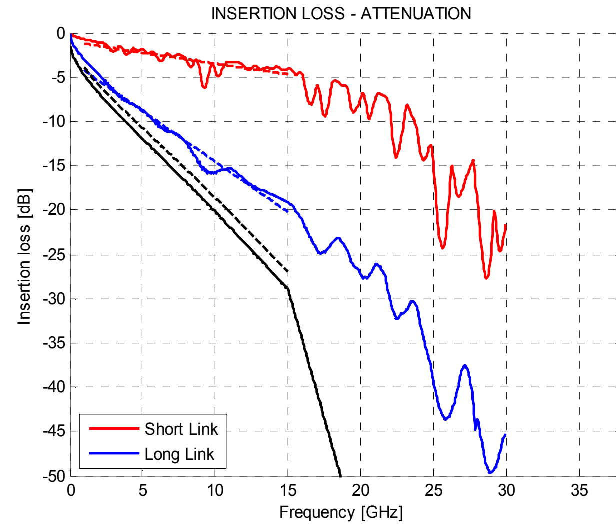


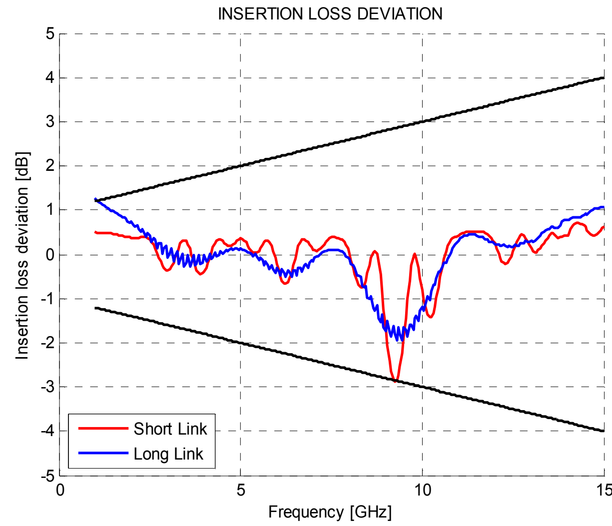


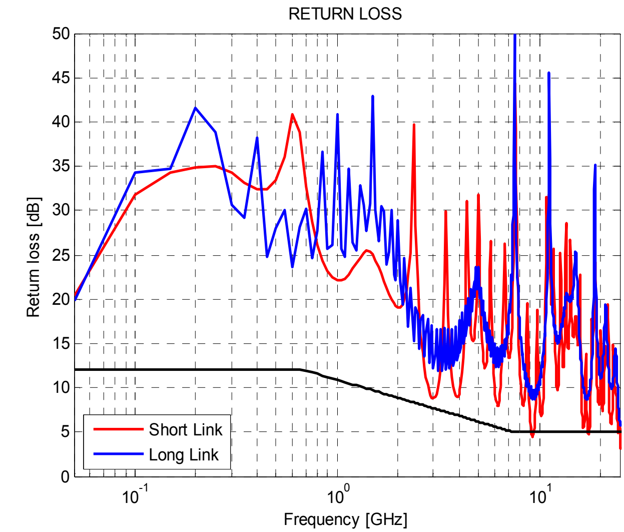


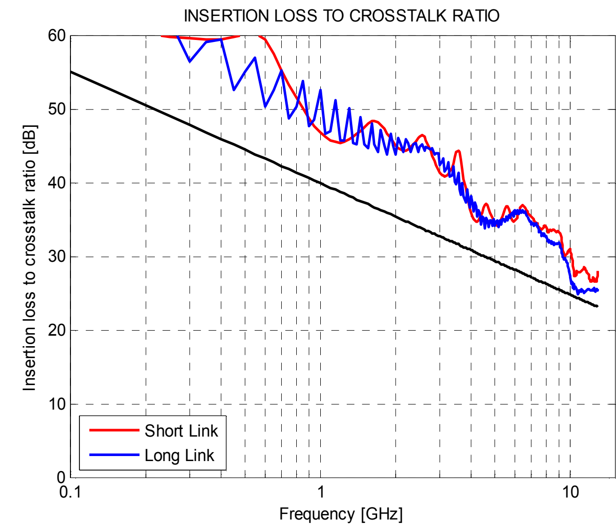
ILD excursions on the short link are due to impedance mismatches in the connector footprint and could be addressed in many ways. One of them being reducing the diameter and/or length of the press-fit pin

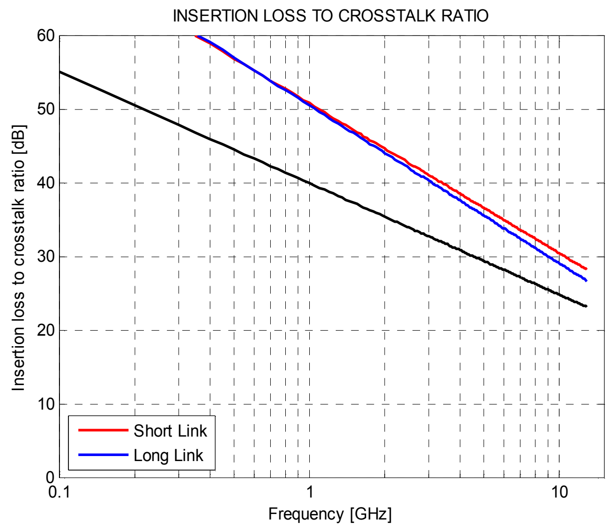
25 Gb/s - CC - GH5(B) TO GH5(A)

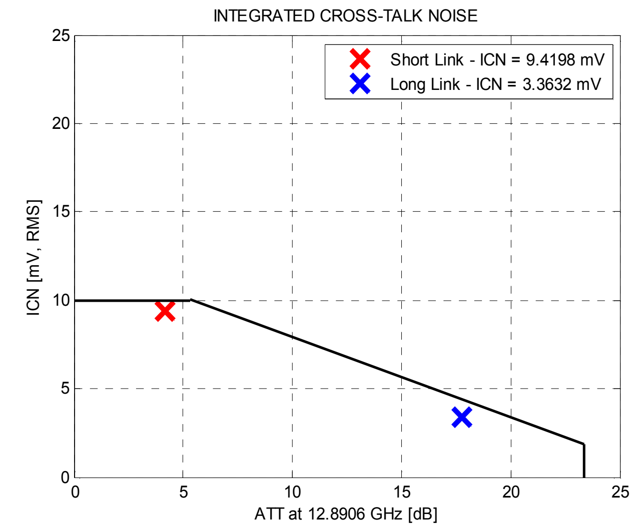




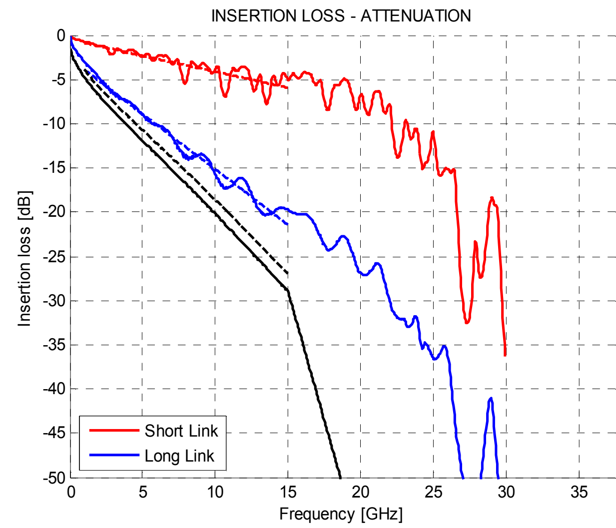


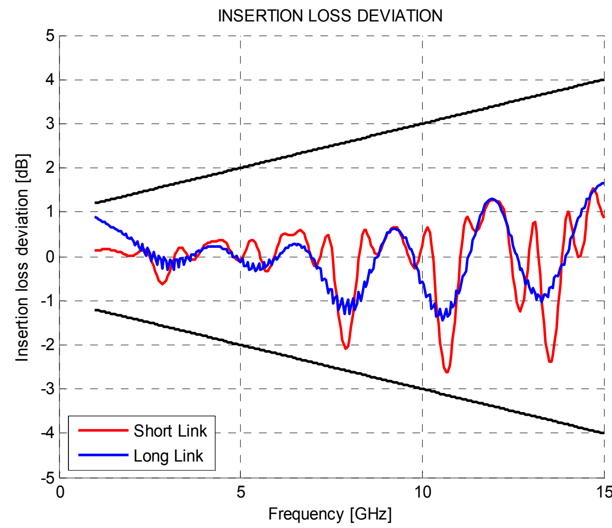


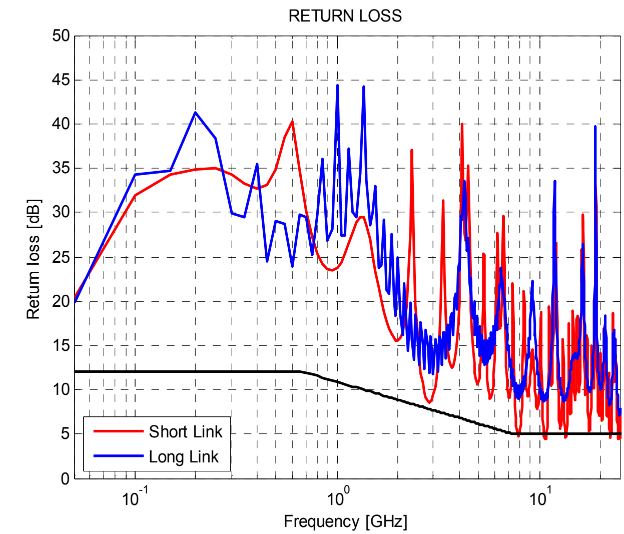


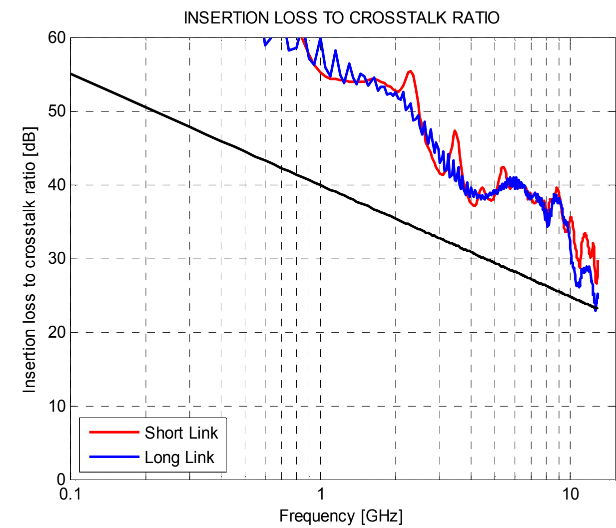


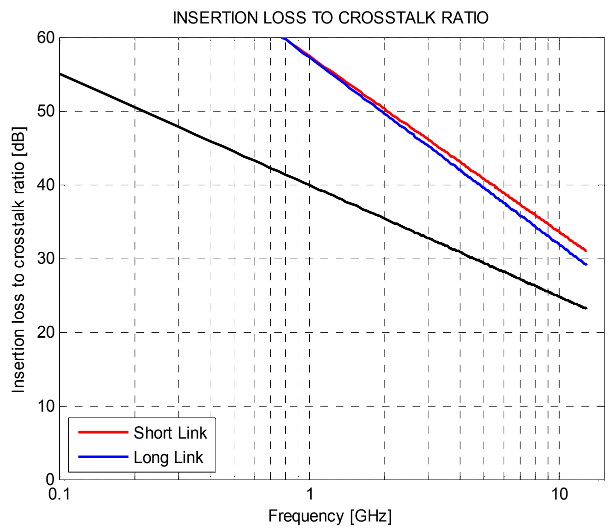
25 Gb/s - CC - JK5(B) TO JK5(A)

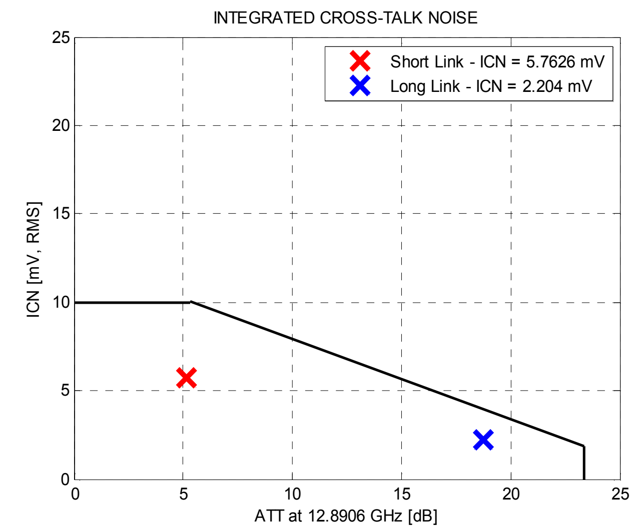




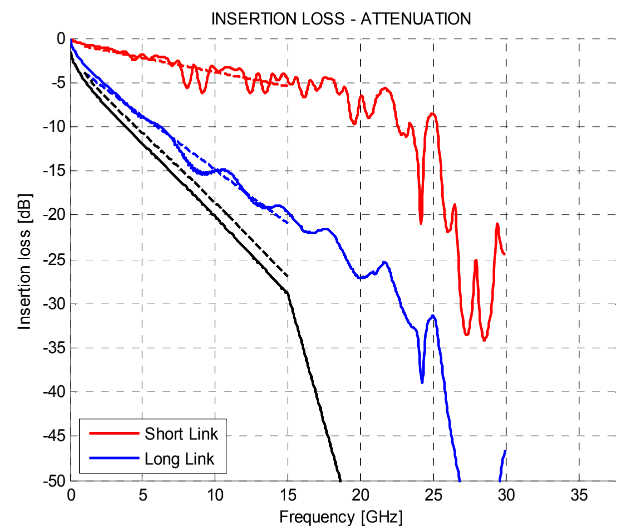


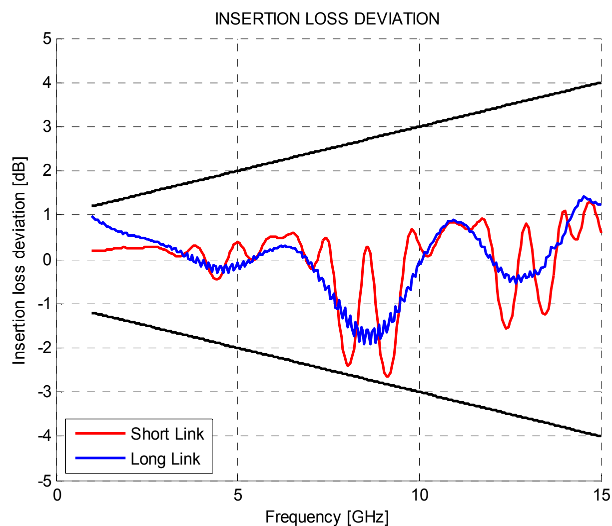


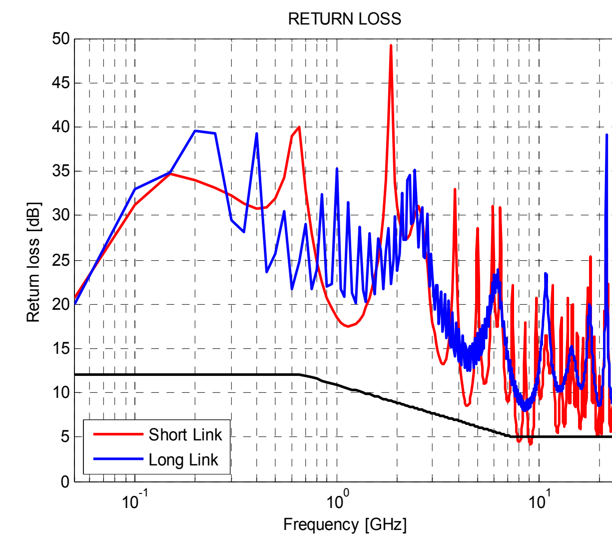


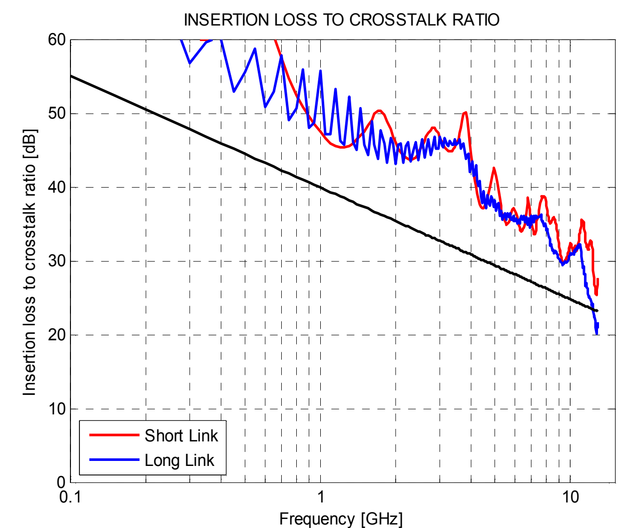


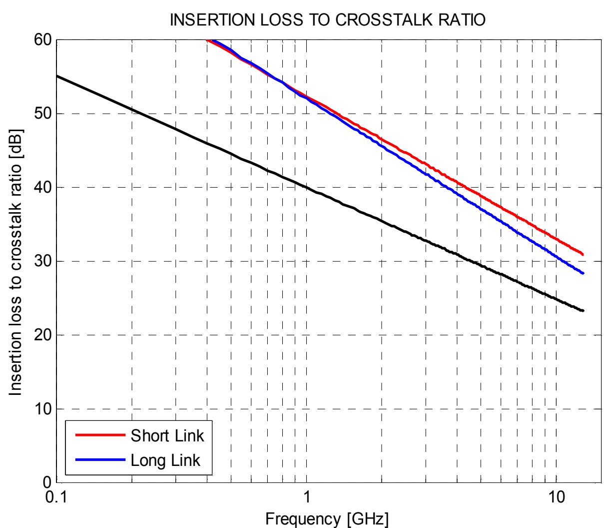
25 Gb/s - CC - BC6(A) TO BC6(B)

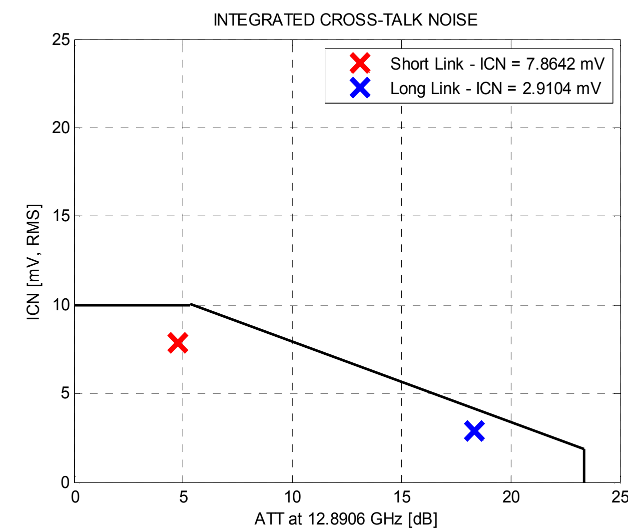




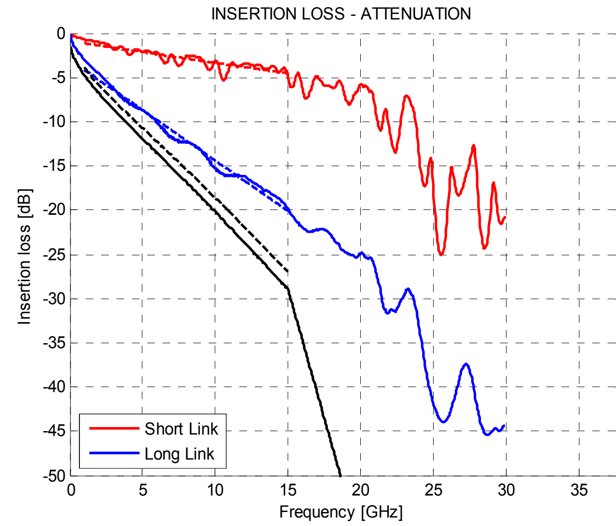


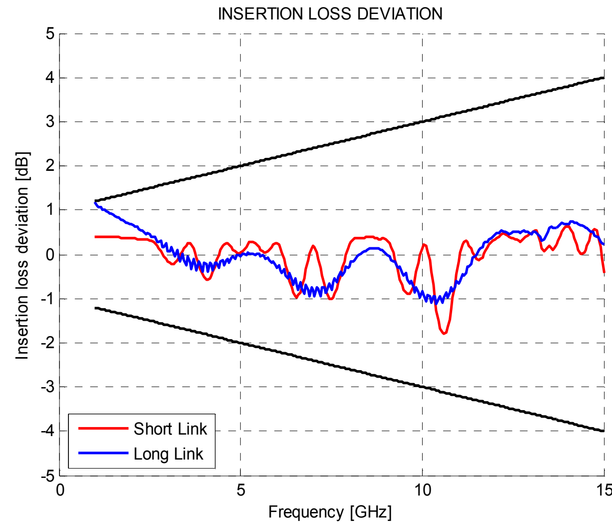


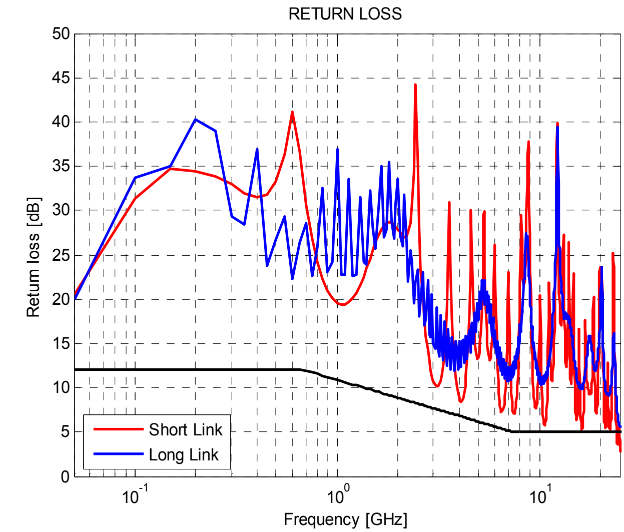


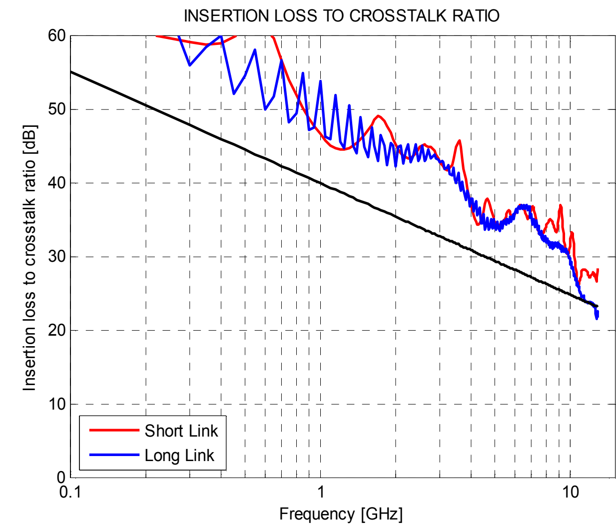


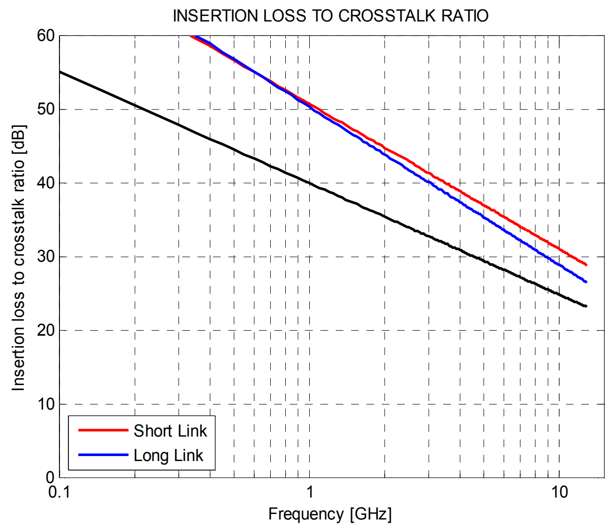
25 Gb/s - CC - EF6(B) TO EF6(A)

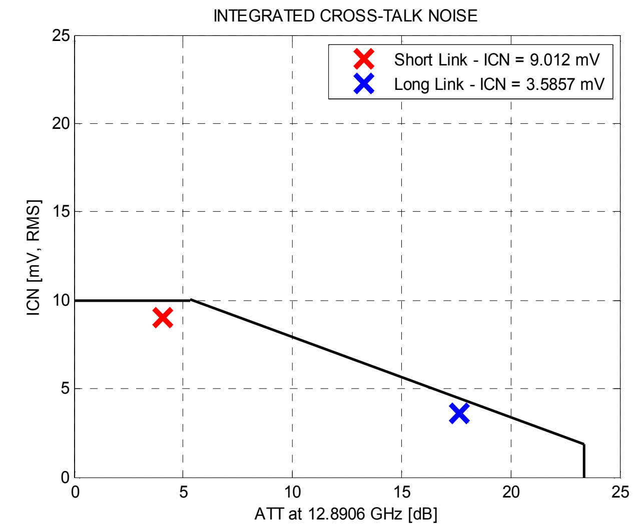




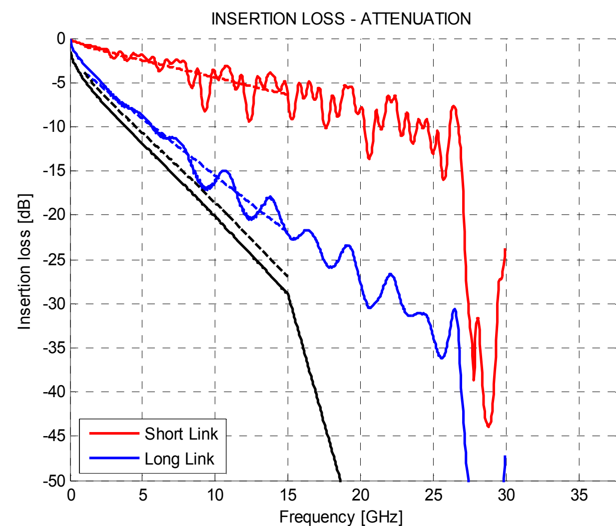


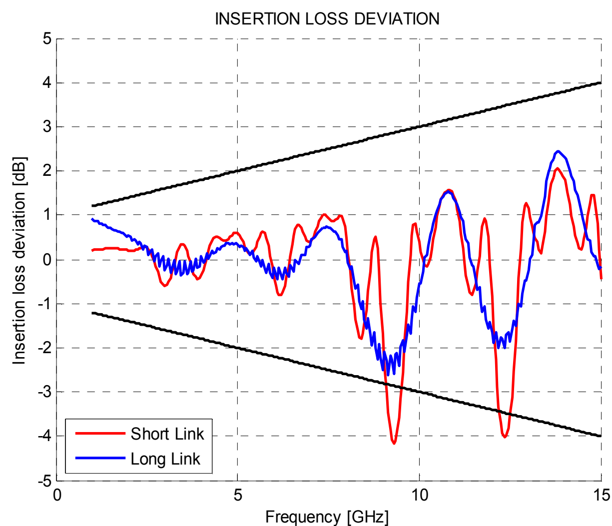


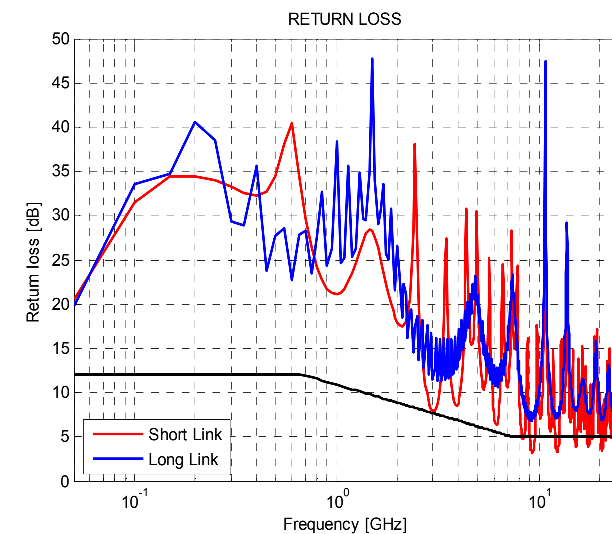


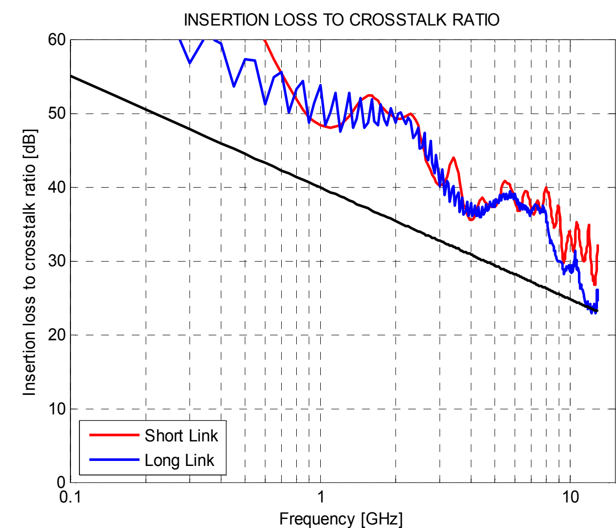


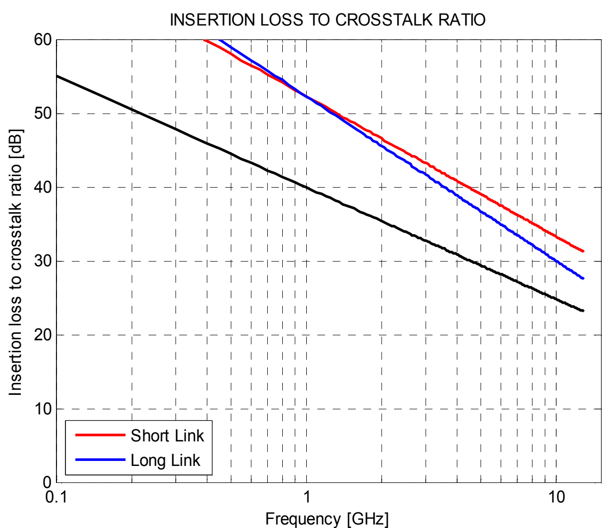
25 Gb/s - CC - HI6(B) TO HI6(A)

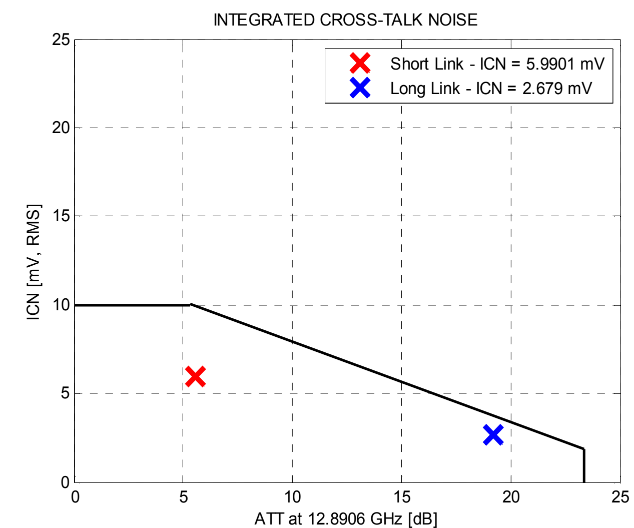












ILD excursions on the short link are due to impedance mismatches in the connector footprint and could be addressed in many ways. One of them being reducing the diameter and/or length of the press-fit pin

25 Gb/s - CC - KL6(A) TO KL6(B)