

The logo for VITESSE, featuring the word in a bold, italicized, white sans-serif font with a registered trademark symbol. The background is dark blue with white circuit-like lines and nodes.

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Making Next-Generation Networks a Reality.

***Technical Feasibility of Serial
25 Gb/s Signaling over
Backplanes: Channel and
System Analysis***

***IEEE 802.3 100GCU Study Group
Interim Meeting, Fort Lauderdale, FL.***

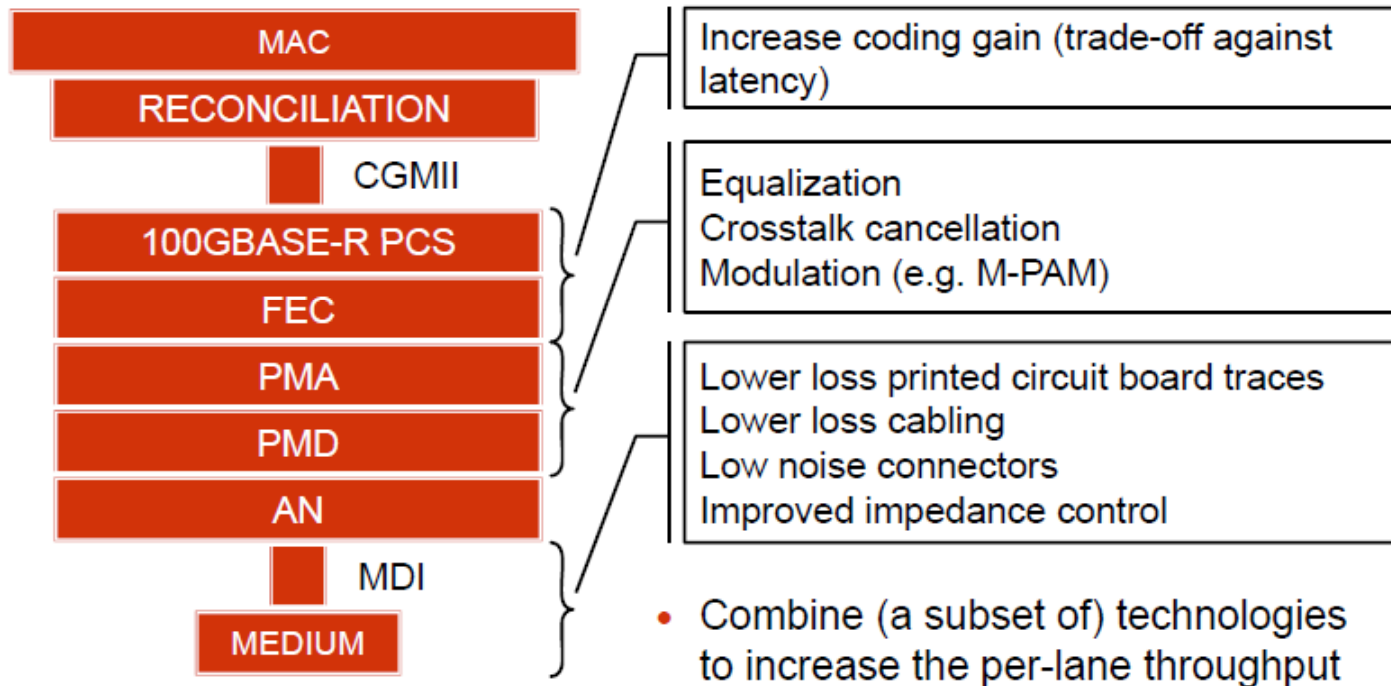
Ziad Hatab and Frank Chang
January 12-13, 2011

Introduction

- ▶ There is a clear demand to develop 25 Gb/s serial over backplane solutions towards higher throughput per lane:
 - ▶ Higher port density in servers and data centers.
 - ▶ Current trends for chip-chip backplane speeds vary from 19.9 to 25.8 Gb/s/lane.
- ▶ Technical & economical feasibility are among major concerns for end users:
 - ▶ Signal integrity through 25 Gb/s backplane is hard to achieve with higher insertion losses, distortions, and impairments.
 - ▶ Various well-understood technologies such as equalization, multi-level coding schemes, and FEC can be combined to achieve 25 Gb/s.
 - ▶ New and higher-cost channel materials and connectors with improved signal integrity are in development by industry.
 - ▶ Technical solutions, while feasible, should make economic sense (power/complexity/cost/latency).

Considering Technology Enablers

Potential enablers for more Gb/s/lane



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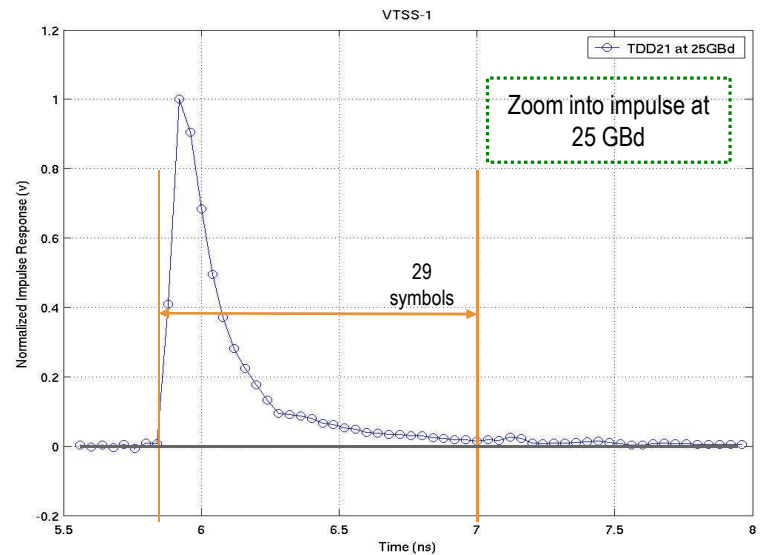
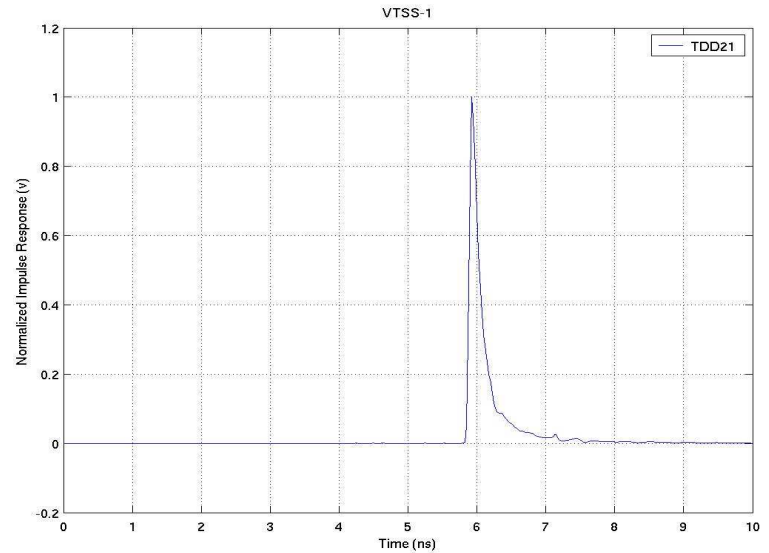
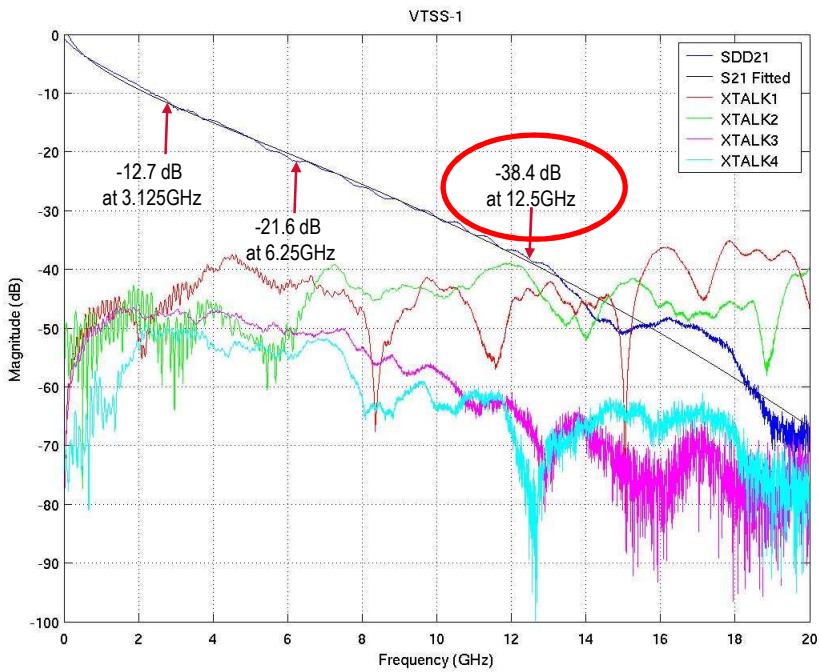
100GbE Backplane/Cu Cable CFI
IEEE 802 Plenary, Dallas, TX, Nov 2010

November 9, 2010

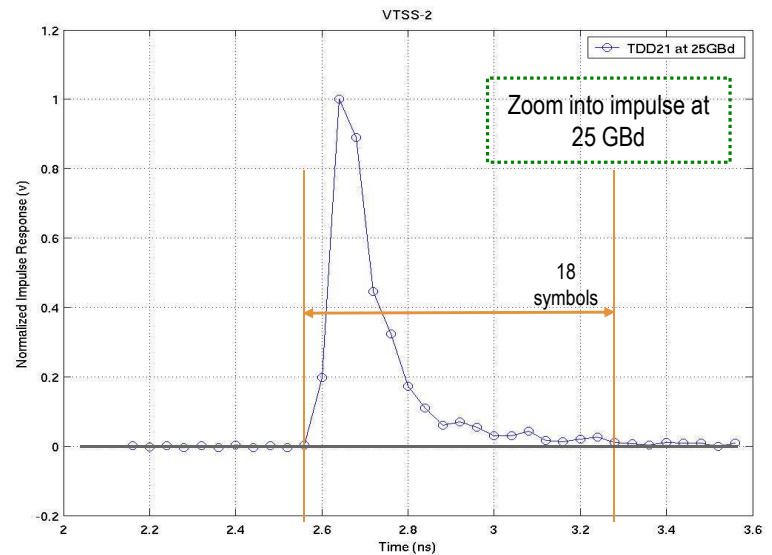
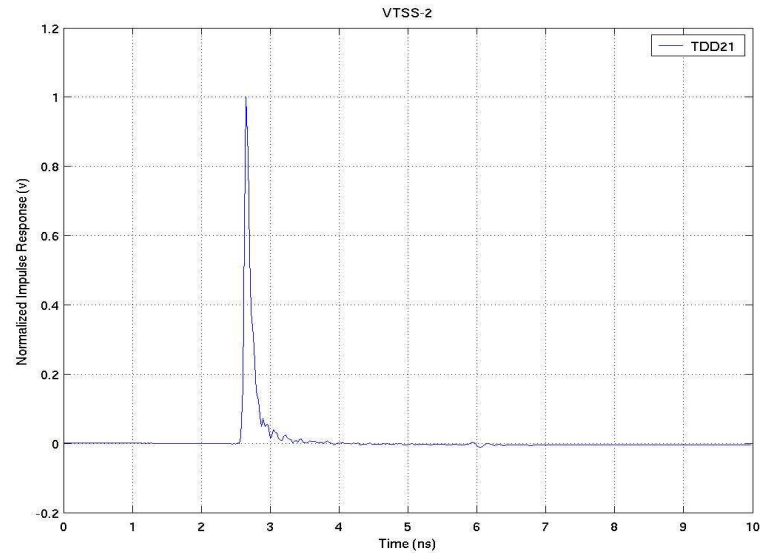
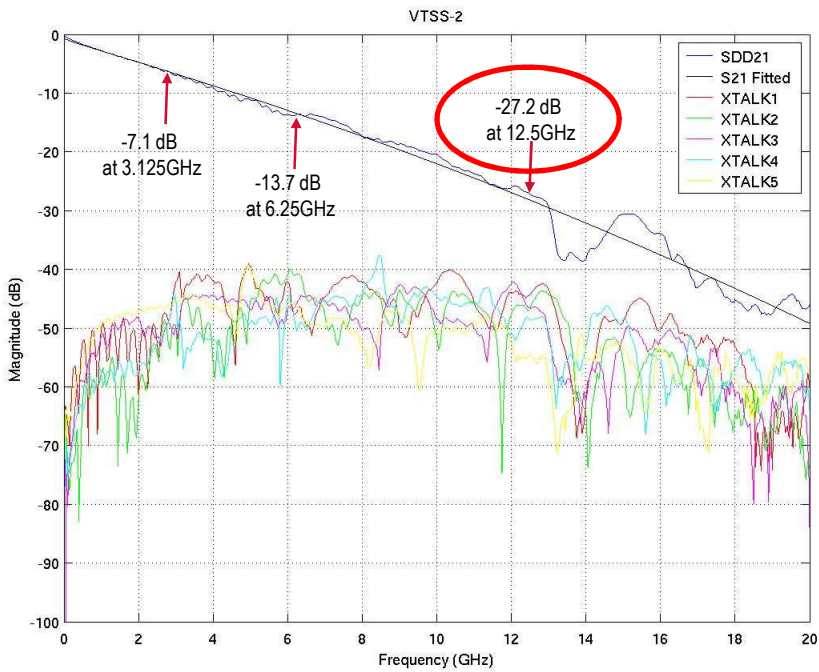
25 Gb/s Backplane Channels: Initial Insight

- ▶ The Study Group should first reach consensus on clear objectives regarding the reference channel models based on end users' input.
- ▶ Early visibility into 25 Gb/s backplane channels reveals 2 categories:
 - ▶ Legacy 10 Gb/s designs
 - Long lengths ($\approx 30''$)
 - 10G-generation trace material
 - 10G-generation connectors
 - Example case study: VTSS-1
 - ▶ New/Upgraded designs
 - Intermediate and short lengths ($\approx 20''$ and $10''$)
 - Backwards compatible
 - 10G-generation trace material
 - Improved connectors
 - Example case study: VTSS-2 and VTSS-3

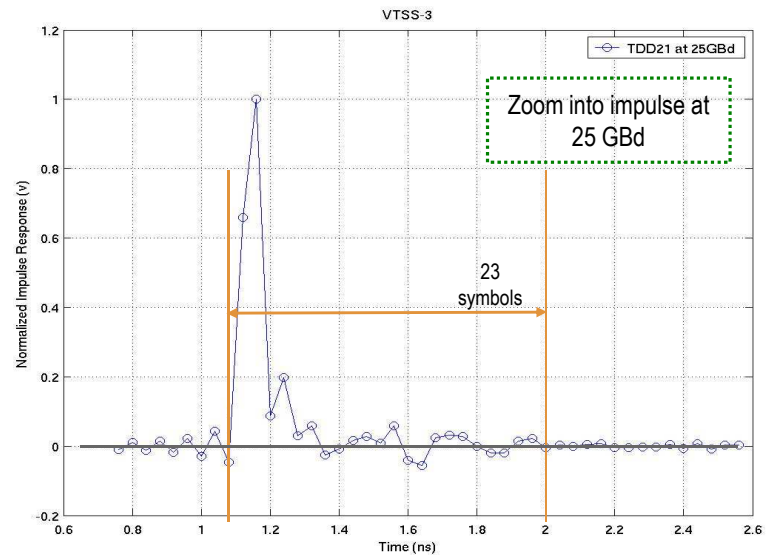
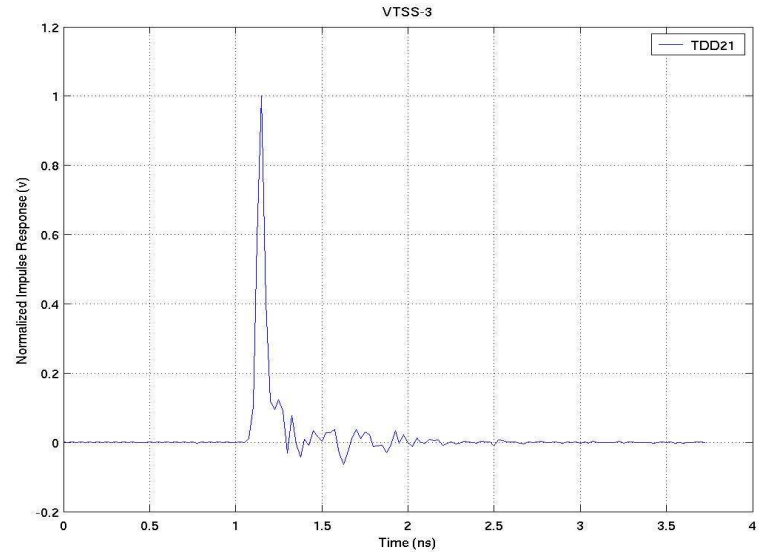
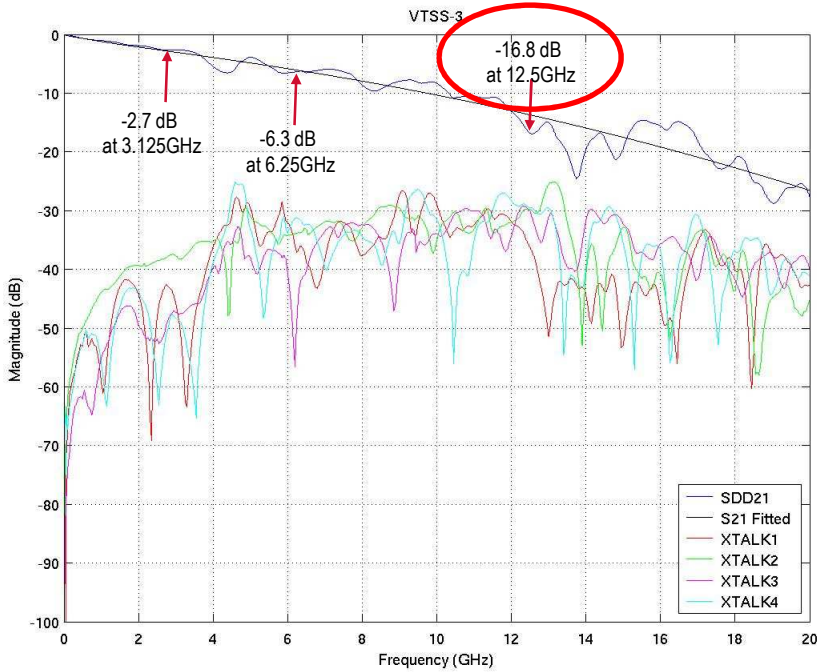
Backplane Channel: VTSS-1 (LR Traces)



Backplane Channel: VTSS-2 (IR Traces)



Backplane Channel: VTSS-3 (SR Traces)



Equalization and Modulation

- ▶ Equalization Requirements:
 - ▶ Approximate equalizer size derived from impulse responses sampled at 25GHz:
 - Legacy designs: \approx 25 equalizer taps
 - Upgraded designs: \approx 20 equalizer taps
 - ▶ Rx equalizer only.
 - ▶ Combination of Tx equalizer and Rx equalizer.

- ▶ Potential Line Codes to Consider and Compare:
 - ▶ NRZ:
 - Viable with next-generation trace materials and connectors.
 - ▶ Duobinary:
 - Potentially outperform NRZ coding at high data rates with similar complexities.
 - ▶ PAM-4:
 - More complex coding scheme at half the baud rate.

- ▶ Ultimately, time-domain simulations are required to determine best equalization and to compare line codes.

Criteria for Line Code Comparisons

- ▶ When comparing multi-level and NRZ codes using time-domain simulations, pay attention to:
 - ▶ Transmit Power:
 - Same V_{pp} : NRZ at a launch power advantage.
 - Same V_{RMS} : all line codes should have similar TX launch power.
 - ▶ Equalizer Convergence: Different modulation schemes tend to have different adaptive (LMS) equalizer convergence rates. Use ideal (LS/MMSE) equalizer results in conjunction with LMS equalizer results, especially on difficult channels requiring long simulation time for convergence.
 - ▶ Signal to Noise ratio (SNR): absolute SNRs are irrelevant, compare SNR margins at given BER:

$$SNR_{\text{margin}} = SNR_{\text{actual}} - SNR_{\text{required}}$$

Line Code Summary

Line Code	Bit Rate (Gb/s)	Symbol Alphabet (a_k)	Tx V_{PP} (v)	Tx V_{RMS} (v)	Baud Rate (GHz)	Nyquist freq. (GHz)	Approx. VTSS-1 channel loss at Nyquist (dB)	Rx Slicers
NRZ	25	$\{\pm 1\}$	2	1	25	12.5	-38.4	1
Duobinary	25	$\{\pm 1, 0\}$	2	0.5	25	12.5	-38.4	2
PAM-4	25	$\{\pm 1, \pm 1/3\}$	2	0.56	12.5	6.25	-21.6	3

FEC and Crosstalk Cancellation

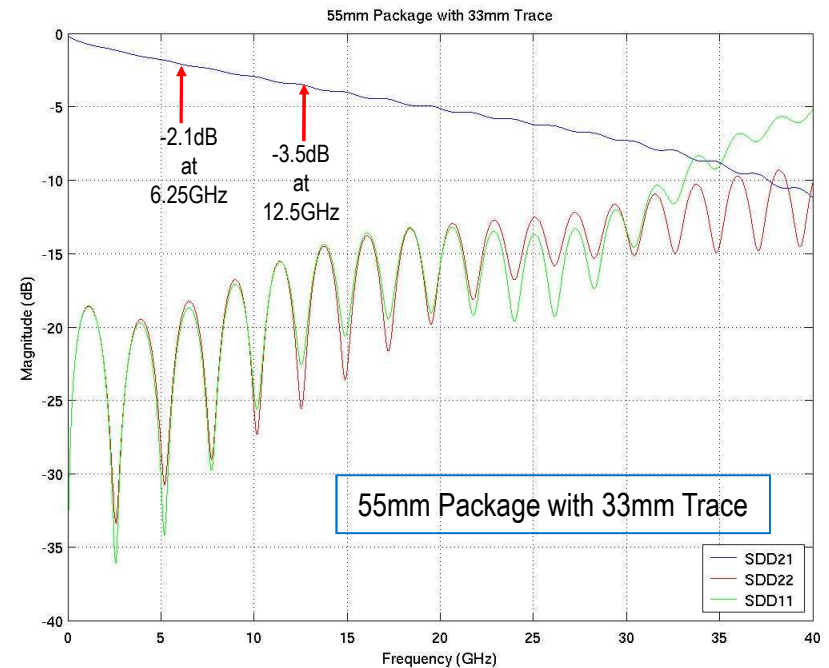
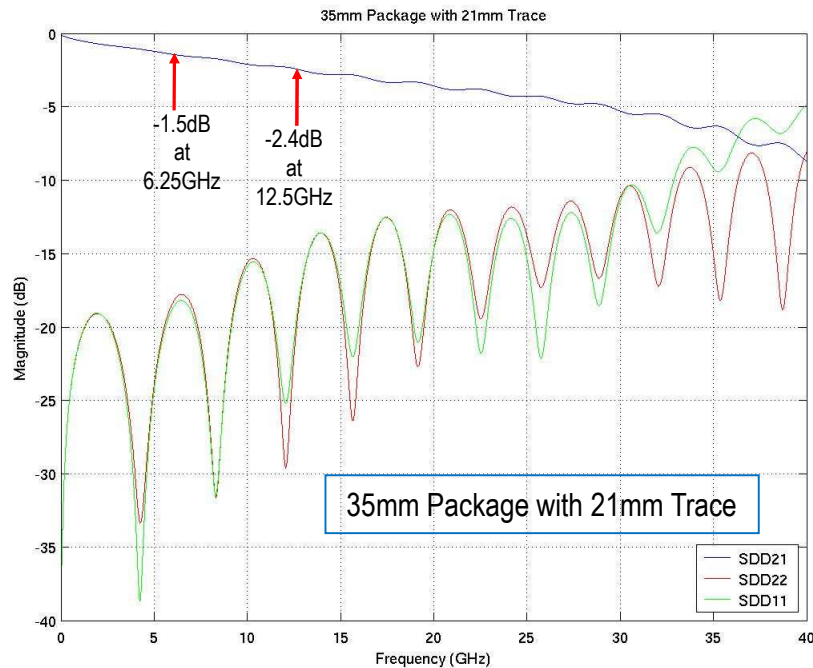
▶ Forward Error Correction (FEC)

- ▶ Burst-Error-Correcting codes provide 2-3 dB of net electrical coding gain (NECG):
 - Low-latency and low-power (Fire/cyclic codes).
 - Common implementation handles single bursts.
 - Example: 10GBASE-KR FEC
- ▶ Burst-and-Random-Error-Correcting codes provide 5-7 dB NECG:
 - Higher latency and higher power/complexity (Reed-Solomon codes, BCH codes, concatenated codes, etc.)
 - Example: RS(255,239) FEC
- ▶ Enhanced Burst-and-Random-Error-Correcting codes provide >7 dB NECG:
 - LDPC, Turbo Codes, Interleaved codes, etc.
 - Example: G.975 codes such as Vitesse CI-BCH FEC

▶ Crosstalk Cancellation

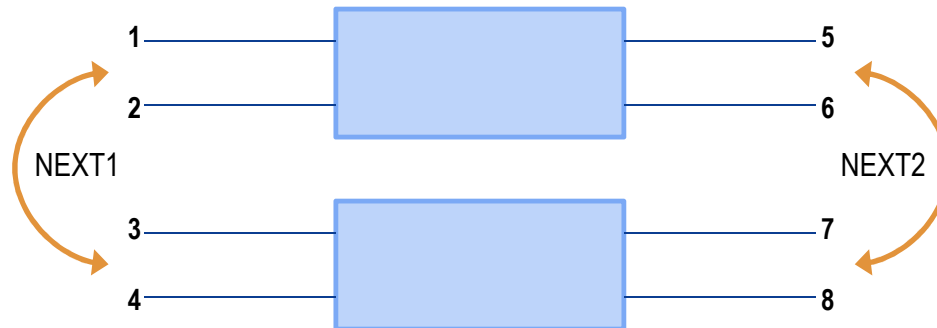
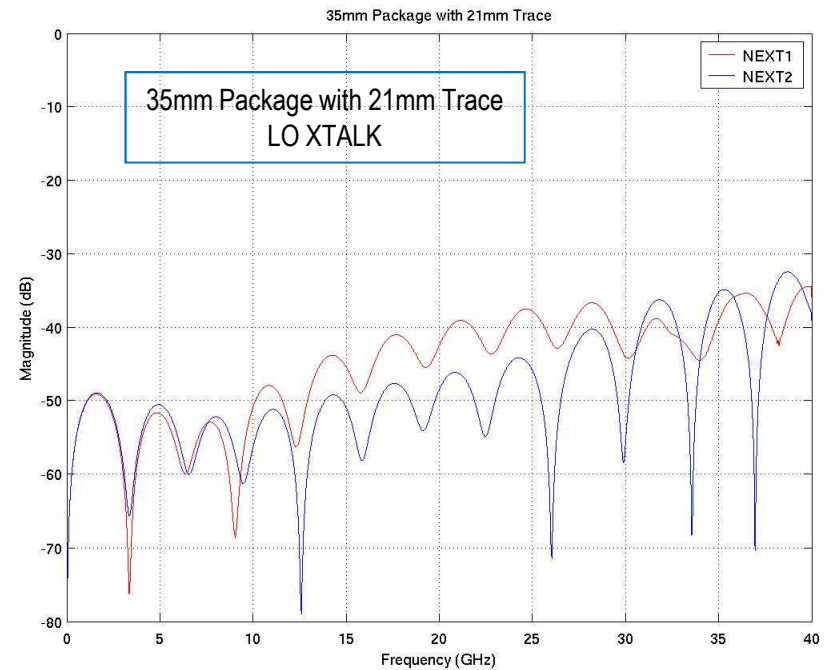
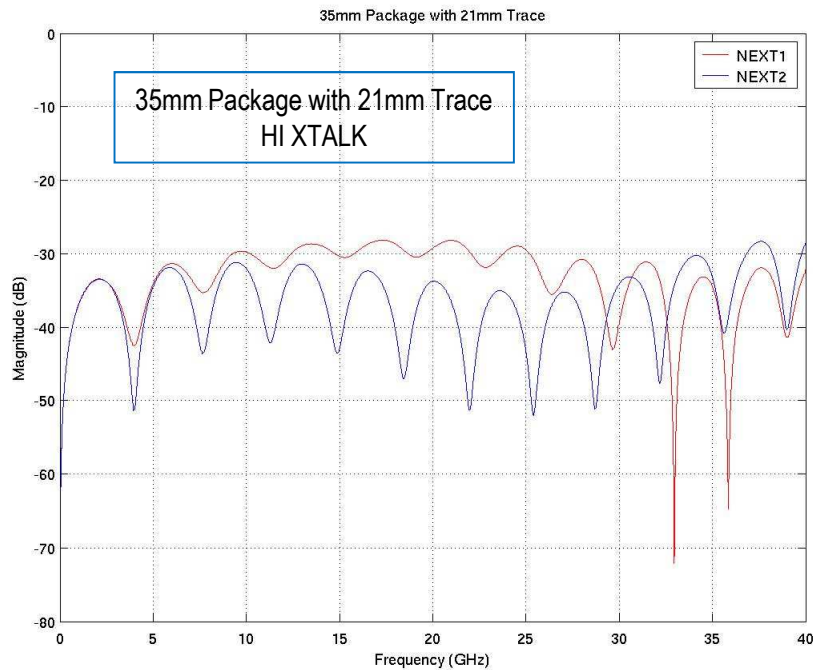
- Crosstalk canceller block requires access to aggressor waveforms:
 - Better suited for near-end crosstalk cancellation.
 - For some applications, NEXT is no longer an issue because of physical separation at pin-out level.
 - Of concern at these rates is package crosstalk.

Package Models: Insertion Loss and Return Loss



- ▶ At 25 Gb/s serial over backplanes, packaging insertion loss, return loss, and possibly crosstalk become important factors:
 - ▶ Package IL favors multi-level line codes.
 - ▶ Package RL not as deterministic and has large variations.
 - ▶ Package models above provided courtesy of IBM:
 - www.ieee802.org/3/ba/public/tools/PkgModels40GHz.zip

Package Models: Crosstalk



Conclusions

- ▶ Strong market demand for 25 Gb/s serial over backplanes.
- ▶ The Study Group should first reach consensus on clear objectives regarding the reference channel models based on end users' input:
 - ▶ Current Vitesse backplane channels limited to 30" in length with mostly 10G-era components.
- ▶ It is technically feasible to transmit 25Gb/s serial over backplanes:
 - ▶ Multi-level coding techniques need to be considered in addition to NRZ:
 - The pro and cons of various line coding schemes need to be carefully taken into account.
 - When comparing NRZ and multi-level coding schemes, keep playing field as leveled as possible.
 - ▶ Consider economic feasibility.
- ▶ Need to specify package models for specific process node:
 - ▶ At 25 Gb/s serial over backplanes, packaging insertion loss, return loss, and possibly crosstalk become important factors.
- ▶ FEC will most likely be needed:
 - ▶ Mandatory or optional depending on line code and channel reach.
 - ▶ Investigate codes with "mid-range" NECGs (3-5 dB) while keeping latency low.