FEC Triple Tradeoffs & 100GCU SG Objectives

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Exploring the FEC Triple tradeoff

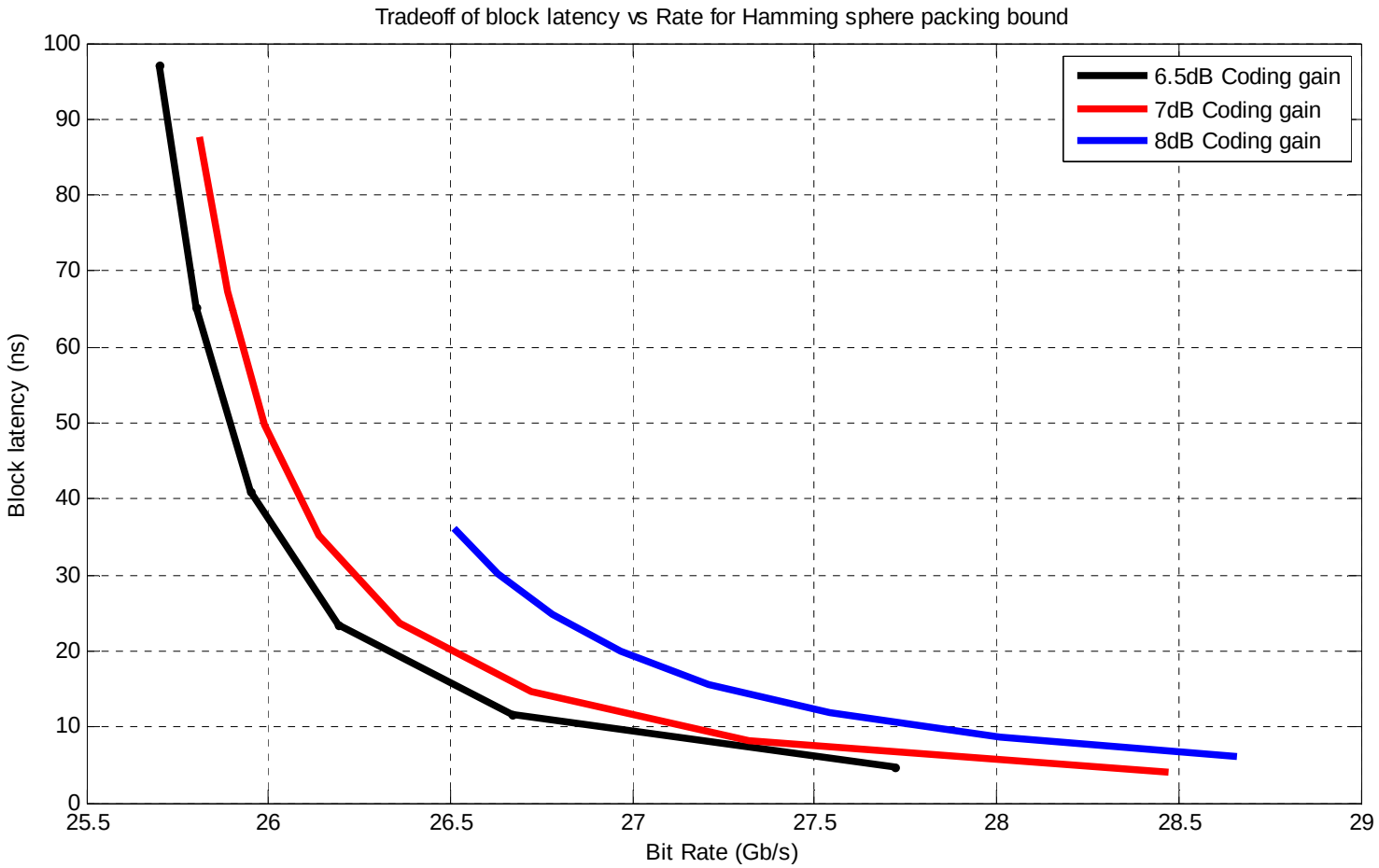
- FEC improves link performance but adds latency and complexity
- The spreadsheet on the next page explores the triple tradeoff of:
  - Latency
  - Coding gain
  - Over clocking
- No specific code is proposed
  - Theoretical limits are explored with the Hamming sphere packing bound
    - This bound is the lowest over clocking that one can get from any FEC for a given block size and coding gain
  - Practical binary BCH codes are then compared
    - Close to the hamming bound for random error correction
  - Reed Solomon Codes operating on larger symbols can provide good compromise between random error correction and burst error correction
  - A family of codes that provides 4-9dB coding gain with 4 to 70ns of block latency (does not include processing latency) are listed in the spreadsheet
    - Coding across physical lanes is assumed
    - Gain reduction due to the burst error characteristics of the receivers is not yet factored in

Triple tradeoff details

Spreadsheet sorted by coding gain of 4dB - 9dB

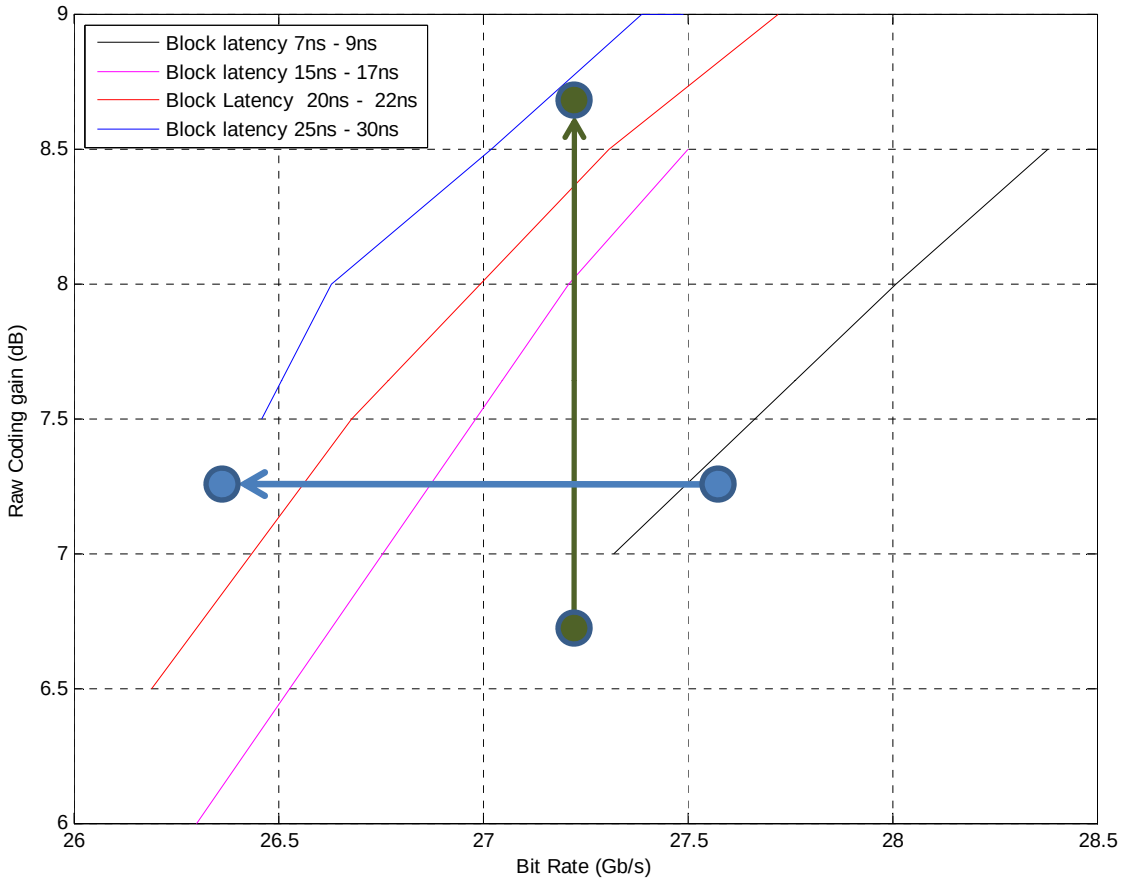
Block Latency (ns)	*Block Size (bits)*	*Required Error Correction (t)*	*Raw input BER for 1E-18 output BER*	*Raw coding gain for 1E-18 o/p BER*	*Raw input BER for 1E-15 output BER*	*Raw coding gain for 1E-15 o/p BER*	*Hamming Sphere Packing Rate (Gb/s)*	*Delta over 100GE-LR4 rate*	*BCH Rate (Gb/s)*	*BCH Delta over 100GE-LR4 rate*
41.62	4261	3	1.66E-08	**4.0**	9.26E-08	**3.7**	25.59	-0.72%	25.63	-0.61%
69.32	7098	5	4.22E-07	**5.0**	1.34E-06	**4.6**	25.60	-0.70%	25.63	-0.60%
4.80	526	5	5.70E-06	**6.0**	1.80E-05	**5.7**	27.42	6.37%	28.06	8.83%
15.14	1593	6	5.70E-06	**6.0**	1.53E-05	**5.6**	26.30	2.01%	26.49	2.74%
35.97	3724	7	5.70E-06	**6.0**	1.36E-05	**5.5**	25.88	0.40%	25.98	0.76%
4.82	535	6	1.70E-05	**6.5**	4.56E-05	**6.1**	27.72	7.53%	28.60	10.93%
11.71	1249	7	1.70E-05	**6.5**	4.04E-05	**6.1**	26.67	3.45%	27.06	4.96%
23.39	2451	8	1.70E-05	**6.5**	3.68E-05	**6.0**	26.19	1.59%	26.43	2.50%
40.98	4253	9	1.70E-05	**6.5**	3.42E-05	**6.0**	25.95	0.64%	26.11	1.27%
65.34	6742	10	1.70E-05	**6.5**	3.21E-05	**6.0**	25.80	0.06%	25.89	0.42%
8.29	906	8	4.60E-05	**7.0**	9.96E-05	**6.6**	27.32	5.97%	27.85	8.02%
14.71	1572	9	4.60E-05	**7.0**	9.24E-05	**6.5**	26.72	3.63%	27.10	5.10%
49.78	5176	12	4.60E-05	**7.0**	7.93E-05	**6.5**	25.99	0.82%	26.18	1.55%
14.29	1543	11	1.10E-04	**7.5**	1.98E-04	**7.0**	27.00	4.73%	27.55	6.87%
20.28	2165	12	1.10E-04	**7.5**	1.90E-04	**7.0**	26.68	3.50%	27.20	5.50%
36.02	3789	14	1.10E-04	**7.5**	1.77E-04	**6.9**	26.30	2.01%	26.57	3.05%
15.63	1701	14	2.45E-04	**8.0**	3.95E-04	**7.5**	27.21	5.56%	27.92	8.29%
24.82	2659	16	2.45E-04	**8.0**	3.75E-04	**7.4**	26.78	3.88%	27.37	6.15%
36.20	3839	18	2.45E-04	**8.0**	3.61E-04	**7.4**	26.51	2.82%	26.90	4.36%
23.61	2564	20	5.00E-04	**8.5**	7.13E-04	**7.9**	27.15	5.30%	28.01	8.66%
31.09	3346	22	5.00E-04	**8.5**	6.94E-04	**7.9**	26.90	4.35%	27.57	6.92%
44.00	4691	25	5.00E-04	**8.5**	6.73E-04	**7.9**	26.65	3.38%	27.28	5.82%
36.50	3965	31	1.00E-03	**9.0**	1.29E-03	**8.4**	27.16	5.34%	28.02	8.68%

Latency vs. Over Clocking



- The block latency increases sharply as the rate approaches 100GE-LR4 rate

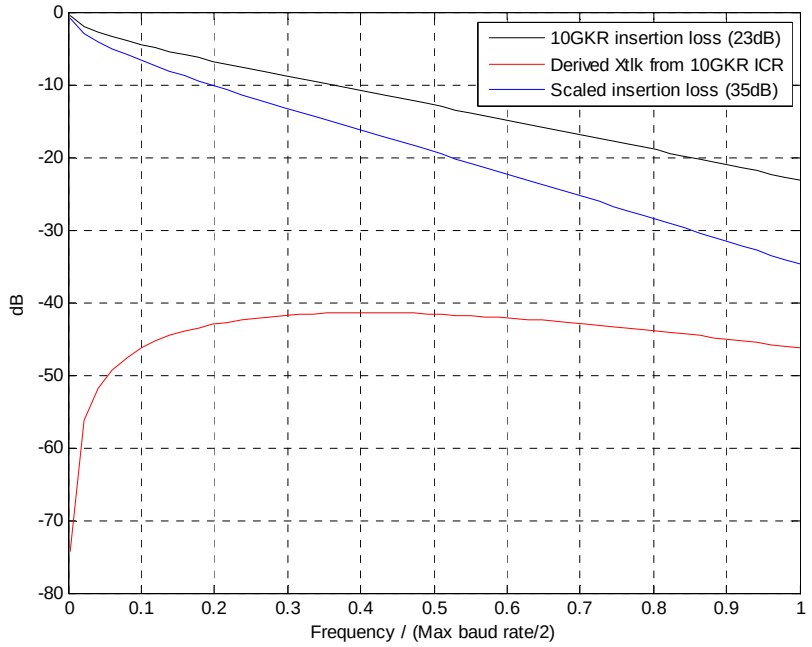
Coding gain vs. Over Clocking

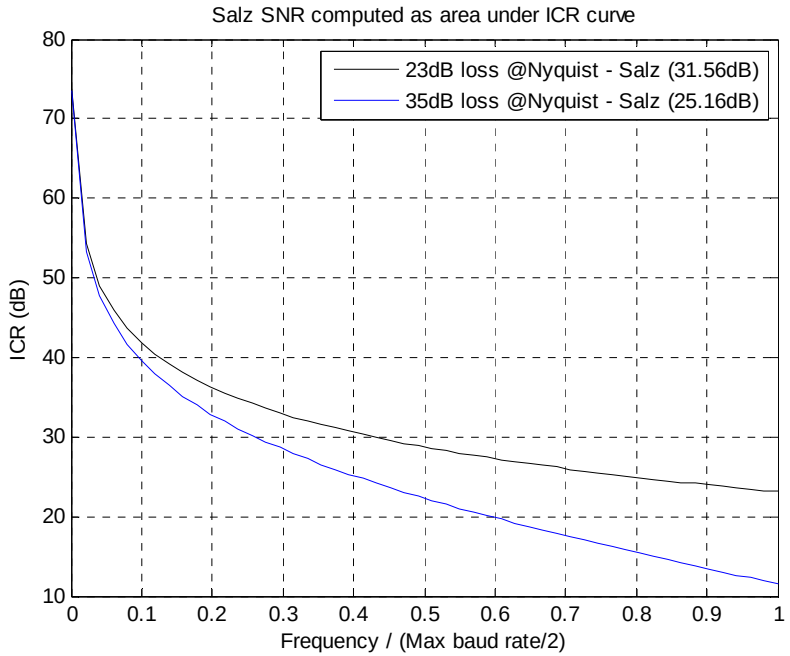


- For a given Rate (say 27.3Gb/s), a small increases in latency (7ns to 25ns) brings large coding gain (2dB)
- For a given coding gain (say 7.5dB), a small latency increase brings a significant rate reduction

Relating FEC to 100GCU SG Objectives

- Reach objective, technical feasibility and broad market potential can be improved by use of FEC
  - An x dB coding gain from FEC can theoretically improve the insertion loss by 2x dB (See Will Bliss, bliss_01_0111.pdf for details on Salz SNR below)
    - Examples: 6dB FEC coding gain means we can extend the KR insertion loss limit of 23dB at Nyquist frequency to 23 + 6 * 2 = 35dB
    - Note that this does not take into account all impairments, actual achievable gain is likely less





Relating FEC to 100GCU SG Objectives

- BER objective
  - FEC could be used to support a BER objective of 10^{-12} with high loss links if we decide to set our BER objective to 10^{-12}
  - FEC can also be used to optionally support a better BER (10^{-15} or 10^{-18} etc) for those applications that require it
  - FEC can allow for a better BER objective without requiring long test times
  - We could decide to always send FEC encoded blocks, and whether to correct or not in the receiver can be based on the application's needs

Relating FEC to 100GCU SG Objectives

- Latency (Data Delay) objective
  - Previous 802.3 projects did not have a latency objective. However, low latency is now a critical need for some networking applications.
  - There are many FEC codes that can support a stringent latency requirement
  - Many codes with 6-8dB of coding gain have an intrinsic latency of 7-18ns when the FEC blocks encode data from all 4 lanes
    - An over clocked rate up to 28G greatly helps in the triple tradeoffs
    - KR triples the intrinsic latency of QC(2112, 2080) to max of 614.4ns as per clause 74.6
      - Including processing delay, the latency for codes under consideration is 21-54ns when encoded across all 4 lanes

Thanks!