

Technical Feasibility for 100GBASE-CR



Tom Palkert

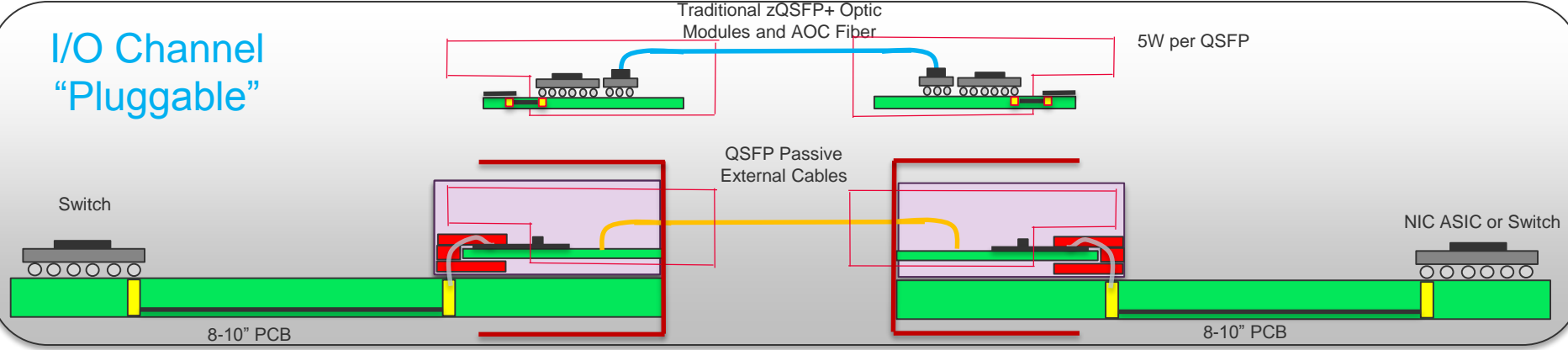
1

Jan 2018

molex[®]
one company ▶ a world of innovation

Today @ 25Gbps lanes

I/O Channel
"Pluggable"



Assumes same trace length on both sides of interconnect

56Gbps PAM4 Channel Link Budget (ball to ball)

Traditional 56 Gbps, $f_0=14$ GHz

Parameter	Loss
External cable loss (5m) (26 AWG)	16 dB
2 Host PCB trace (9" Megtron 6)	2 x 7.3 dB
2 Connectors	2 x 1.2 dB
2 Module PCB & capacitor & termination	2 x 1.5 dB
Total channel loss	36 dB

Traditional 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG)	13 dB
2 Host PCB trace (9" Isola Tachyon)	2 x 13.5 dB
2 Connectors	2 x 1.4 dB
2 Module PCB & capacitor	2 x 2 dB
Total channel loss	46.8 dB

- Current 25G-generation CDR/DFE/DSPs provide -36 dB loss compensation @ 14 GHz
- The traditional PCB channel is broken at 28 GHz

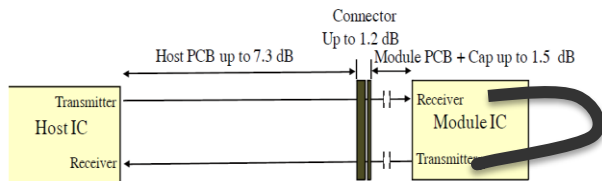
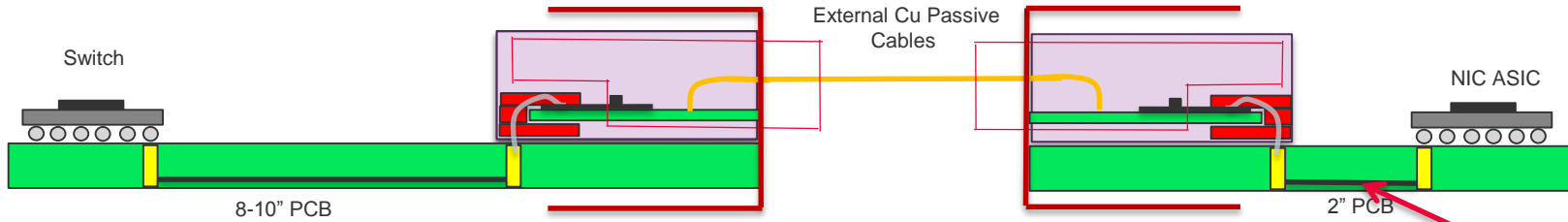


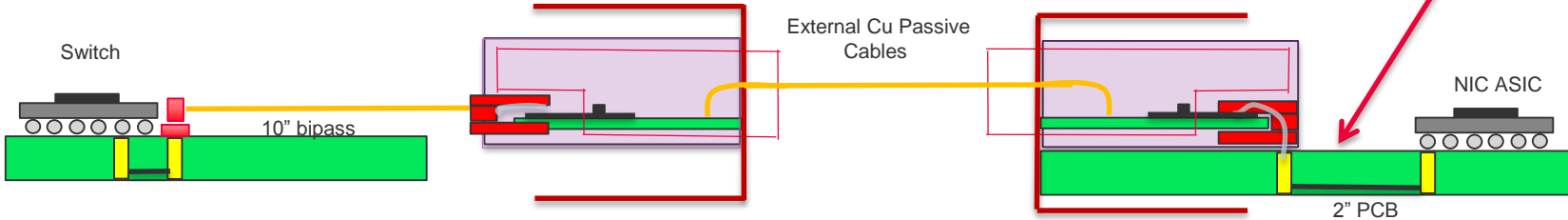
Figure 13-20. CEI-28G-VSR full Channel Reference Model

Options for 100GBASE-CR

2m external cable with PCB traces for both switch and server



2m external cable and bypass cables in switch

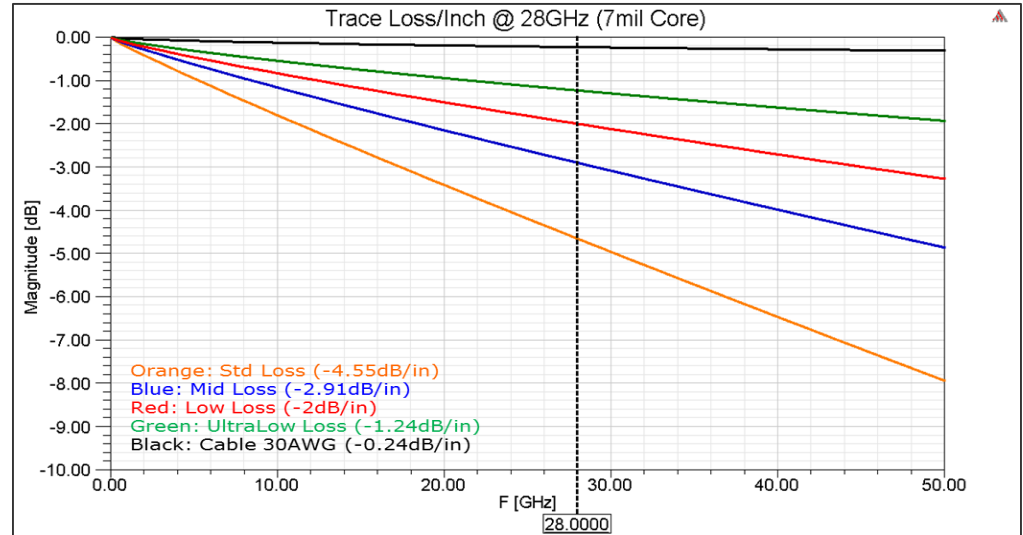


Note: short trace assumed for server

Material Loss Effect

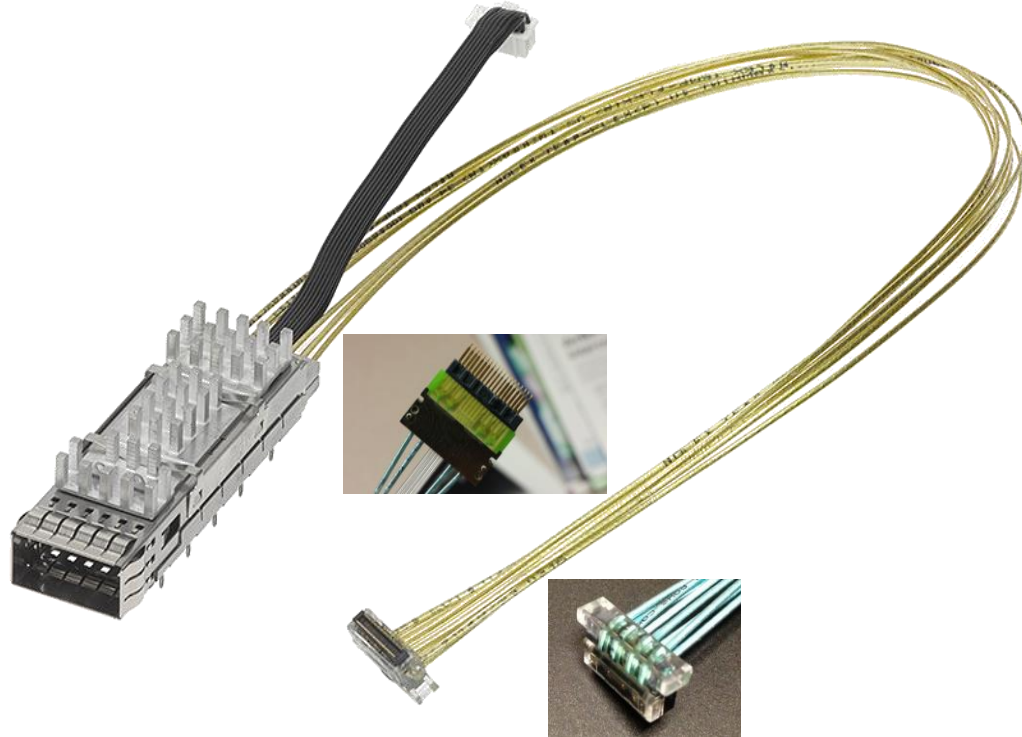
Laminate Loss Category	Df	Loss/in @ 28GHz
Standard Loss	0.024	-4.55dB
Mid Loss	0.014	-2.91dB
Low Loss (Meg6)	0.008	-2dB
Ultra Low Loss (Meg7)	0.003	-1.0 to -1.3dB
TwinAx Cable 30AWG	0.003	-0.24dB

Loss/inch for different PCB laminates and cable



- To characterize different available PCB laminates and determine the possible reach for each material.
- Loss per inch as functions of frequency up to 50 GHz and a tabulated summary of loss per inch at 28 GHz

QSFP BiPass to NearStack “VSR” Cable



Key Benefits:

- › **Lower System-Level Costs:**
 - › Eliminate the need for costly PCB materials (Nelco, Megtron, Tachyon, etc)
 - › Eliminate the use of additional DFE or retimer chips to drive long traces
 - › Improved thermal performance with 1x1 cages (air-cooled)
- › **Architectural Flexibility:**
 - › Freedom to locate ASIC anywhere (eg. further from backplane)
 - › Enable lower power ASIC
 - › Extended reach from ASIC to I/O
 - › Enable longer external copper I/O cables
 - › Cool the ports and the ASIC better
- › **New ways to handle power integrity to large ASICs**

Possible 112G-CR PAM4 Channel Link Budget

'Improved' PCB (112 Gbps, $f_0=28$ GHz)

Parameter	Loss
External cable loss (2m) (26 AWG)	13 dB
Switch PCB trace (8" Meg7) and connector	9.5 dB
NIC Host PCB trace (2" Meg6)	5 dB
2 Module PCB and capacitor and wire terminations	2x2dB
Total channel loss	31.5 dB

BiPass Cables 112 Gbps, $f_0=28$ GHz

Parameter	Loss
External cable loss (2m) (26 AWG)	13 dB
BiPass cables (10")(30 AWG) incl 'near ASIC' and QSFP connectors and 2" Meg 6	7.1 dB
NIC Host PCB trace (2" Meg6)	5 dB
2 Module PCB & capacitor & wire terminations	2 x 2 dB
Total channel loss	29.1 dB

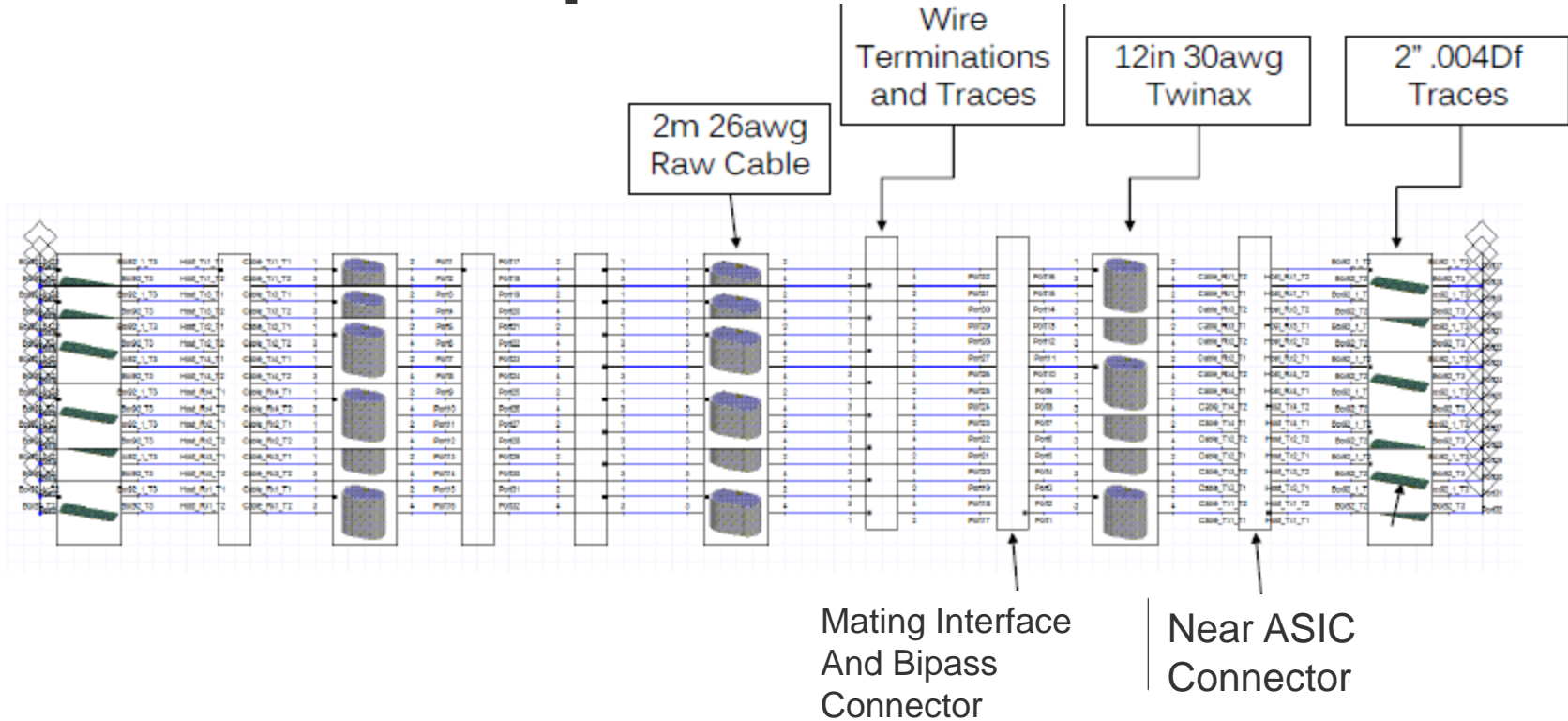
100G-CR Channel S parameters

- 'Ball to Ball' parameters
 - i.e. Package not included
- 2" PCB traces from ASIC to Bypass connection

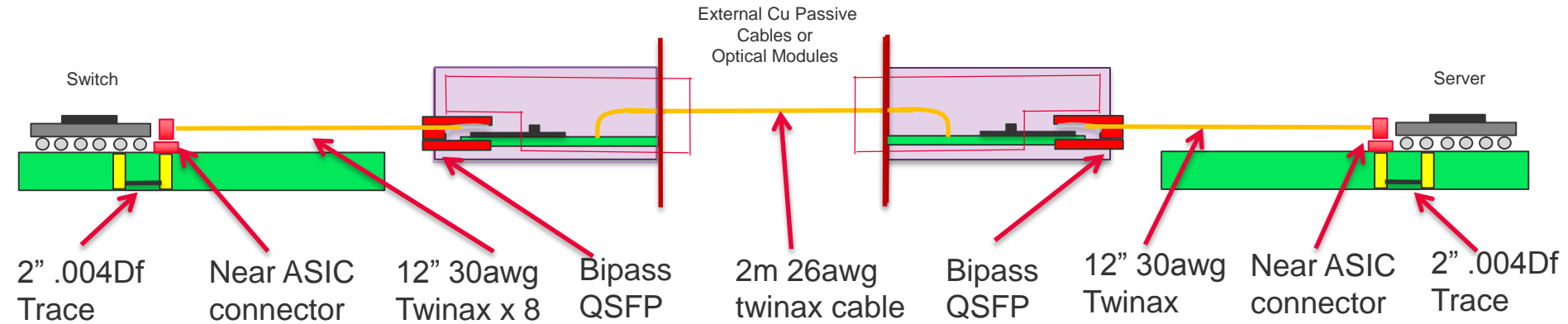
CR channel summary

- Copper Cable Connector includes entire mating interface of the paddlecard including trace routing, vias, wire terminations

Simulation set up



Simulation element breakdown



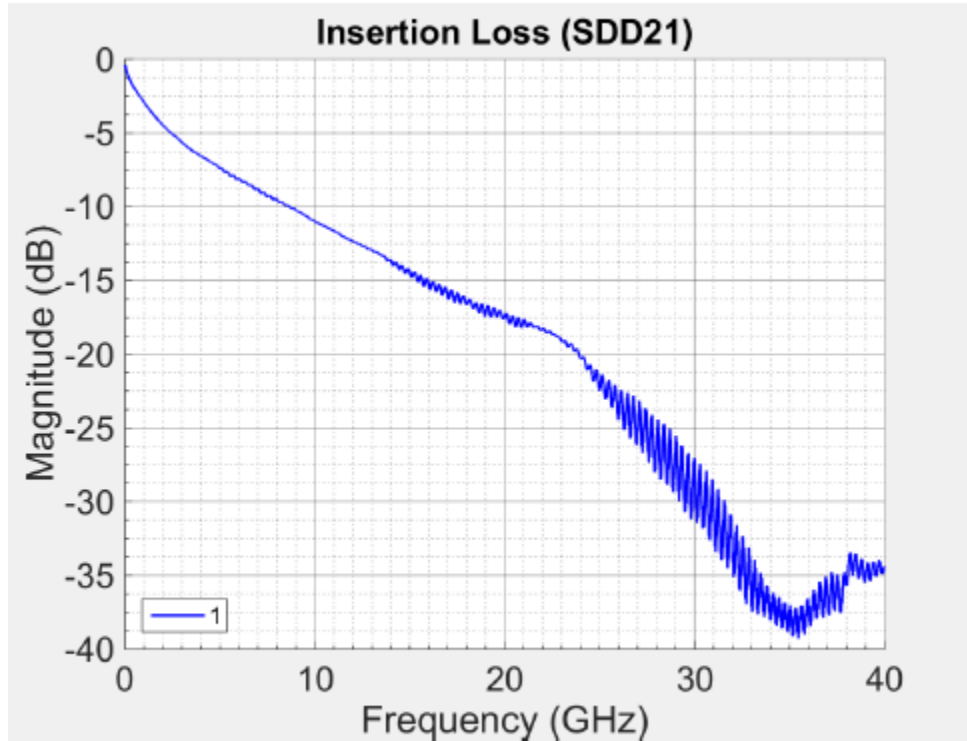
Pin mapping

➤ Cross Talk Pin Definition

- Victim pairs are on left side, differential pairs 1-8
- NEXT aggressors are on right side, differential pairs 9-16
- FEXT aggressors are on left side, differential pairs 1-8
- For TX Victim: all NEXT aggressors are RX and all FEXT aggressors are TX.
- For RX Victim: all NEXT aggressors are TX and all FEXT aggressors are RX.

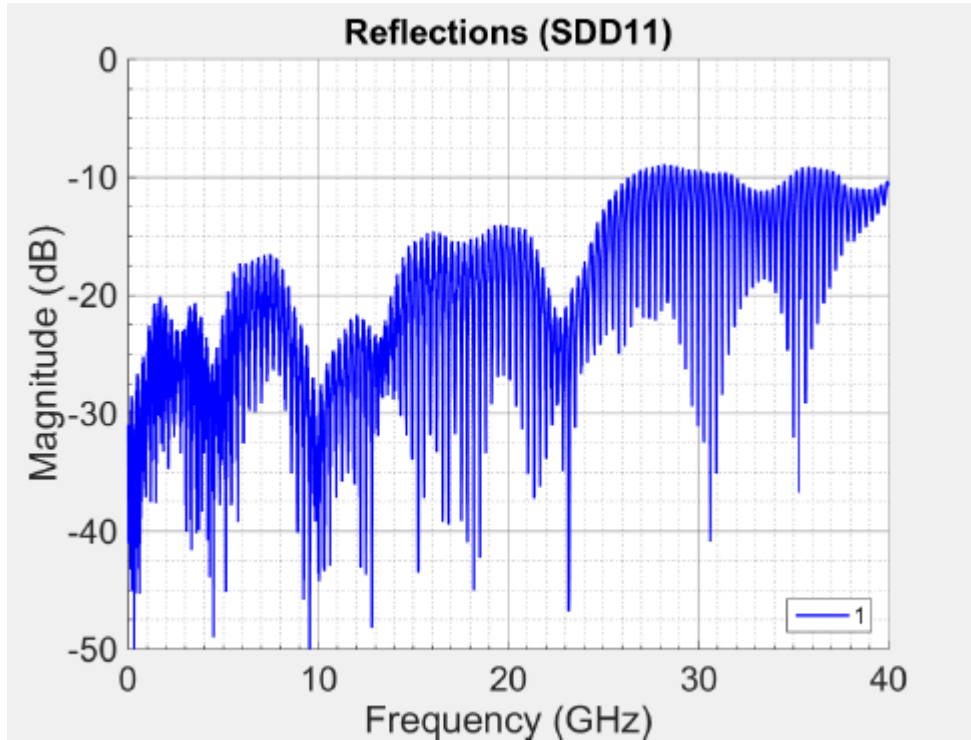
	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	--->	TX1	17,18	Diff9
	Diff 2	3,4	TX3	--->	TX3	19,20	Diff10
	Diff 3	5,6	TX2	--->	TX2	21,22	Diff11
	Diff 4	7,8	TX4	--->	TX4	23,24	Diff12
	Diff 5	9,10	RX4	<---	RX4	25,26	Diff13
	Diff 6	11,12	RX2	<---	RX2	27,28	Diff14
	Diff 7	13,14	RX3	<---	RX3	29,30	Diff15
	Diff 8	15,16	RX1	<---	RX1	31,32	Diff16

Insertion loss



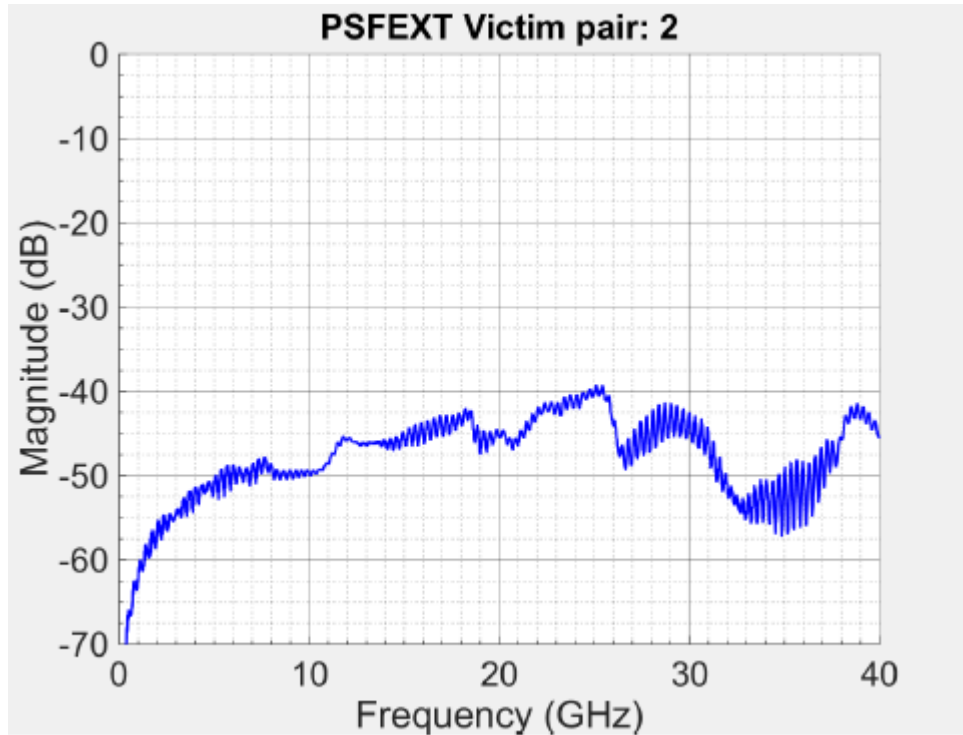
	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	→→	TX1	17,18	Diff9
	Diff 2	3,4	TX3	→→	TX3	19,20	Diff10
	Diff 3	5,6	TX2	→→	TX2	21,22	Diff11
	Diff 4	7,8	TX4	→→	TX4	23,24	Diff12
	Diff 5	9,10	RX4	←←	RX4	25,26	Diff13
	Diff 6	11,12	RX2	←←	RX2	27,28	Diff14
	Diff 7	13,14	RX3	←←	RX3	29,30	Diff15
	Diff 8	15,16	RX1	←←	RX1	31,32	Diff16

Return Loss



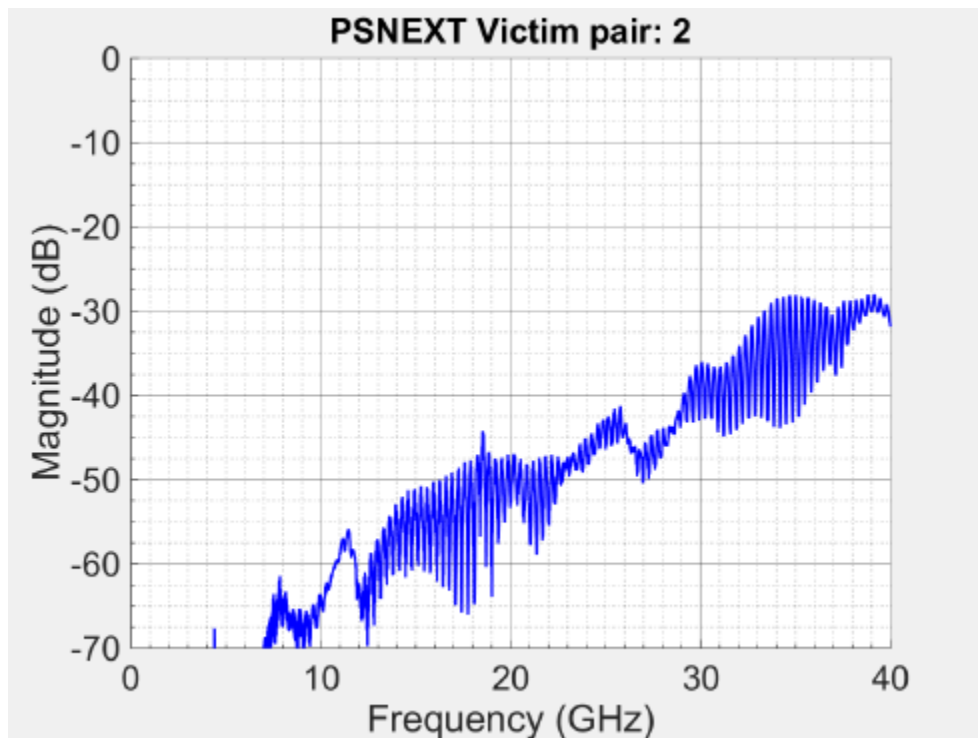
	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	--->	TX1	17,18	Diff9
	Diff 2	3,4	TX3	--->	TX3	19,20	Diff10
	Diff 3	5,6	TX2	--->	TX2	21,22	Diff11
	Diff 4	7,8	TX4	--->	TX4	23,24	Diff12
	Diff 5	9,10	RX4	<---	RX4	25,26	Diff13
	Diff 6	11,12	RX2	<---	RX2	27,28	Diff14
	Diff 7	13,14	RX3	<---	RX3	29,30	Diff15
	Diff 8	15,16	RX1	<---	RX1	31,32	Diff16

Crosstalk



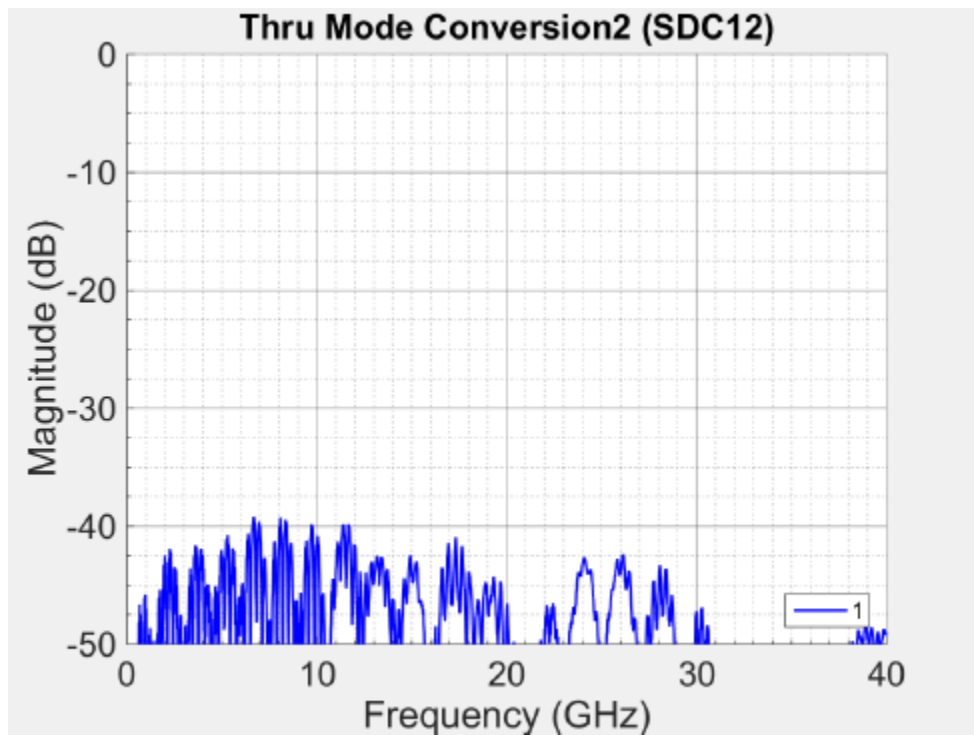
	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	--->	TX1	17,18	Diff9
	Diff 2	3,4	TX3	--->	TX3	19,20	Diff10
	Diff 3	5,6	TX2	--->	TX2	21,22	Diff11
	Diff 4	7,8	TX4	--->	TX4	23,24	Diff12
	Diff 5	9,10	RX4	<---	RX4	25,26	Diff13
	Diff 6	11,12	RX2	<---	RX2	27,28	Diff14
	Diff 7	13,14	RX3	<---	RX3	29,30	Diff15
	Diff 8	15,16	RX1	<---	RX1	31,32	Diff16

More crosstalk



	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	--->	TX1	17,18	Diff9
	Diff 2	3,4	TX3	--->	TX3	19,20	Diff10
	Diff 3	5,6	TX2	--->	TX2	21,22	Diff11
	Diff 4	7,8	TX4	--->	TX4	23,24	Diff12
	Diff 5	9,10	RX4	<---	RX4	25,26	Diff13
	Diff 6	11,12	RX2	<---	RX2	27,28	Diff14
	Diff 7	13,14	RX3	<---	RX3	29,30	Diff15
	Diff 8	15,16	RX1	<---	RX1	31,32	Diff16

Mode Conversion



	Input Port (Differential Pairs)	Pin Number	zQSFP		Nearstack	Pin Number	Output Port (Differential Pairs)
P1	Diff 1	1,2	TX1	→→	TX1	17,18	Diff9
	Diff 2	3,4	TX3	→→	TX3	19,20	Diff10
	Diff 3	5,6	TX2	→→	TX2	21,22	Diff11
	Diff 4	7,8	TX4	→→	TX4	23,24	Diff12
	Diff 5	9,10	RX4	←←	RX4	25,26	Diff13
	Diff 6	11,12	RX2	←←	RX2	27,28	Diff14
	Diff 7	13,14	RX3	←←	RX3	29,30	Diff15
	Diff 8	15,16	RX1	←←	RX1	31,32	Diff16



Thank you

molex[®]