

Power Comparison of 106Gbps Dual-Duplex and Single-Duplex PHY Architectures

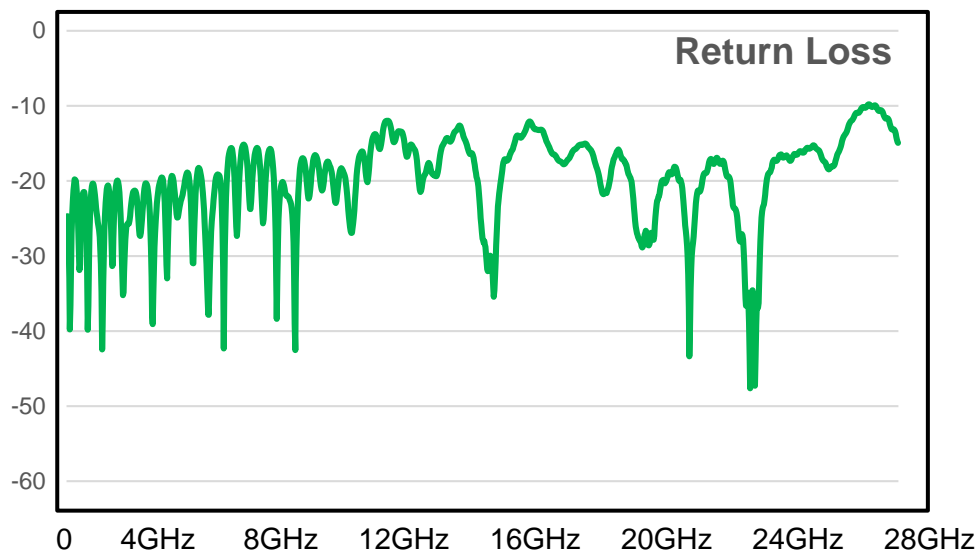
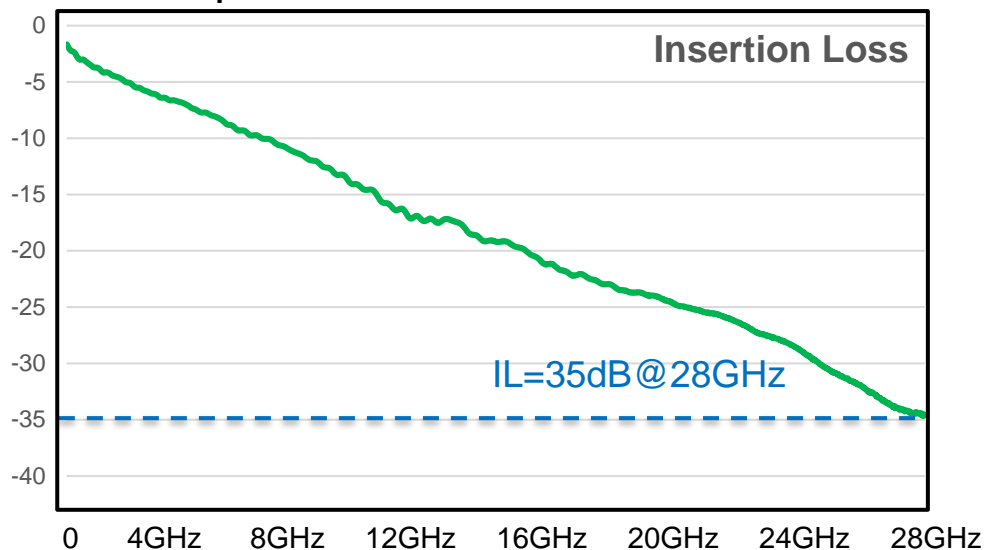
Ramin Farjadrad

SVP of R&D

March 2018, Chicago

100Gbps Power Tradeoffs Over a Common Electrical Link

Sample 20" PCB + Connector



Goal: Power comparison analysis for Single-Duplex (SD) and Dual-Duplex (DD) schemes over a common channel (shown) and common process technology node (7nm)

Dual-Duplex: 2xReceiver/2xTransmitter

- DSP: 53Gbps Equalizer + Echo Cancellers
- AFE: 53Gbps ADC/DAC/CTLE/PGA
- Clocking: 53Gbps jitter spec
- 106Gbps Mux/Demux & FEC/PCS

Single-Duplex: 1xReceiver/1xTransmitter

- DSP: 2x-4x FIR Equalizer of 53Gbps
- AFE: 2x Sampling rate/2x Gain. BW of 53Gbps
- Clocking: $\frac{1}{2}$ jitter spec of 53Gbps
- 106Gbps Mux/Demux & FEC/PCS

Digital/DSP Power Comparison over an Electrical Link

Single Duplex: PAM4 & 53Gbaud

- Assumptions:
 - ADC:8bit/6.5ENOB, Tx:1Vpk-pk,Jitter:0.15ps-rms
 - Channel Noise: -150dBm/Hz (AWGN)
 - 1-Tap DFE
 - FIR Power: 0.03mW/tap/Gbaud/data_res

FFE Taps	16 Tap	32-tap
SNR Margin	2.0	3.8

→ FFE Power:

- 32 Taps $\rightarrow 0.03 \times 32 \text{tap} \times 8 \text{bit} \times 53 \text{Gbaud} \approx 400 \text{mW}$

• Total DSP Canceller FIR Power \approx **400mW**

- 1-tap 53Gbaud DFE: More pipelining/buffering
 - $\sim 2x$ power of 1-tap 26.5Gbaud DFE

Dual Duplex: PAM4 & 26.5Gbaud

- Assumptions:
 - ADC:8bit/6.5ENOB, Tx:1Vpk-pk, Jitter:0.3ps-rms
 - Channel Noise: -150dBm/Hz (AWGN)
 - 1-Tap DFE & 64-Tap Echo Canceller
 - FIR Power: 0.03mW/tap/Gbaud/data_res

FFE Taps	8 Tap	16-tap
SNR Margin	3.94	6.54

→ FFE Power

- 8 Taps $\rightarrow 0.03 \times 8 \text{tap} \times 8 \text{bit} \times 26.5 \text{Gbaud} \approx 50 \text{mW}$

→ Echo Canceller power

- 64 Taps $\rightarrow 0.03 \times 64 \text{tap} \times 2 \text{bit} \times 26.5 \text{Gbaud} \approx 100 \text{mW}$

• Total DSP Cancellers Power $= 2 \times 150 \text{mW} \approx$ **300mW**

AFE/Clocking Power Comparison over an Electrical Link

Power Relative to SD 53G PAM4 AFE: ADC, DAC/Driver, PGA/CTLE, Clocking

Single Duplex: 1x Transceiver 53Gbaud PAM4

- ADC: $2.5 \times \text{Power} = \underline{250\text{mW}^*}$
 - 2x Parallelism \rightarrow 2x Power = 200mW
 - 53GHz S&H / 1:2DeMux \rightarrow 0.5x Power = 50mW
- DAC/Driver: 3x DAC + 1x Driver = 225mW^{*}
 - 2x Parallelism \rightarrow 2x Power = 140mW
 - 53GHz 1:2Mux PreDriver \rightarrow 1x Power = 70mW
 - Line Driver (1V pk-pk): 15mW
- PGA/CTLE: $4 \times \text{Power} = \underline{200\text{mW}^*}$
 - $2 \times \text{BW} \rightarrow \frac{1}{2} R_{\text{load}} \rightarrow \text{Gain} = G_m \cdot R_{\text{load}} = 1 \rightarrow 2 \times G_m \rightarrow 4 \times I_{\text{bias}}$
- AFE Total Estimate = 675mW^{*}
- 53Gbaud Clocking: >2x Power
 - $2 \times f_{\text{clk}}$ & $\frac{1}{2}$ Jitter $\rightarrow 2 \times \underline{CV^2 f_{\text{clk}}}$ & Bigger Buffers \rightarrow >2x Power

Dual Duplex: 2x Transceiver 26.5Gbaud PAM4

- ADC: $2 \times \text{Power} = \underline{200\text{mW}^*}$
 - 2x Transceiver \rightarrow 2x ADC = 200mW
- DAC/Driver: 2x DAC + 2x Driver = 170mW^{*}
 - 2x Transceiver \rightarrow 2x Power = 140mW
 - 2x Line Driver (1V pk-pk): 30mW
- Hybrid: $2 \times \text{Power} = \underline{100\text{mW}^*}$
- PGA/CTLE: $2 \times \text{Power} = \underline{100\text{mW}^*}$
 - 2x Transceiver at same Gain.BW \rightarrow 2x Power
- AFE Total Estimate = 570mW^{*}
 - .
- 26.5Gbaud Clocking: 2x Power
 - 2x Transceiver at same f_{clk} \rightarrow 2x Power

* Estimation based on extrapolation

Summary: DD vs. SD PHYs over an Electrical Link

- DD vs. SD Digital Power

- Same 106Gbps Mux/Demux, Datapath and FEC/PCS
- DSP power is dominated by FIR cancellers

- Dual Duplex FIRs Power \rightarrow $\sim 300\text{mW}$
 - Single Duplex FIRs Power \rightarrow $\sim 400\text{mW}$
- } Digital Delta= $\sim 100\text{mW}$

- DD vs. SD Analog Power

- DD 106Gbps AFE includes 2x 53Gbps AFE and 2x Hybrid \rightarrow DD AFE = 570mW
 - SD 106Gbps AFE at 2x BW consumes over 2x of 53Gbps AFE \rightarrow SD AFE = 675mW
- } Analog Delta= $\sim 100\text{mW}$

- A Dual-Duplex PHY can operate 106Gbps over longer-reach/higher-loss/lower-cost media than a Single Duplex PHY, while its power consumption can be as low as $\sim 20\%$ ($\sim 200\text{mW}$) lower than Single-Duplex PHY if operating over the same media

106Gbps/lane DAC Solution: SD Optical vs. DD Electrical

Active Optical DAC solution

- Reach:
 - > 10m over existing MMF
- Power: (assuming C-M is 100Gbps SD link)
 - $\sim 1.1\text{W}(\text{ASIC}) + \sim 1.1\text{W}(\text{Mod}) + \sim 2.5\text{W}(\text{Optics}) = \underline{\sim 4.7\text{W}}$
- Cost:
 - Optical DAC always much higher cost than copper counter parts
 - Not an option for backplane applications. Needs upgrade

Passive/Active Electrical DD DAC solution

- Reach:
 - Passive: >3m on 30AWG and >5m on 26AWG
 - Active: >5m on 30AWG and >10m on 24AWG
- Power: (assuming C-M is 100Gbps DD link)
 - Passive Long Reach: $\sim 1.2\text{W}$
 - Active: $\sim 1\text{W}(\text{ASIC}) + \sim 1\text{W}(\text{Mod}) + 1.2\text{W}(\text{DAC}) = \underline{\sim 3.2\text{W}}$
- Cost:
 - Enables use of existing legacy DAC cables at >3m
 - No need to upgrade backplanes

Thank you.

AQUANTIA®
ACCELERATING CONNECTIVITY™