Insertion loss target for 100 Gb/s per lane electrical PHYs

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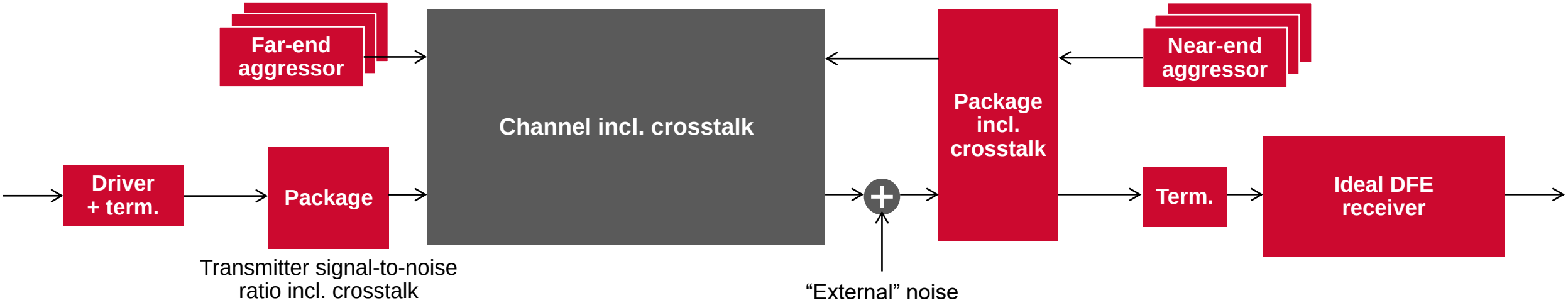
Scope and purpose

- Calculate the signal-to-noise ratio (SNR) at the receiver decision point for a large number of die-to-die channels
- Evaluate currently defined error correction schemes for 4:1 bit multiplexing with error propagation
  - 4:1 bit multiplexing is the currently defined method to achieve 100 Gb/s physical lanes
- Combine these results to derive some useful statistics relating die-to-die insertion loss to acceptable performance
- These statistics are intended to inform the Study Group for a decision on insertion loss targets for 100 Gb/s per lane electrical PHYs

Link model for Salz SNR calculations



Modeled impairments

Parameter	Value
Driver differential output amplitude (peak), V	0.4
Driver rise/fall times (20-80%), ps	6.3
Uncorrelated jitter, mUI RMS	23
Transmitter signal-to-noise ratio, dB	32.5
Far-end aggressor output amplitude (peak), V	0.4
Near-end aggressor output amplitude (peak), V	0.6
External noise spectral density (1-sided), V^2/Hz	1.6e−8
Implementation allowance, dB	6.8

Decision-point SNR for ideal DFE (a.k.a. Salz SNR)

$$SNR_{MMSE-DFE} = \frac{1}{2\pi}\int_{-\pi}^{\pi} 10\log_{10}(F(\theta)+1)d\theta$$

…where $F(\theta)$ is the folded SNR at frequency θ.

$$F(\theta) = \frac{1}{T}\sum_{m}\left|S\left(\frac{\theta+2\pi m}{2\pi T}\right)\right|^2 \qquad -\pi < \theta \le \pi$$

…and $S(f)$ is the frequency-dependent ratio of signal power to noise power.

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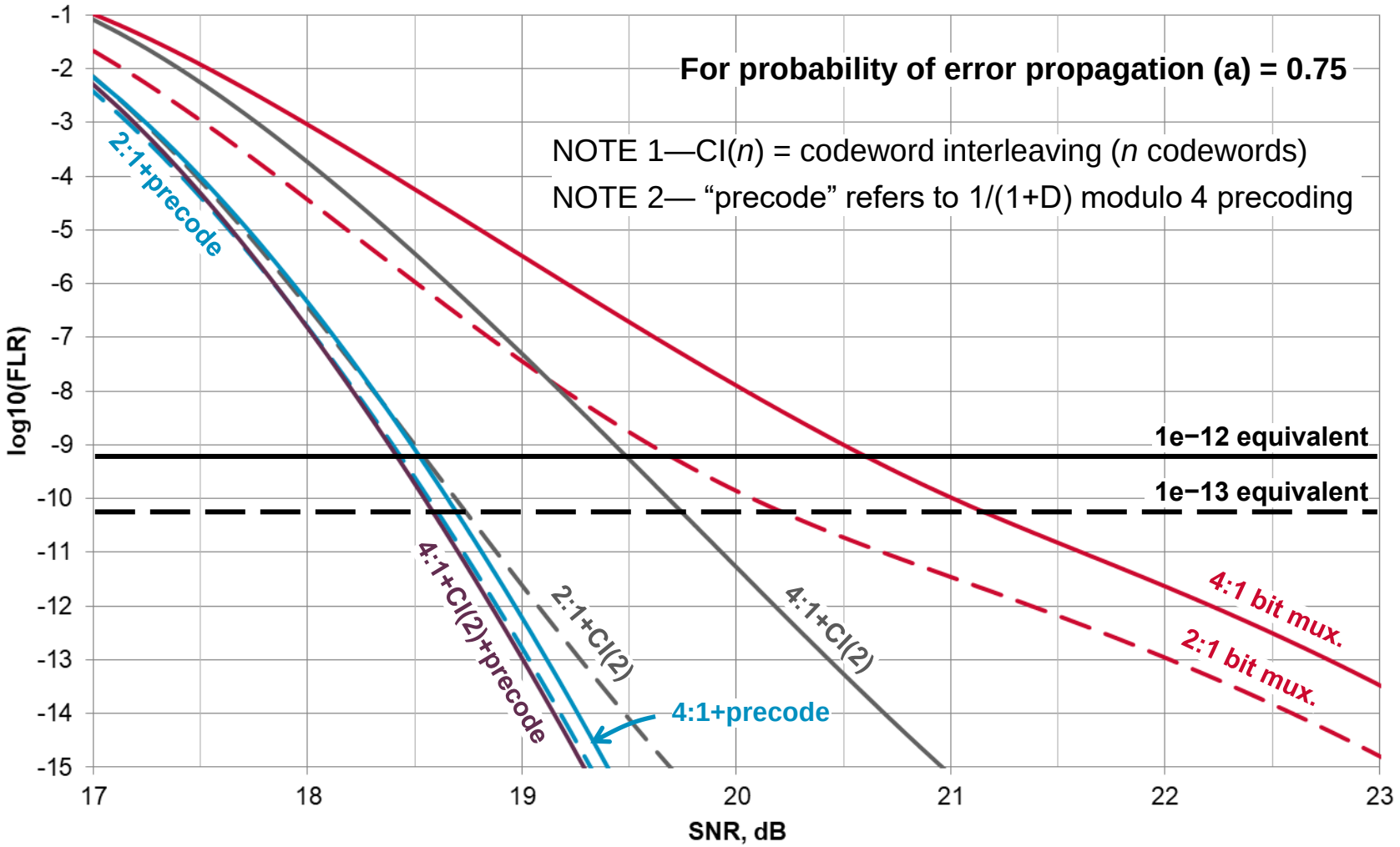
Remarks on the implementation allowance

- Salz SNR can be computed very quickly which is useful for large data sets
- However, it is an upper bound on performance and an allowance must be made for the limitations of practical receivers
  - E.g., circuit noise and distortion, receiver jitter, quantization effects, finite-length filters
- Also, the gap between Salz SNR and the decision point SNR of a practical receiver is often channel-dependent
- In this study, 6.8 dB is allocated to allow for the aforementioned limitations on receiver implementation and impairments not readily included in a Salz SNR analysis (e.g., even-odd jitter)

SNR required for target frame loss ratio

Evaluate performance of defined error correction schemes with 4:1 bit mux.



Prob. of initial PAM-4 symbol error

$$SER_1 = \frac{3}{4}\,\mathrm{erfc}\left(\sqrt{\frac{SNR}{2 \times 5}}\right)$$

PAM-4 signal variance

1e−12 equivalent (100 Gb/s Ethernet)

Test case	SNR req'd, dB
4:1 bit mux.	20.6
4:1+precode	18.52
4:1+CI(2)	19.48
4:1+CI(2)+precode	18.41

1e−13 equivalent (200/400 Gb/s Ethernet)

Test case	SNR req'd, dB
4:1 bit mux.	21.13
4:1+precode	18.69
4:1+CI(2)	19.73
4:1+CI(2)+precode	18.58

SNR target

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Data profile

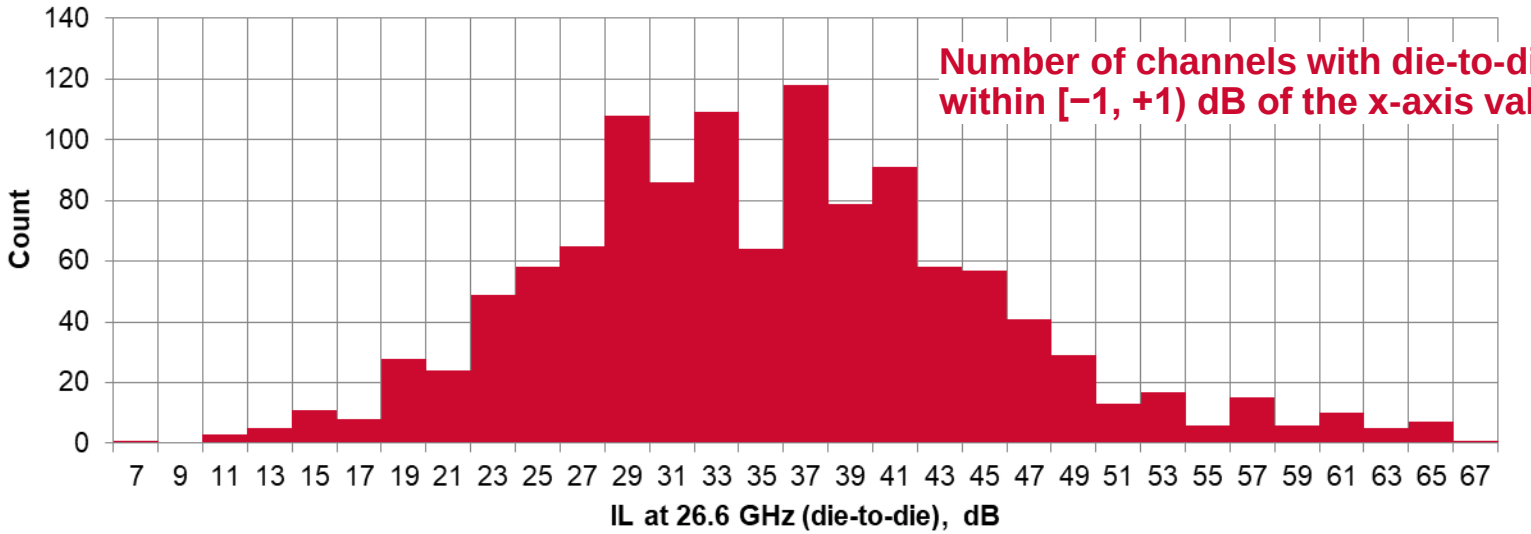
- 293 channels under consideration for 100 Gb/s support
- 4 combinations of transmitter and receiver packages (design-extracted)

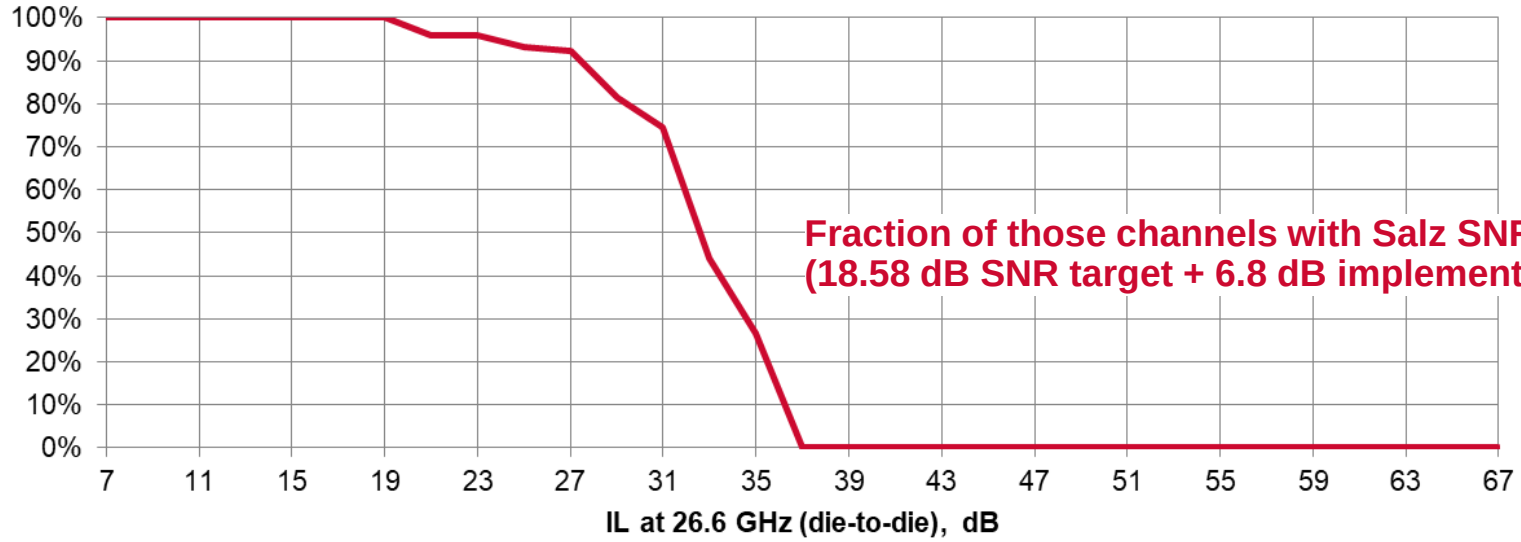
#	Transmitter	Receiver
1	Small (e.g., retimer)	Small
2	Large (e.g., net. proc.)	Large (e.g., switch fabric)
3	Medium	Medium
4	Large (e.g., switch)	Small (e.g., retimer)

NOTE – All package models include crosstalk.

- Total of 1172 test cases with die-to-die loss (at 26.6 GHz) spanning 7 to 68 dB
- On-die terminations included

Results





Percentile	IL at 26.6 GHz (die-to-die), dB
90%	27.4
75%	30.8
50%	32.6
25%	35.1

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Summary

- Error correction schemes in IEEE Std 802.3bs-2017 and IEEE P802.3cd were re-evaluated for 4:1 bit multiplexing
  - Some loss in performance for codeword interleaving has been observed.
- Pre-coding introduced in IEEE P802.3cd should be carried forward to 100 Gb/s per lane electrical PHYs as a tool to improve error correction performance
- A large number of die-to-die channels were analyzed to provide guidance to the Study Group for an insertion loss target
  - As the insertion loss increases, the solution space constricts