

# Using Chiplets to Lower Package Loss

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IEEE 802.3 100 Gb/s Electrical Lane Study Group

March 7, 2018

Brian Holden, VP of Standards

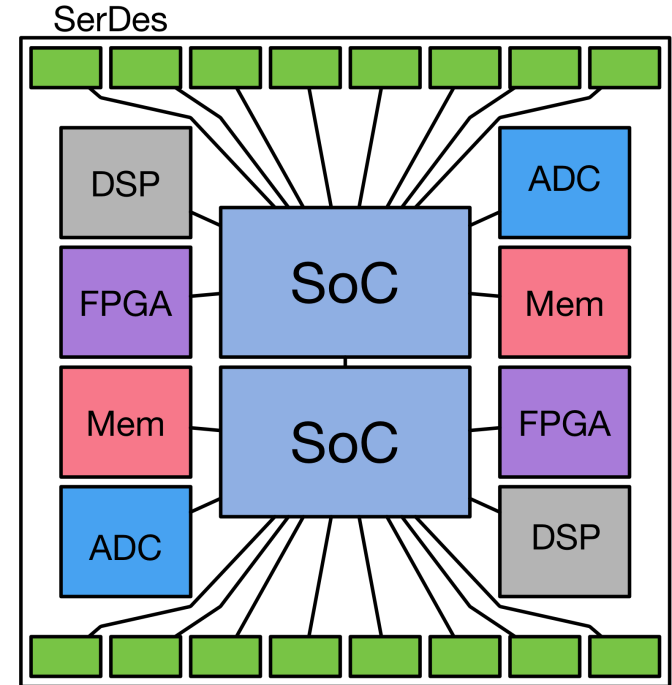
Kandou Bus SA



# Chiplet Technology

- A trend in IC technology is to move away from monolithic chips toward the use of chiplets tied together on an MCM
- Chiplets allow the:
  - Combination of many dies into large packages
  - **Improvement in yield and cost** because of a smaller central die(s) – a major factor
  - Distribution of heat away from a single die
  - Use of the best semiconductor process for each die
  - Enabling of multi-vendor ecosystems
  - **I/O subsystem dies containing SerDes to be placed around the perimeter, creating virtual smaller packages**

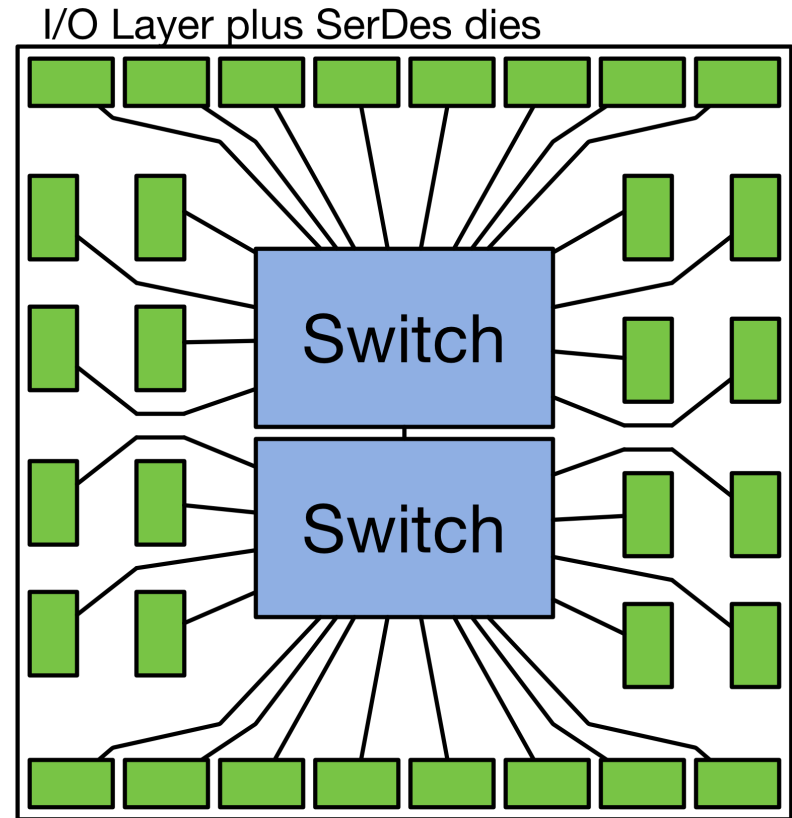
Big, 70mm packages are routine



Non-interposer MCMs can easily use 20 or more dies plus passives

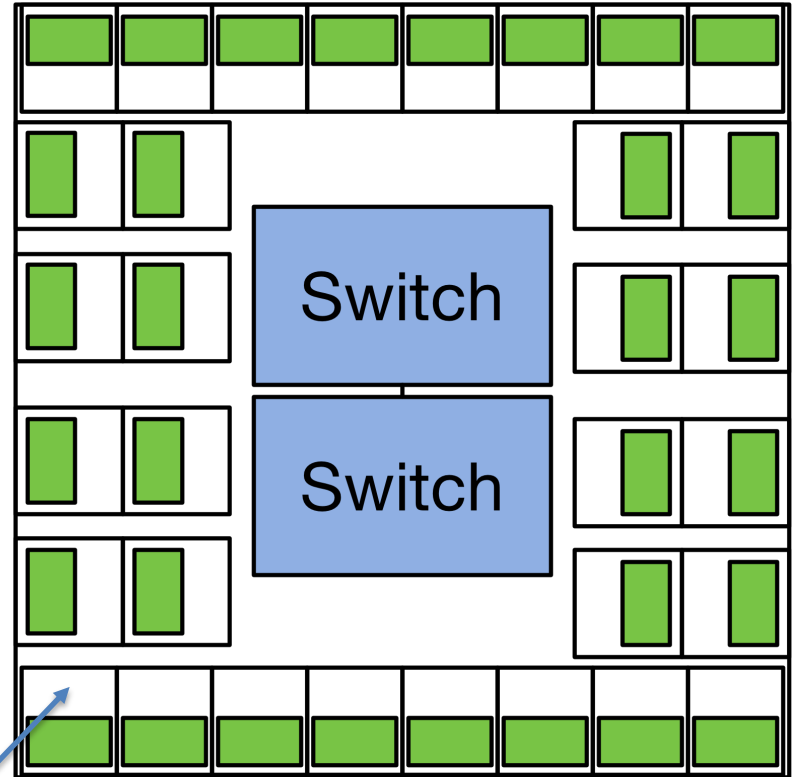
# Chipllets in Switches

- The Ethernet I/O Subsystem including the SerDes can be put on a chiplet
  - Chiplet can have the PCS, FEC and long-reach SerDes and use a fat-pipe packet protocol between devices with a little speed-up factor
    - The chiplets could alternatively use a lower or higher level protocol between devices
  - 800 Gb/s, 1600 Gb/s or 3200 Gb/s of I/O are three possible chiplet sizes
  - Switch-to-chiplet link can use a Femto SerDes
    - A chord signaling Femto SerDes is one example
    - Femto SerDes can reach to the corners of a 70 mm package



# Virtual Packages

- Putting the I/O subsystem on chiplets allows virtual packages to be created
  - Chiplet only fans out to the package balls in its immediate area
  - Looks like a small package to the system
  - The package loss budget can be reduced
  - The front panel optics interface can be modeled as being between two 12mm reach packages
  - **A 30mm reach package model is not needed**

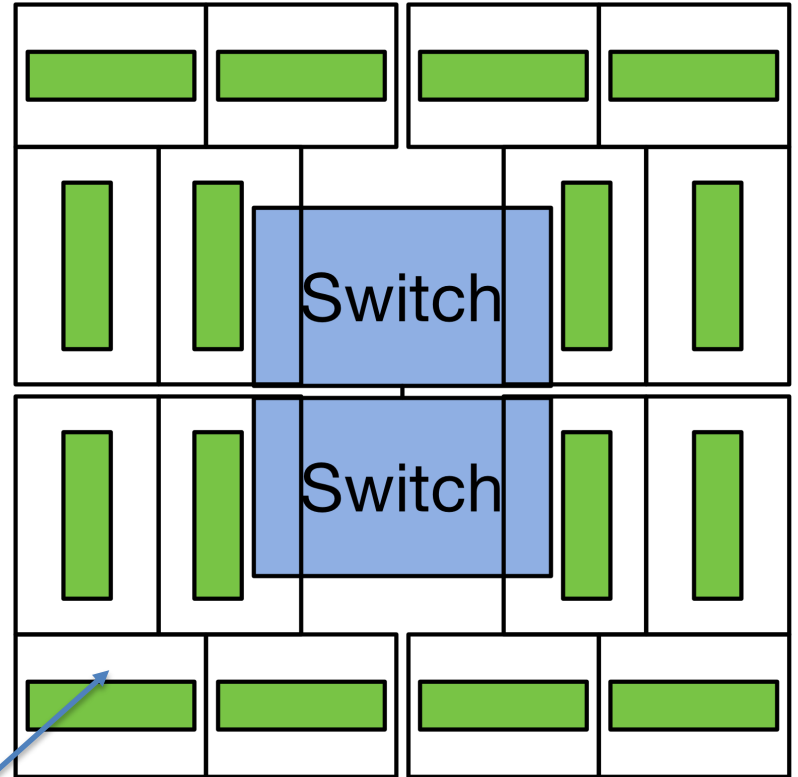


Virtual package  
Around each I/O chiplet



# Virtual Packages

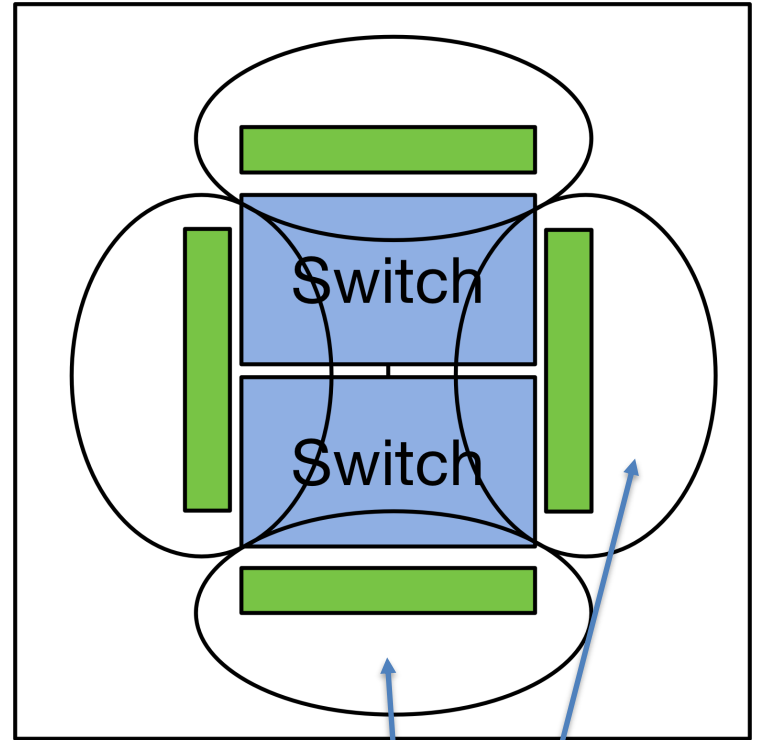
- With 16 I/O chiplets, slightly larger virtual packages are formed
  - A 30mm reach package model is still not needed



Virtual package  
Around each I/O chiplet

# Virtual Packages

- Even with shorter reach (<10mm) technology that can only get to 4/8 chiplets, virtual packages can be formed
  - Put other I/O in the four corners
  - This is representative of what micro-bump fan-out layer and silicon interposer techniques can deliver
  - **Here, a virtual package in the 20 mm reach range can be created**
- **Given that multiple chiplet solutions exist, it would be wasteful to budget for a monolithic chip solution**



Virtual package  
Around each I/O chiplet

# Package Alternatives

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# Conventional Packaging

	Conventional
Die placement	Inflexible
Signal integrity of external interfaces	<b>Worst</b> - traces must fan out to reach the perimeter package balls
Assembly Yield	Good
Number of Dies	1
Supply chain	Good

- Ideas for extending
  - Use better materials
  - Co-design the ASIC and the package
  - Tune equalizers to the fan-out trace
  - Don't try to fit so many SerDes in one package
- But there is only so much that can be done

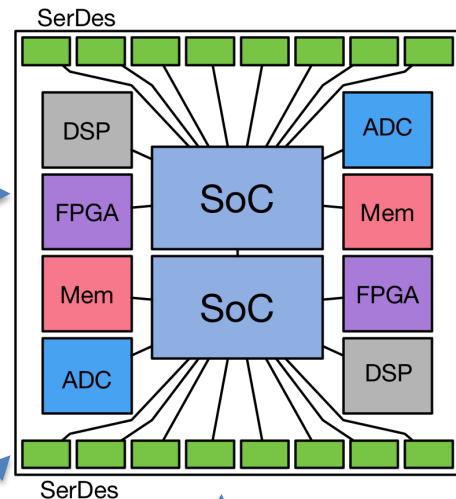
# MCM with Femto SerDes

	MCM using Femto SerDes
Die placement	Flexible because of the 2.5cm reach
Signal integrity of external interfaces	<b>Best</b> - external interface can be located close to the package balls
Assembly Yield	Made with PCB-like fabrication equipment. Well known technology with good yield
Number of Dies	Can handle many dies
Supply chain	Multiple OSATs can handle

Big, 70mm packages are routine

Can put SerDes right over the package balls

Can easily use 20 or more dies plus passives



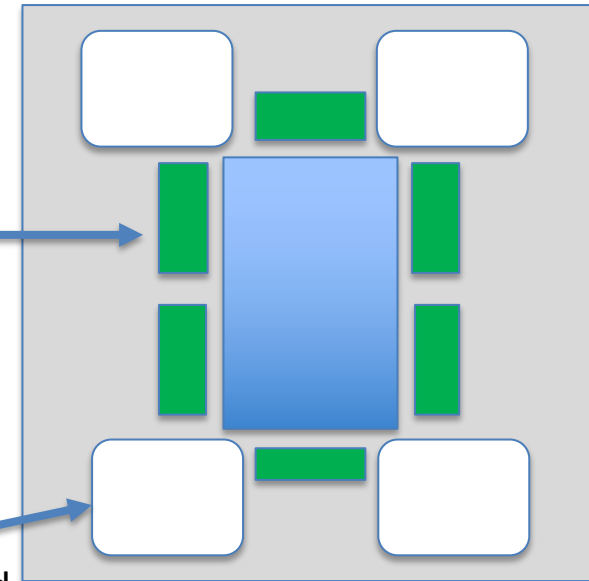
# Silicon Interposers

	2.5D interposers
Die placement	Non-flexible & strict design rules
Signal integrity of external interfaces	<b>Medium</b> - restrictions on die location may cause long traces of external high speed interfaces
Assembly Yield	Made with semiconductor fab equipment => fine pitch leads to yield loss
Number of Dies	Yield problems limit to only a few dies "Stitched" interposers are more exotic, have connection limits, and have stricter design rules
Supply chain	Specialized suppliers

Can't fill a 70mm package due to reticle size

Constraints may force non-optimal SerDes placement

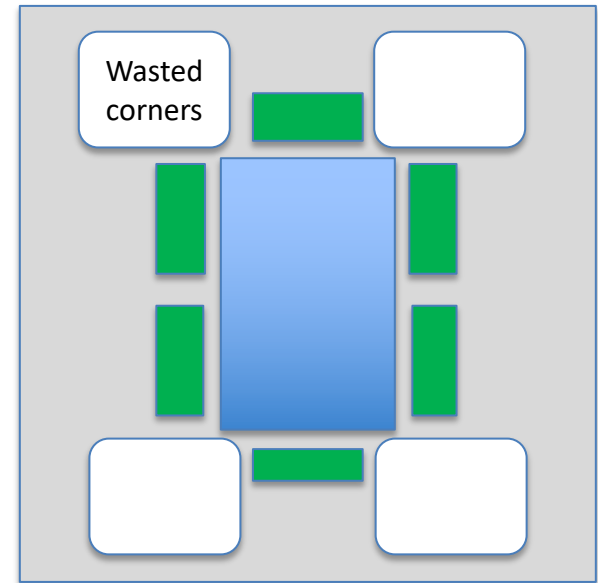
Corners tend to get wasted



# Micro-bump Fan-Out Layers

	FO-WLP, FO-PLP
Die placement	Even stricter design rules
Signal integrity of external interfaces	<b>Medium</b> - die location may cause long traces of external high speed interfaces, impacting link performance
Assembly Yield	Micro-bump fan-out layers are made with semiconductor fab equipment => fine pitch leads to yield loss
Number of Dies	Yield problems limit to only a few dies
Supply chain	Limited number of suppliers

Similarly, micro-bump fan-out layers have reticle size limits



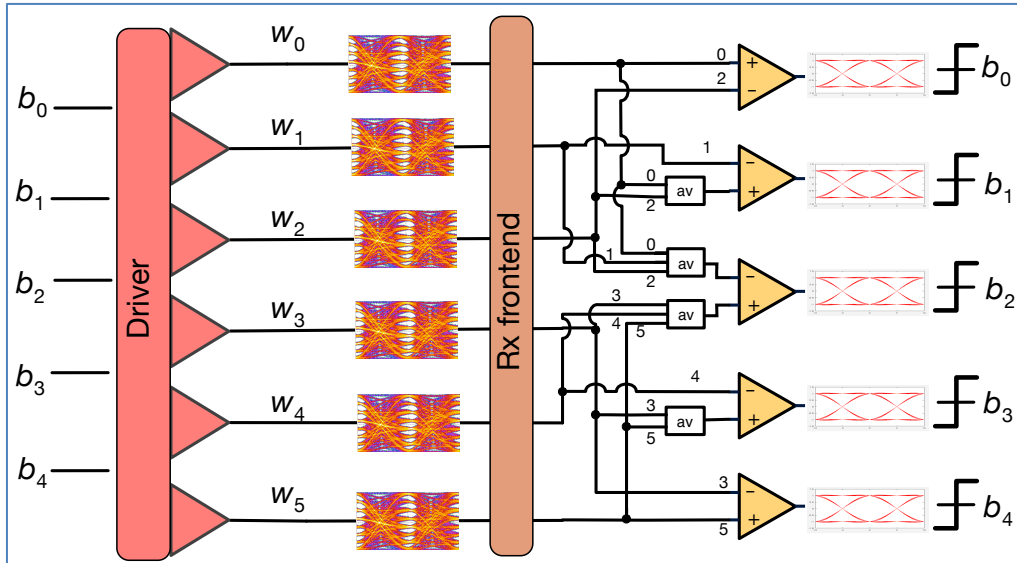
# Example Femto SerDes technology

## Chord signaling

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# CNRZ-5

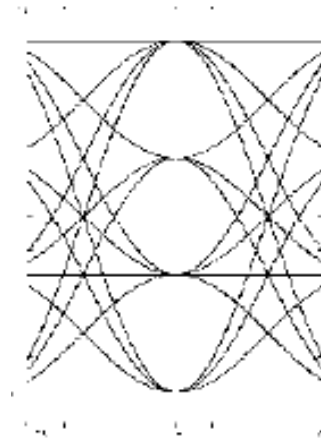


## Advantages:

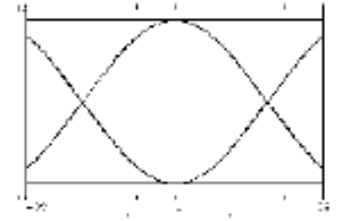
- Ideal for shorter connections including die-to-die interconnect inside a package.
- Balanced values on wires reduce SSO Noise and EMI.
- Tolerates common mode noise similar to differential signals.
- Values at slicers are binary.
  - Similar to NRZ signaling
  - ISI Ratio = 1
- Comparators are self-referencing.

# Key Advantage of CNRZ-5 over PAM-4: ISI Ratio

- Inter Symbol Interference Ratio (ISI Ratio):
  - Inherent property of any given code
  - A rough definition is that it is the code's ratio between the largest and smallest eyes at the decision point
- Energy from the larger eyes bleeds over and tends to close the smaller eyes
  - High ISI Ratio codes require more energy to be spent on ISI equalization
  - High ISI Ratio codes are more vulnerable to reflections



PAM-4's ISI  
Ratio = 3



CNRZ-5's ISI  
Ratio = 1

# Standardization of Chord Signaling

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# JEDEC

- CNRZ-5 is part of the JESD247 standard
- Specifies
  - Signal levels on the wires
  - Driver specification
  - Receiver specification
  - HSPICE modeling

## JEDEC STANDARD

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**Multi-wire Multi-level I/O Standard**

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**JESD247**

JUNE 2016

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



# OIF

- ENRZ, CNRZ-5's cousin code, is a part of the OIF's published CEI 4.0 specification
  - Full Interoperability Agreement at 56 Gb/s equivalent throughput
- The OIF announced the CEI-112 in MCM project to address this need
  - Kandou has been active in this project



**IA Title: Common Electrical I/O (CEI) -  
Electrical and Jitter Interoperability  
agreements for 6G+ bps, 11G+ bps,  
25G+ bps I/O and 56G+ bps**

**IA # OIF-CEI-04.0**

**December 29, 2017**

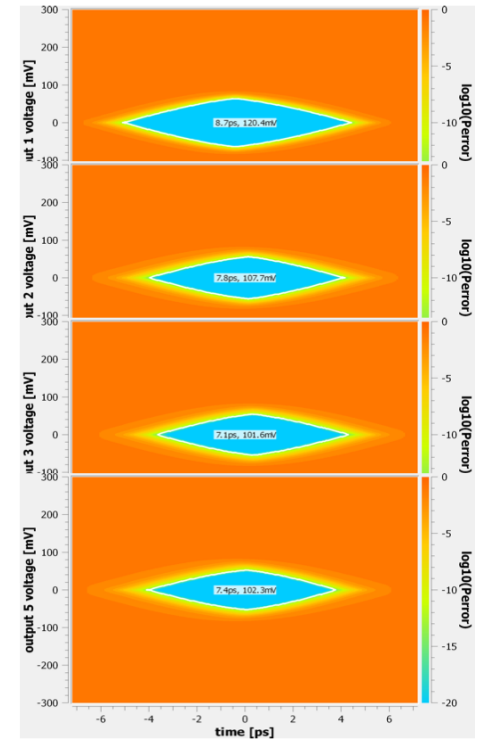
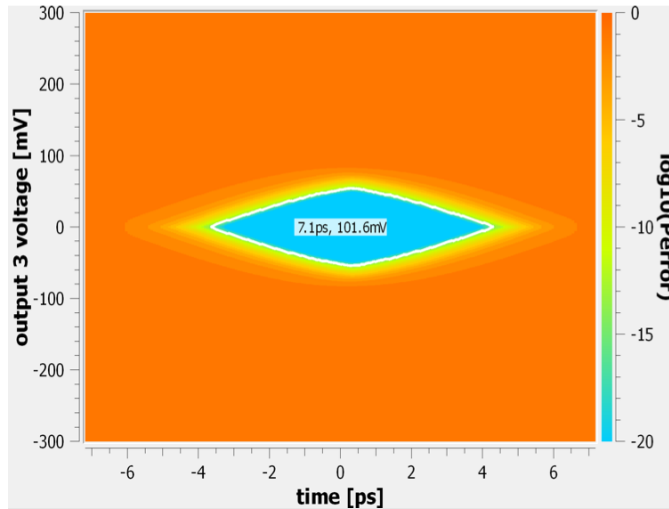
Implementation Agreement created and approved  
by the Optical Internetworking Forum  
[www.oiforum.com](http://www.oiforum.com)

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# CNRZ-5 Simulation at 69.6 GBaud

- Simulation over a 1 cm MCM link at 69.6 GBaud
  - Robust, even at high speed
  - Much larger eyes than equivalent PAM-4 solution

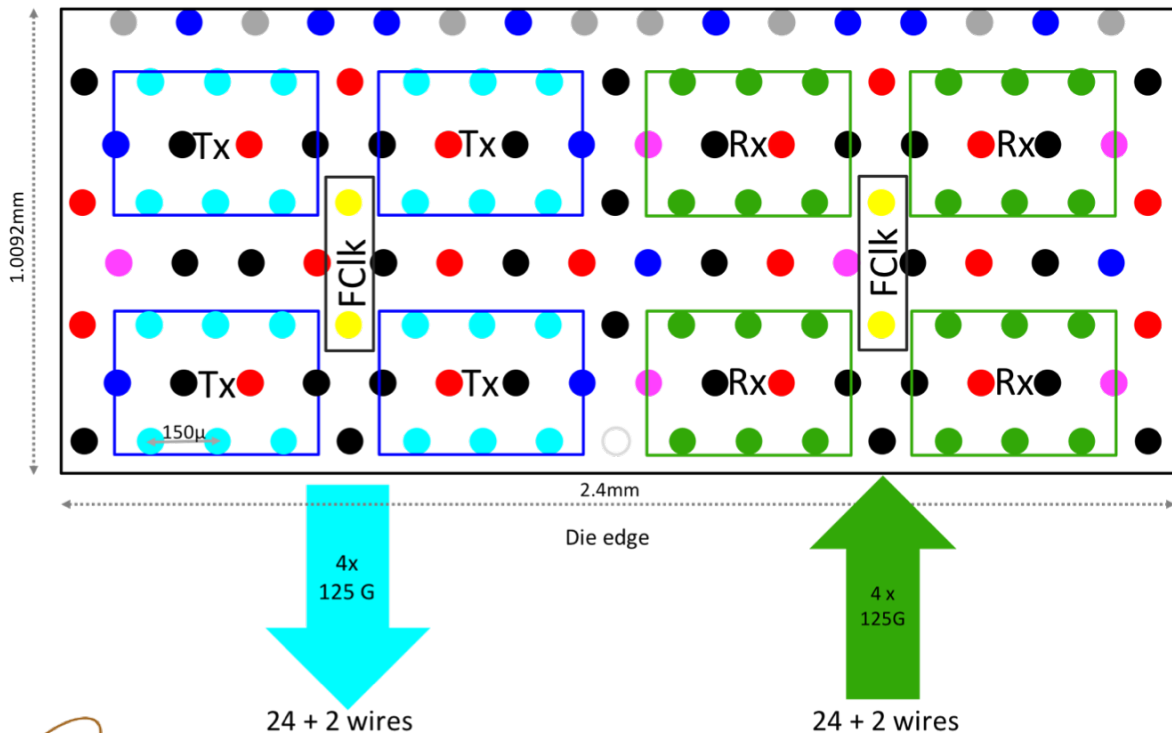
Smallest of  
the 5 eyes



# Example Femto SerDes for MCMs

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# The GW16-500 PHY



## Process:

- TSMC 16nm FFP-GL
- Metal stack for GW is 12 layer;  
12ML\_M1\_1Mx\_2Mxa\_2Mxy\_2My\_2Myy\_1Mz\_1Mr\_A P280
- Devices used: HVT, LVT and nominal VT (3 types)

## General:

- IP uses inductors (Tx side) and T-coil (Rx side)
- Tx output driver is voltage mode (SST type)
- Flip chip package with 150µm bump pitch

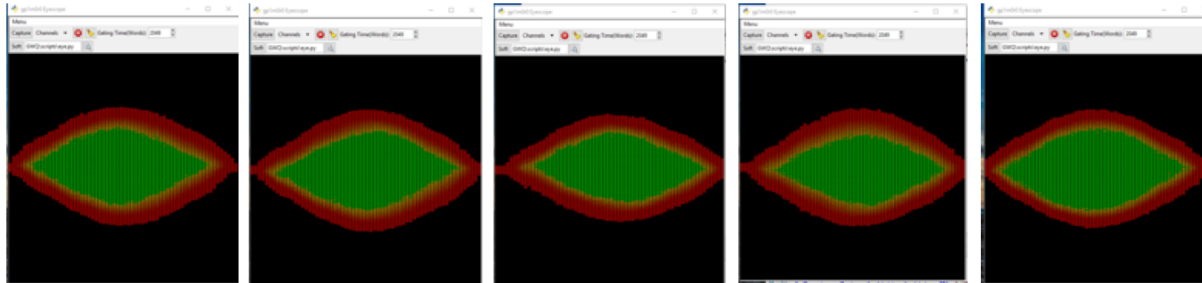
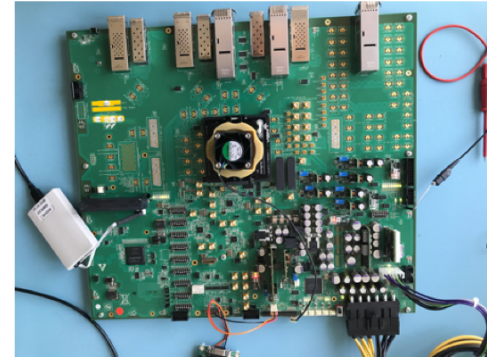


# GW16-500 PHY Metrics

Sample applications	Connecting to 56G outbound SerDes, subdivision of large ASIC
Process	TSMC 16nm FF+ GL
Max throughput	500 Gbps Tx, 500 Gbps Rx
Supported BER	1E-15 across all corners
Supported insertion loss	6dB @ 12.5 GHz w/60 ohm ref impedance
Supported skew	Up to 10% of UI in 6-wire chord
Power	0.82 pJ/b (nominal PVT) -- measured
Latency	< 4.5 nsec - fixed
ESD	250V CDM; 1000V HBM
Total area	2.4 mm <sup>2</sup> – bump limited
Beachfront BW	208 Gbps/mm per direction, 417 Gbps/mm total
Optional FEC	Can be used to lower BER to 1E-28, or save power.
FEC latency	1.25 ns collection latency

# GW16-500 Lab Results

- The MCM has 12 test chips inside connected by channels of various length/quality
  - Multiple bends
  - Lengths from 3mm to 30mm
- Eye diagrams below done via on-die eyescope on a single chord

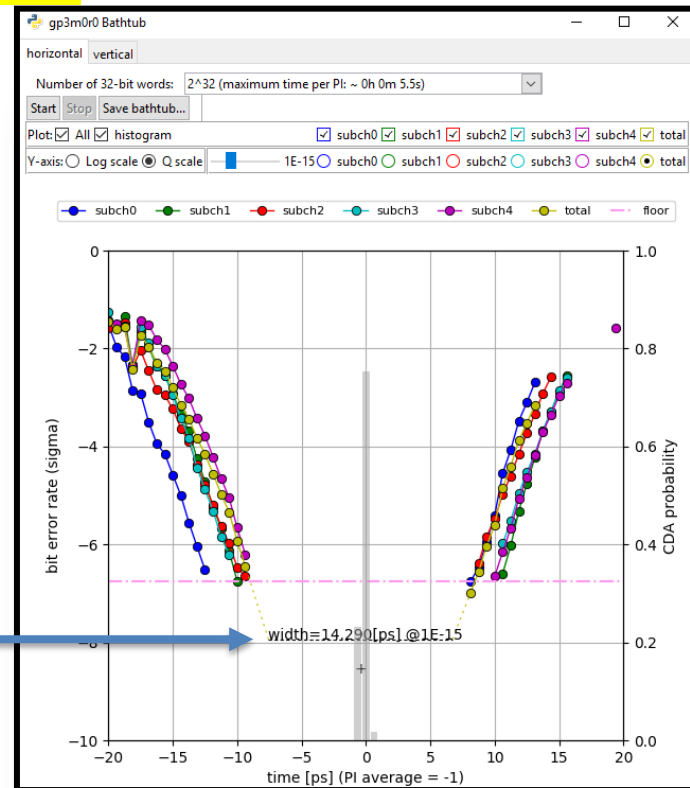
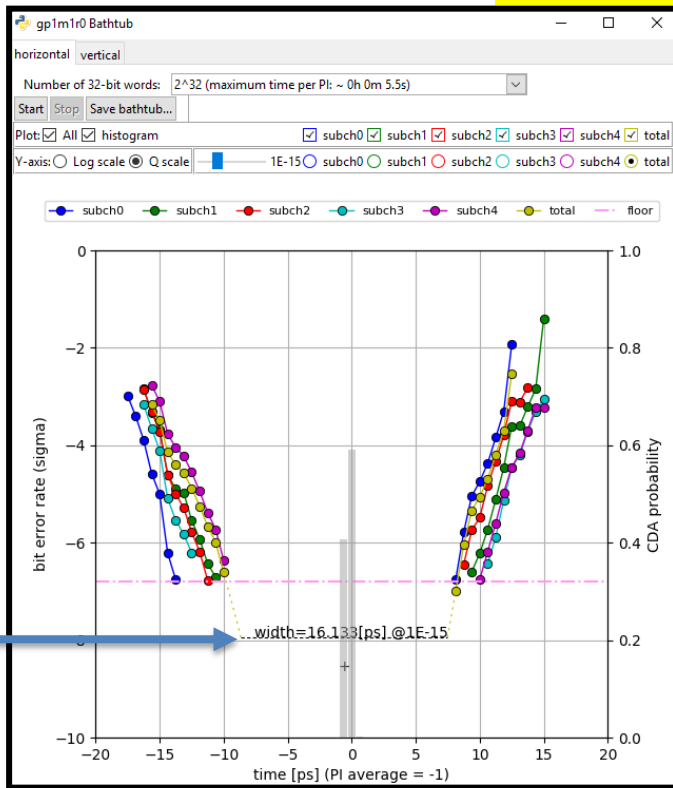


# Lab Results: Horizontal Bathtub Plots @ 25 Gbaud

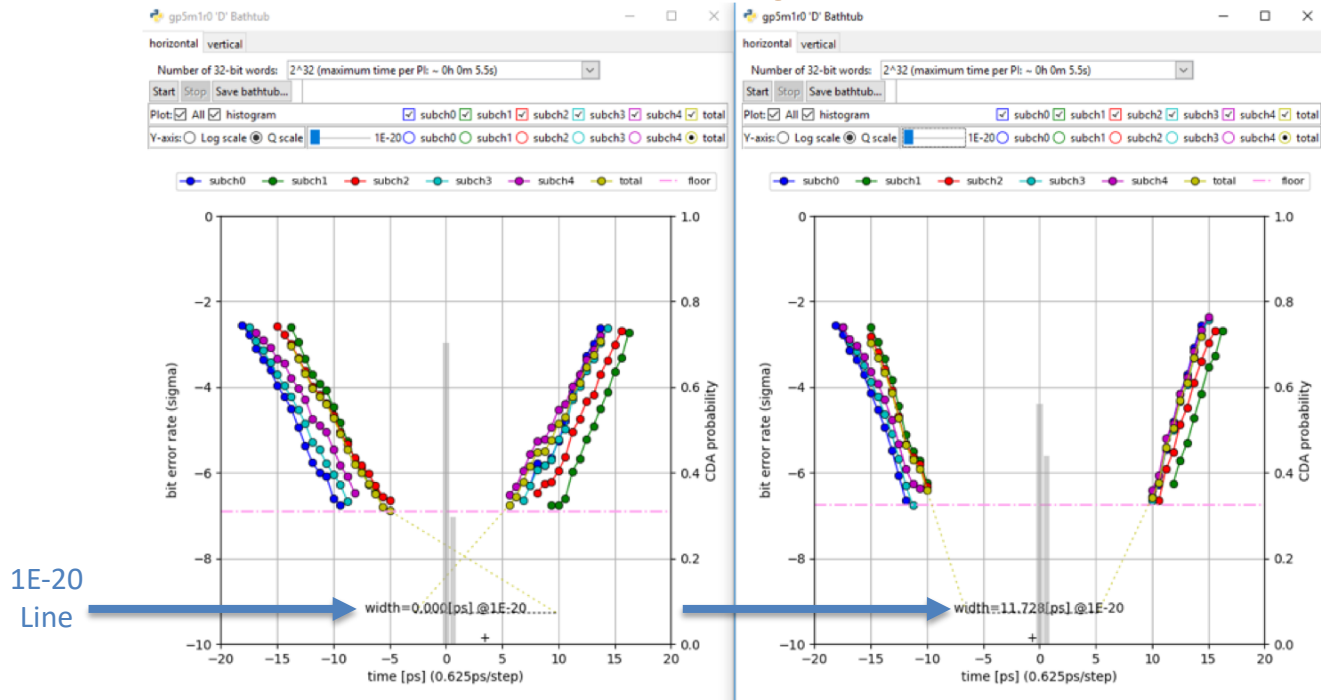
30 mm

Open eyes @ 1e-15

5 mm



# Lab results: Same with Low-latency FEC



- On the left is a measured (out of spec) channel that is closed (<25%) at 1E-15
- On the right FEC is turned on – the bathtub to support 1E-20 is open (>25%)

# IP Disclosure

- Kandou Bus, S.A. discloses that we own intellectual property related to Chord Signaling and the PHYs described in this contribution.
  - We are committed to adhering to the bylaws of all standards organizations to which we contribute and maintain membership including RAND licensing of our intellectual property.
  - We are committed to being good corporate citizens.

# Thank you!

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## QUESTIONS?