100Gbps/Lane Electrical Signaling

Loop-Timed Configurations

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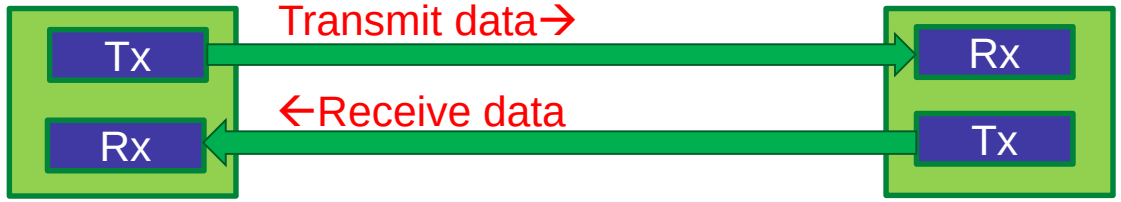
Dual Duplex Definition

Single Duplex (SD):



Dual Duplex (DD):

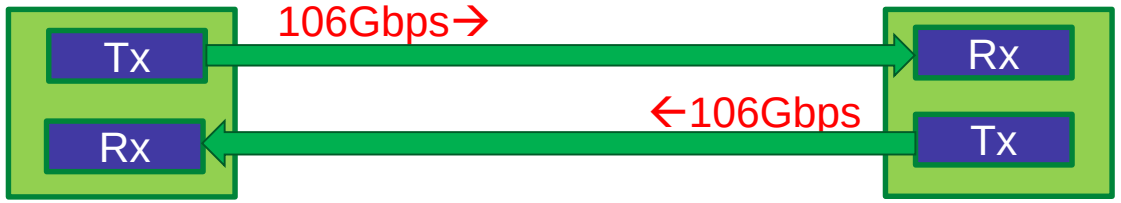
- Transmit and receive data on each pair
- In Dual Duplex data rate on each pair is half of the data rate of Single Duplex

→ Insertion Loss in Dual Duplex mode is much lower

SD – Single Duplex (Tx on one pair, Rx on one pair)
DD – Dual Duplex (Tx and Rx on both pairs)

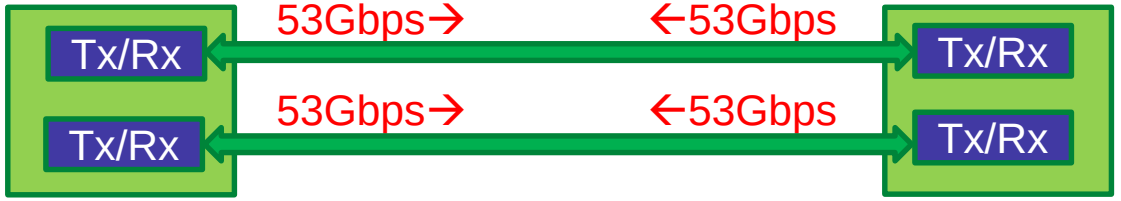
100G Dual Duplex Technology

Standard 100G Electrical:



Baud rate: 53Gbaud (f_N=26.5GHz)

Aquantia 100G Electrical:
Dual Duplex PAM4 Signaling



Baud rate: 26.5Gbaud (f_N=13.25GHz)

- Using the standard Tx and Rx channels to transmit and receive on each one.
  - Signal rate is half of standard rate, results in a much lower Insertion Loss
  - Echo cancelation technology is required to remove ~40dB echo power
  - Echo cancellation at Multi-Gbaud performs much better in a loop-timed link
    - Rx and Tx operate at the same exact frequency, thus keep a constant phase relationship

Dual-Duplex Loop-Timed: Passive DAC w/o Retimer

- Scenario 1: Both side have 100G Dual Duplex (DD) PHYs:
  - A simple low-speed auto-negotiation (AutoNeg) between PHYs sets the Master/Slave
    - Autoneg communication uses very wide pulses → No high-speed challenges like equalization/clock recovery
    - Autoneg operates in single-duplex, i.e. AutoNeg pulse only transmitted on one channel and received on another
  - Master PHY transmits data using its reference clock (Clk_M).
  - Slave PHY receiver recovers Clk_M from incoming data, while its transmitter is off
  - In the next phase, Slave PHY turns on its transmitter and uses recovered Clk_M to transmit data

Dual-Duplex Loop-Timed: Passive DAC w/o Retimer

- Scenario 2: One side 100G DD PHY and the other side 50G SD PHY
  - The DD PHY initiates AutoNeg phase, if it does not hear back AutoNeg pulses after a certain period:
    - DD PHY assumes link partner PHY is legacy Single-Duplex (SD), so switches to 50G SD mode

      → Turns off its Tx on the port connected to SD Tx and turns off its Rx on the other port
    - DD PHY ends AutoNeg, considers the legacy PHY as Master, and itself as Slave

      → DD PHY recovers Clk$_M$ from incoming data on one channel and uses that clock to transmits data back on the other channel

Dual-Duplex Loop-Timed: Passive w/ Retimer or Active DAC

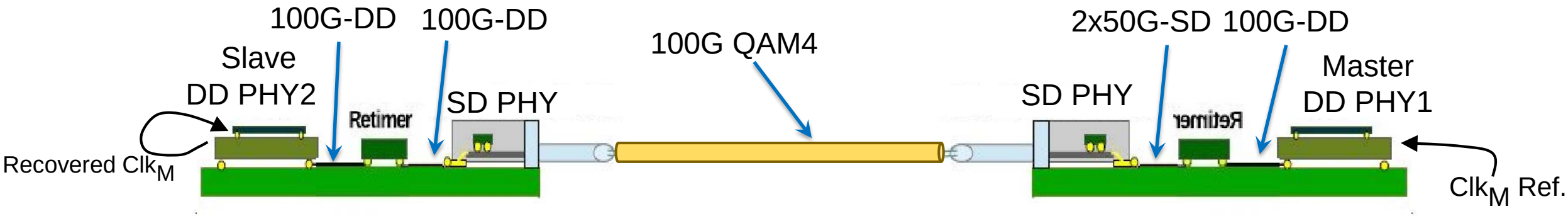
- Scenario 1: PHYs on both ends are 100G Dual Duplex:
  - Only ASIC (e.g. switch) PHYs at ether end of the link participate in Autoneg for Master/Slave selection
  - Retimer PHYs act as pass-through for AutoNeg communication, and are set as Slaves post AutoNeg
  - Once AutoNeg determines Master/Slave, Master PHY starts transmitting. Slave and Retimer PHYs keep their transmitters off in direction to Master (nothing transmitted to Master) and only transmit in Slave direction
  - The Retimer PHYs and end Slave recover Clk$_M$ from data sourced from Master

Dual-Duplex Loop-Timed: Passive w/ Retimer or Active DAC

- Scenario 2: One side 100G DD PHY and the other side 1x/2x 50G SD PHY
  - Retimer PHYs act as pass-through for AutoNeg communication, and are set as Slaves post AutoNeg
  - The ASIC DD PHY initiates AutoNeg phase, if it does not hear back AutoNeg pulses after a certain period:
    - DD PHYs assume link partner ASIC PHY is legacy SD PHY, considers it as Master PHY, self as Slave
    - If Retimer on DD ASIC is a 100G-DD→ 2x50G-SD PHY, operation continues to next phase, else

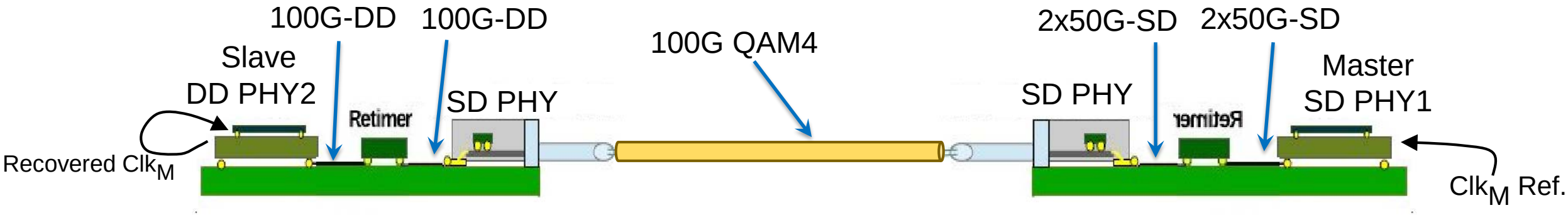
      → DD Retimer Turn off Tx on ports connected to a SD Tx and turn off Rx on the other port
    - Post AutoNeg, Retimers (DD or SD) pass data at same Clk$_M$ that their receivers recover from input data
    - DD ASIC recovers Clk$_M$ from its Rx channel and uses it to transmits data on the other channel

Dual-Duplex Loop-Timed: Electrical to Optical Module



- Scenario 1: ASIC PHYs on both ends are 100G Dual Duplex:
  - Only end PHYs (in ASIC or Switch ICs) participate in Autoneg for Master/Slave selection
  - Retimers and Optical transceivers act as pass-through for AutoNeg phase, and set as Slaves post AutoNeg
  - Once AutoNeg determines Master/Slave, Master PHY starts transmitting. Retimers & optical transceiver keep their transmitters off in direction to Master (nothing transmitted to Master) and only transmit in Slave direction
  - The Retimers and end Slave recover Clk$_M$ from data signal sourced from Master:
    - First Retimer to Master recovers Clk$_M$ and uses that to transmit recovered data to 2nd Retimer and so on
  - Slave PHY recovers Clk$_M$ from its Rx, turns on transmitter after certain time to send data back at Clk$_M$

Dual-Duplex Loop-Timed: Electrical to Optical Module



- Scenario 2: One side 100G DD PHY and the other side 1x/2x 50G SD PHY
  - Retimer PHYs act as pass-through for AutoNeg communication, and are set as Slaves post AutoNeg
  - The ASIC DD PHY initiates AutoNeg phase, if it does not hear back AutoNeg pulses after a certain period:
    - DD PHYs assume link partner ASIC PHY is legacy SD PHY, sets it as Master PHY, self as Slave
    - If Retimer on DD ASIC is a 100G-DD → 2x50G-SD PHY, operation continues to next phase, else

      → DD PHYs Turn off Tx on ports connected to a SD Tx and turn off Rx on the other port
    - Post AutoNeg, Retimers (DD or SD) pass data at same Clk$_M$ that their receivers recover from input data
    - DD PHY recovers Clk$_M$ from its received data and uses it to transmits data back to Master ASIC side

Summary

- A 100Gbps DD-PAM4 PHY needs to perform ~40dB of echo cancellation for proper operation over legacy 50Gbps SD-PAM4 channels
- A fixed phase relationship between the DD PHY transmitter and receiver sampling improves the quality of echo cancellations
- Therefore, preferably the 100Gbps DD link should be loop timed for improved performance
- Several 100Gbps link configurations were studied and how a proper while simple AutoNeg algorithm can provide loop-timed dual-duplex links across each configuration: Passive/Active DAC, E2O links, DD to SD, etc, but in summary, if:
  - The ASIC PHY on both ends are DD PHYs, AutoNeg process select which one to be Master and which Slave, and the whole links runs on Master Clock
  - The ASIC PHY on one side is legacy SD PHY, the DD PHY on the other end considers the other end as Master, and locks its clock to the legacy SD PHY

Thank you.