Using Chiplets to Lower Package Loss

IEEE 802.3 100 Gb/s Electrical Lane Study Group

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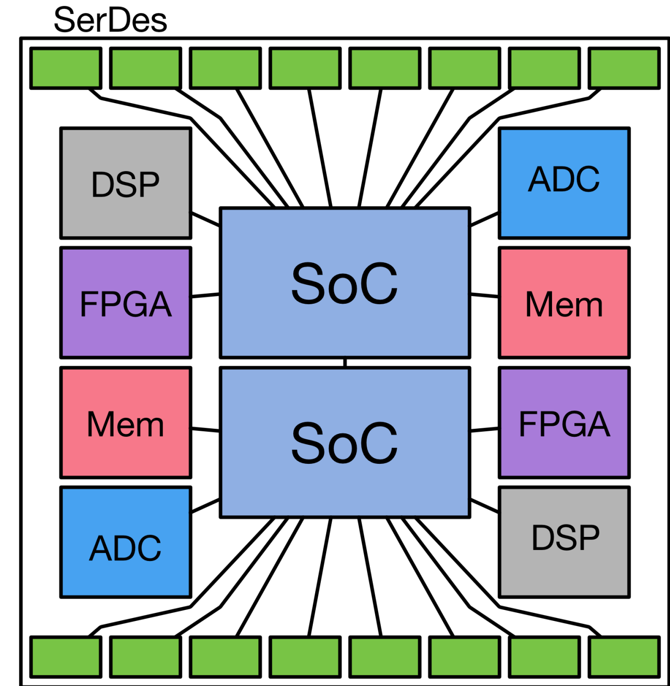
Chiplet Technology

- A trend in IC technology is to more away from monolithic chips toward the use of chiplets tied together on an MCM

- Chiplets allow:
  - Many dies to be combined in large packages
  - Yield and cost to be improved through smaller dies
  - Interoperating dies to use different semiconductor processes
  - Multi-vendor ecosystems to arise
  - **I/O subsystem dies containing SerDes to be placed around the perimeter, creating virtual smaller packages**

Big, 70mm packages are routine



Can easily use 20 or more dies plus passives

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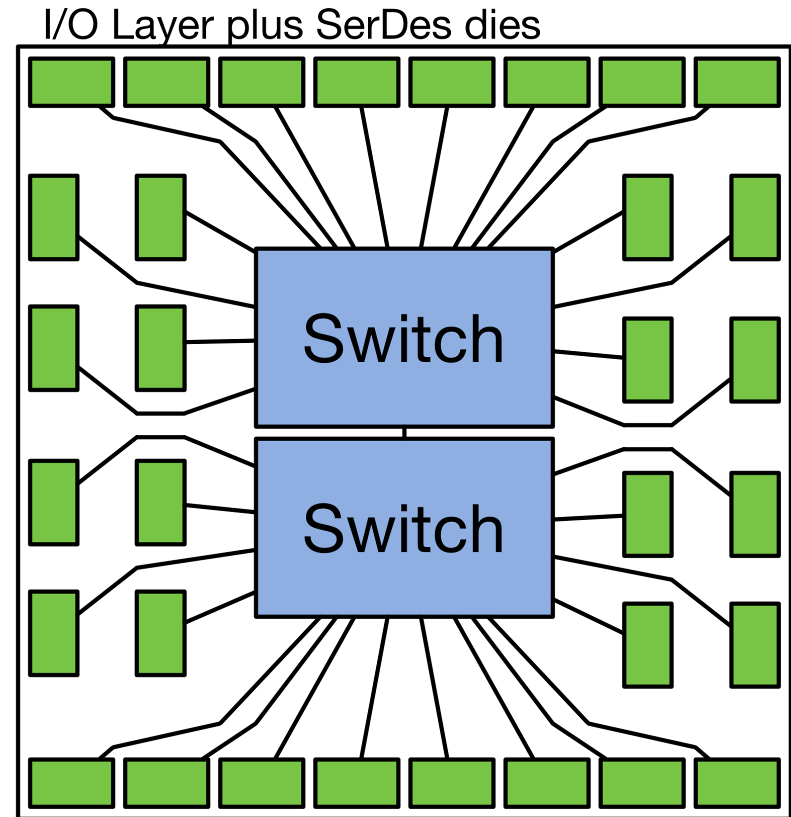
Chiplets in Switches

- The Ethernet I/O Subsystem including the SerDes can be put on a chiplet
  - Chiplet can have the PCS, FEC and long-reach SerDes and use a fat-pipe packet protocol between devices with a little speed-up factor
    - The chiplets could alternatively use a lower or higher level protocol between devices
  - 400 Gb/s, 800 Gb/s or 1600 Gb/s of I/O are three possible chiplet sizes
  - Switch-to-chiplet link can use a Femto SerDes
    - A chord signaling Femto SerDes is one example
    - Femto SerDes can reach to the corners of a 70 mm package



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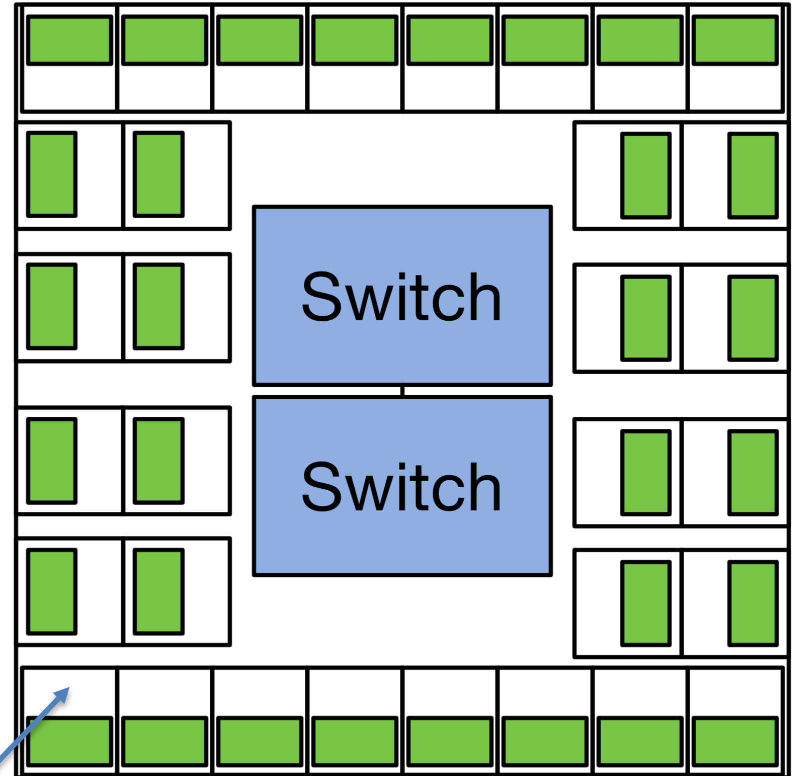
Virtual Packages

- Putting the I/O subsystem on chiplets allows virtual packages to be created
  - Chiplet only fans out to the package balls in its immediate area
  - Looks like a small package to the system
  - The package loss budget can be reduced
  - The front panel optics interface can be modeled as being between two 12mm packages
  - **A 30mm package model is not needed**



Virtual package
Around each I/O chiplet

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Package Alternatives

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Conventional Packaging

	Conventional
Die placement	Inflexible
Signal integrity of external interfaces	Worse - traces must fan out to reach the perimeter package balls
Assembly Yield	Good
Number of Dies	1
Supply chain	Good

- Ideas for extending
  - Use better materials
  - Co-design the ASIC and the package
  - Tune equalizers to the fan-out trace
  - Don’t try to fit so many SerDes in one package
- But there is only so much that can be done

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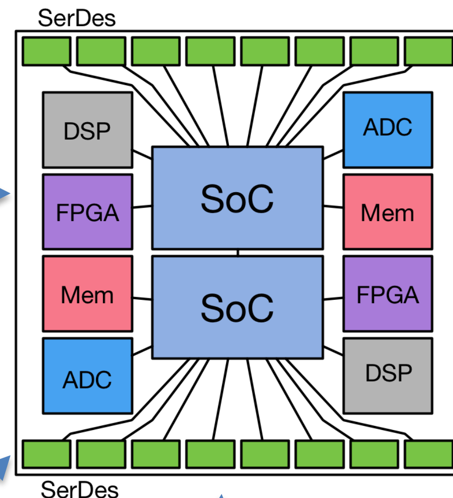
MCM with Femto SerDes

	MCM using Femto SerDes
Die placement	Flexible because of the 2.5cm reach
Signal integrity of external interfaces	Better - external interface can be located close to the package balls
Assembly Yield	Well known technology with good yield
Number of Dies	Number of dies limited only by package size
Supply chain	Multiple OSATs can handle

Big, 70mm packages are routine



Can put SerDes right over the package balls

Can easily use 20 or more dies plus passives

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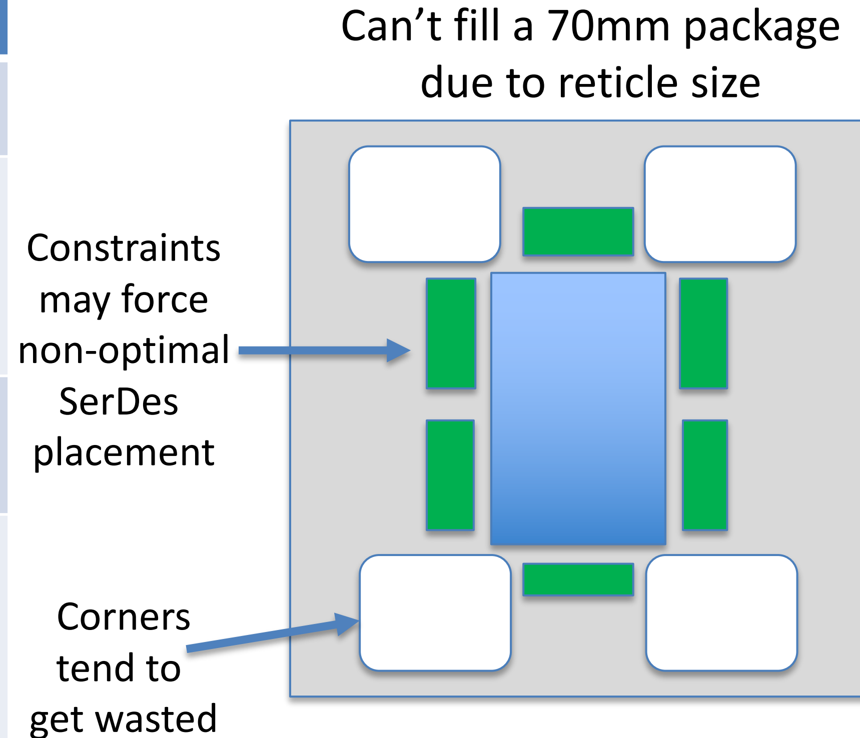
Silicon Interposers

	2.5D interposers
Die placement	Non-flexible & strict design rules
Signal integrity of external interfaces	Medium - restrictions on die location may cause long traces of external high speed interfaces
Assembly Yield	Specialized implementation with yield issues
Number of Dies	Restrictions on the number of dies "Stitched" interposers are more exotic, have connection limits, and have stricter design rules
Supply chain	Specialized suppliers



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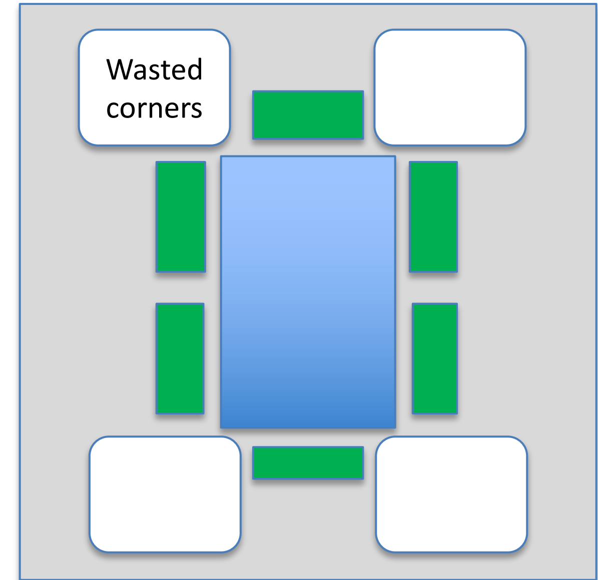
Fan Out Layers

	FO-WLP, FO-PLP
Die placement	Even stricter design rules
Signal integrity of external interfaces	Medium - die location may cause long traces of external high speed interfaces, impacting link performance
Assembly Yield	Relatively new technology especially for large devices and multi dies (>2)
Number of Dies	Restrictions on the number of dies and on the total area
Supply chain	Limited number of suppliers

Similarly, can't fill a 70mm package due to reticle size



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Chord Signaling Femto SerDes

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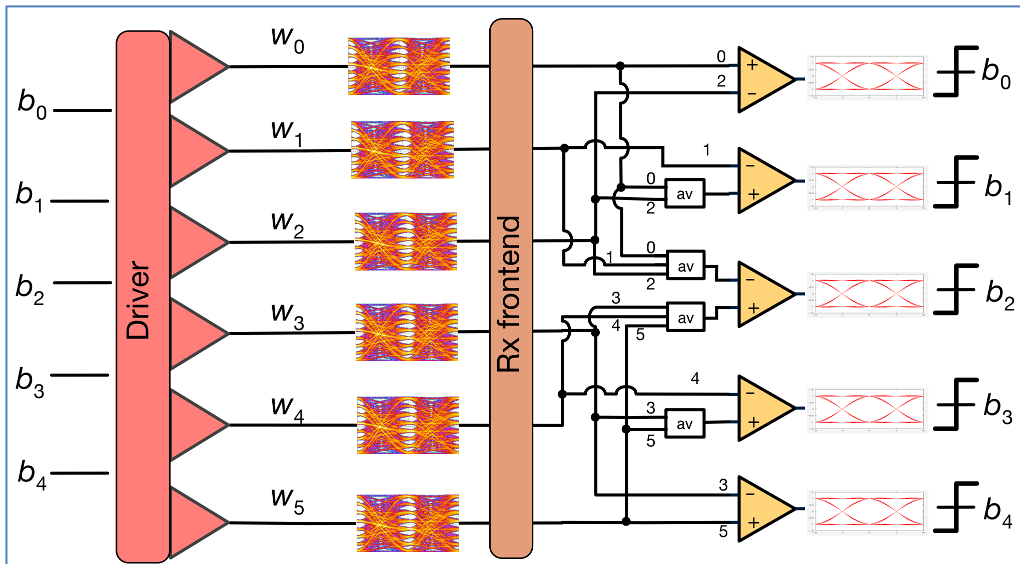
CNRZ-5



Advantages:

- Ideal for shorter connections including die-to-die interconnect inside a package.
- Balanced values on wires reduce SSO Noise and EMI.
- Tolerates common mode noise similar to differential signals.
- Values at slicers are binary.
  - Similar to NRZ signaling
  - ISI Ratio = 1
- Comparators are self-referencing.

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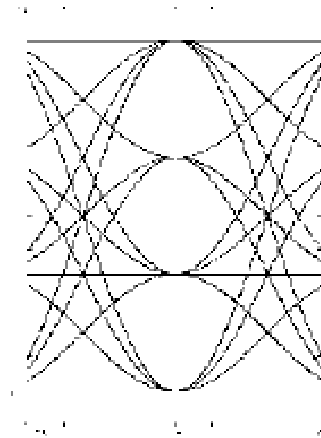
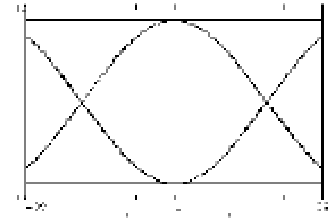
Key Advantage of CNRZ-5 over PAM-4: ISI Ratio

- Inter Symbol Interference Ratio (ISI Ratio):
  - Inherent property of any given code
  - A rough definition is that it is the code's ratio between the largest and smallest eyes at the decision point
- Energy from the larger eyes bleeds over and tends to close the smaller eyes
  - High ISI Ratio codes require more energy to be spent on ISI equalization
  - High ISI Ratio codes are more vulnerable to reflections



PAM-4's ISI Ratio = 3



CNRZ-5's ISI Ratio = 1

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Standardization of Chord Signaling

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JEDEC

- CNRZ-5 is part of the JESD247 standard
- Specifies
  - Signal levels on the wires
  - Driver specification
  - Receiver specification
  - HSPICE modeling

JEDEC STANDARD

Multi-wire Multi-level I/O Standard

JESD247

JUNE 2016

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

OIF

- ENRZ, CNRZ-5's cousin code, is a part of the OIF's published CEI 4.0 specification
  - Full Interoperability Agreement at 56 Gb/s equivalent throughput

- The OIF announced the CEI-112 in MCM project to address this need
  - Kandou has been active in this project

Implementation Agreement OIF-CEI-04.0 Common Electrical I/O (CEI)

IA Title: Common Electrical I/O (CEI) - Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps

IA # OIF-CEI-04.0

December 29, 2017

Implementation Agreement created and approved

by the Optical Internetworking Forum

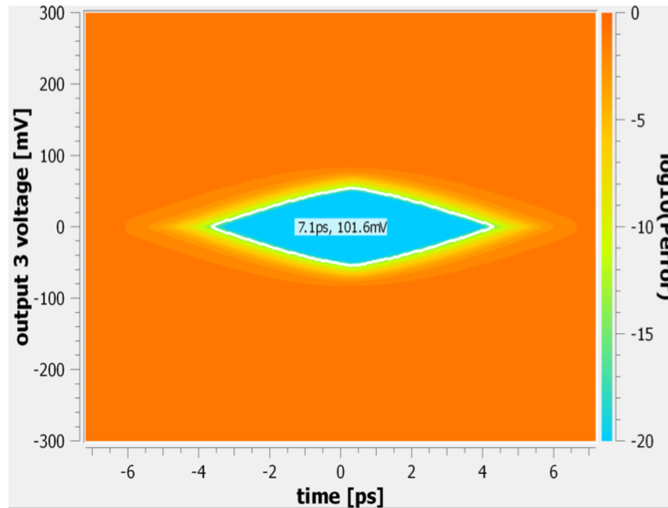
www.oiforum.com

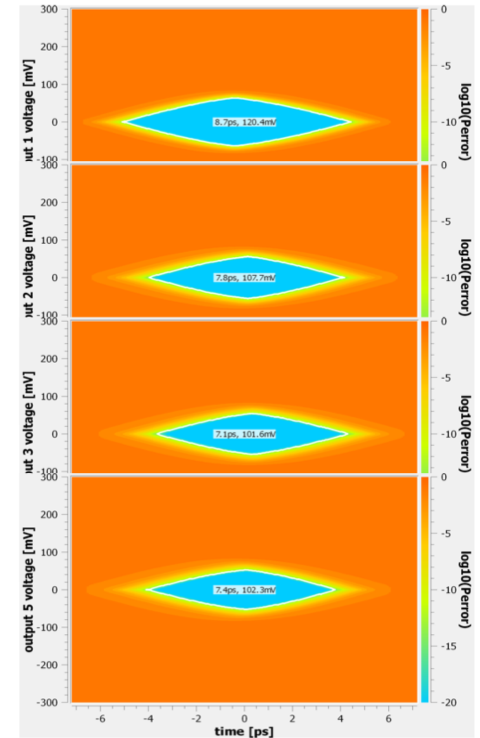
Optical Internetworking Forum - Clause 0 : Document Structure and Contents 1

CNRZ-5 Simulation at 69.6 GBaud

- Simulation over a 1 cm MCM link at 69.6 GBaud
  - Robust, even at high speed
  - Much larger eyes than equivalent PAM-4 solution

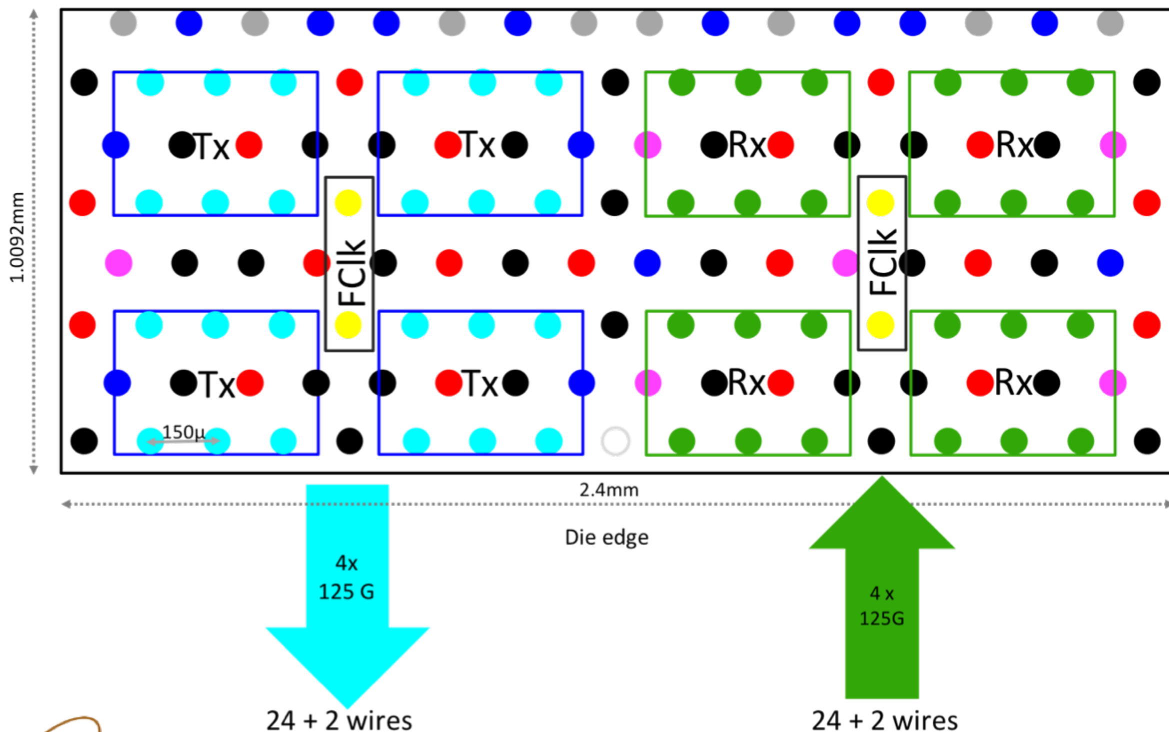
Smallest of the 5 eyes





Example Femto SerDes for MCMs

The GW16-500 PHY



Process:

- TSMC 16nm FFP-GL
- Metal stack for GW is 12 layer; 12ML_M1_1Mx_2Mxa_2Mxy_2My_2Myy_1Mz_1Mr_AP280
- Devices used: HVT, LVT and nominal VT (3 types)

General:

- IP uses inductors (Tx side) and T-coil (Rx side)
- Tx output driver is voltage mode (SST type)
- Flip chip package with 150µm bump pitch

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GW16-500 PHY Metrics

Sample applications	**Connecting to 56G outbound SerDes, subdivision of large ASIC**
Process	TSMC 16nm FF+ GL
Max throughput	500 Gbps Tx, 500 Gbps Rx
Supported BER	1E-15 across all corners
Supported insertion loss	6dB @ 12.5 GHz w/60 ohm ref impedance
Supported skew	Up to 10% of UI in 6-wire chord
Power	0.82 pJ/b (nominal PVT) -- measured
Latency	< 4.5 nsec - fixed
ESD	250V CDM; 1000V HBM
Total area	2.4 mm^2 – bump limited
Beachfront BW	208 Gbps/mm per direction, 417 Gbps/mm total
Optional FEC	Can be used to lower BER to 1E-28, or save power.
FEC latency	1.25 ns collection latency

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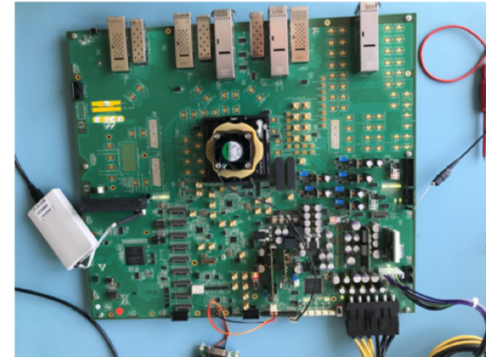
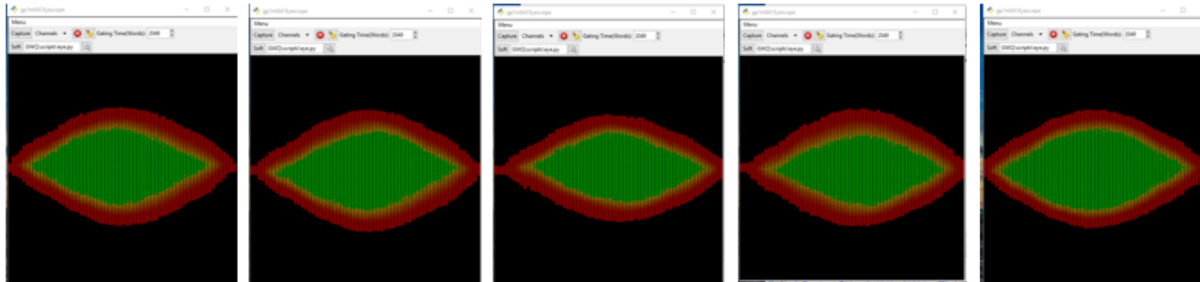
GW16-500 Lab Results

- The MCM has 12 test chips inside connected by channels of various length/quality
  - Multiple bends
  - Lengths from 3mm to 30mm
- Eye diagrams below done via on-die eyescope on a single chord





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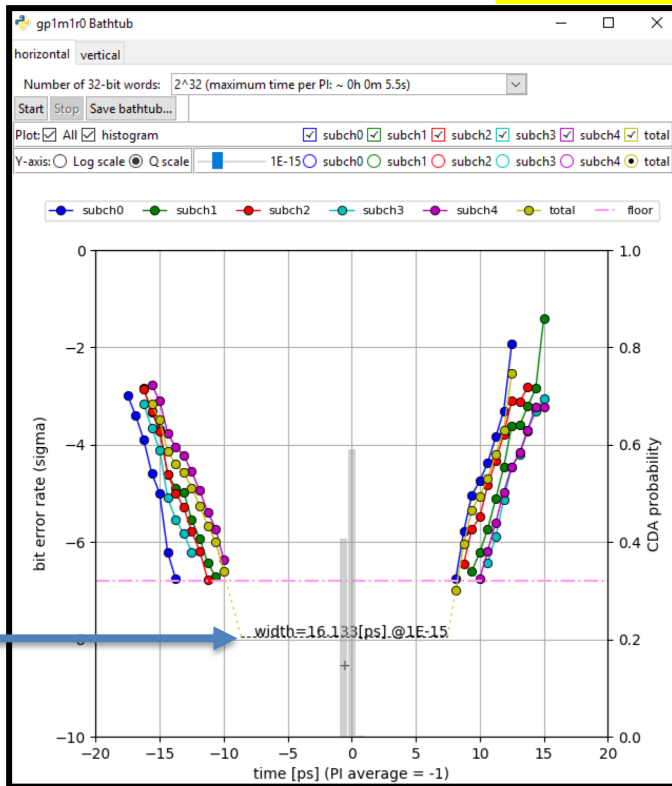
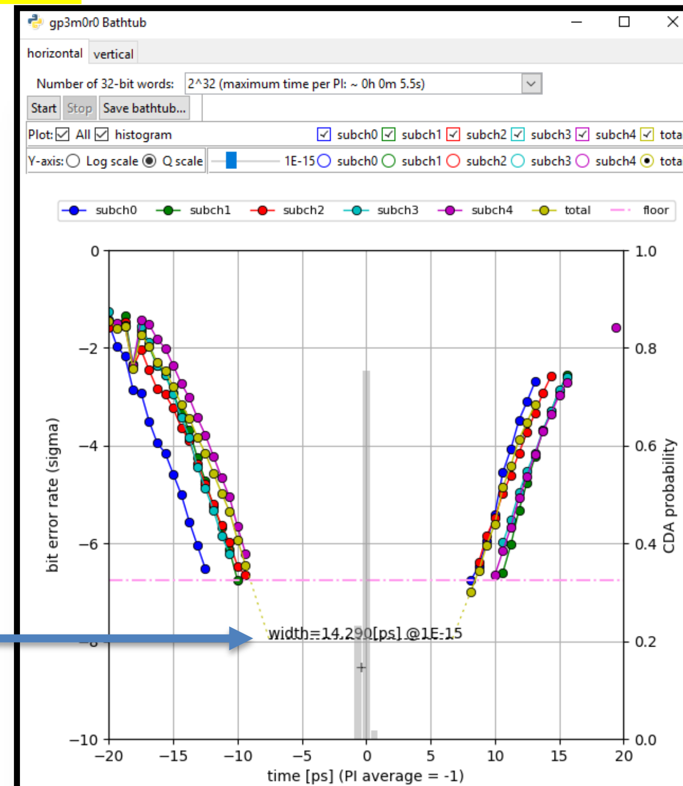
Lab Results: Horizontal Bathtub Plots @ 25 Gbaud

30 mm

Open eyes @ 1e-15

5 mm





1E-15
Line

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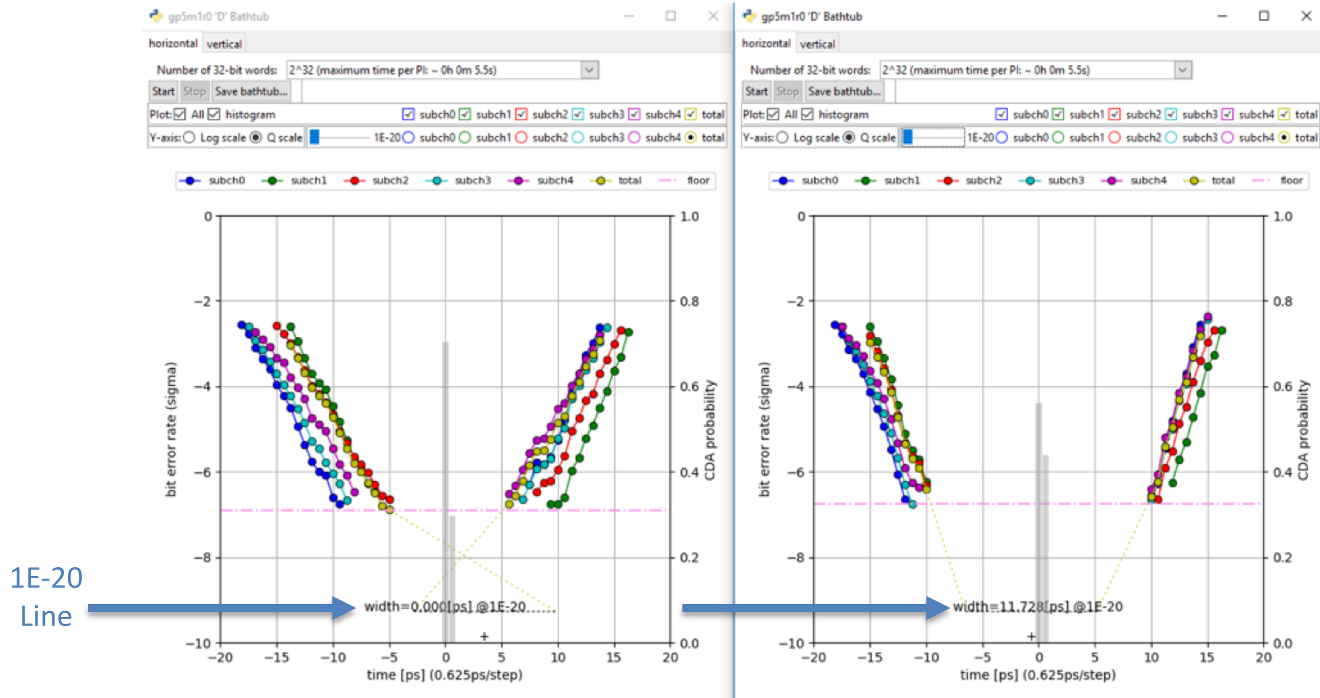
Lab results: Same with Low-latency FEC



- On the left is a measured (out of spec) channel that is closed (<25%) at 1E-15
- On the right FEC is turned on – the bathtub to support 1E-20 is open (>25%)

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IP Disclosure

- Kandou Bus, S.A. discloses that we own intellectual property related to Chord Signaling and the PHYs described in this contribution.
  - We are committed to adhering to the bylaws of all standards organizations to which we contribute and maintain membership including RAND licensing of our intellectual property.
  - We are committed to being good corporate citizens.

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Thank you!

QUESTIONS?

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