100GEL C2M Channel Estimate & Impact on the TBD in the Objectives

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Scope

- Study front port channel loss requirement for next generation 100GEL optical and DAC links
- Check the overall channel characteristics at 26.56GHz including QSFP SMT I/O connector
- Different host PCB materials were used in the analysis

100GEL C2M Channel Requirements

- Target ball to ball IL <12dB @ 26.56GHz :
  - To avoid using heavy receiver inside the optical modules → lower module power consumption
  - Make 100GEL C2M link budget work with 100GEL CR → twinax Cu cables support upto 2 m (ball to ball 30dB @26.56GHz, bump to bump 36dB @26.56GHz)
- Overall IL target should allow reasonable trace length with minimum 5” to reduce # of retimers at front ports
- Include present & next generation packaging and PCB technologies

100GEL C2M Channel - Host PCB Trace

- With DS7409-DV material, trace IL at HT is 1.64dB/in at 28GHz
  - 4.9dB for 3” trace
  - 6.6dB for 4” trace ← To meet 7dB host budget (inc. via loss) → trace length must be < 4”
  - 8.2dB for 5” trace

- With Meg-7NE material, trace IL at HT is 1.24dB/in at 28GHz
  - 3.7dB for 3” trace
  - 4.9dB for 4” trace
  - 6.2dB for 5” trace ← To meet same host budget → trace length must be < 5”

Note: via loss is not included above → each via loss ~0.5dB at 28GHz

100GEL C2M Channel - ASIC Package

- Today 56G ASIC 62.5mm package, longest trace length is ~30mm, with GZ buildup material, worst case IL at HT is 7.2dB, ~0.24dB/mm @ 28GHz
- For next gen 100GEL big size ASIC, likely requires 67.5mm package, longest trace length ~33mm, max. IL is 7.9dB with GZ material, or ~5.0dB with GL103 or VLL material
- To control the package loss within 3dB @26.56GHz, one option is to use chip-lets with USR interface (refer to USR Alliance’s presentation)

100GEL C2M & CR Link Budget Proposal

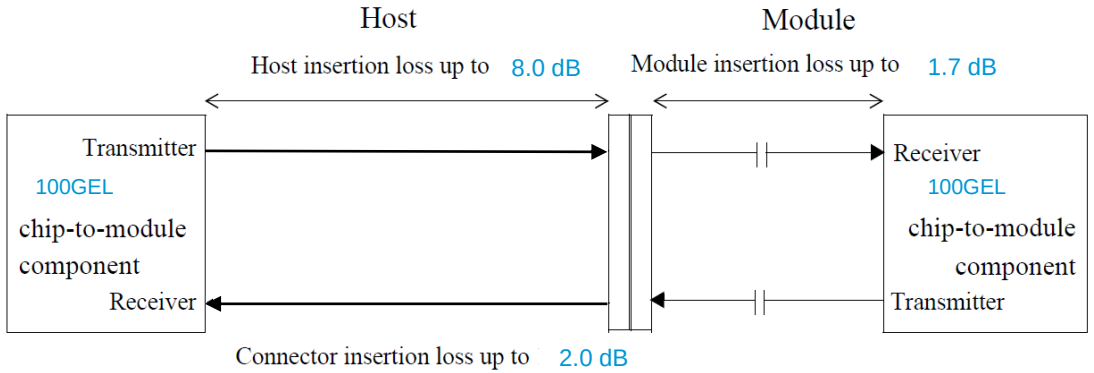


Figure 1: 100GEL C2M insertion loss budget at 26.56 GHz

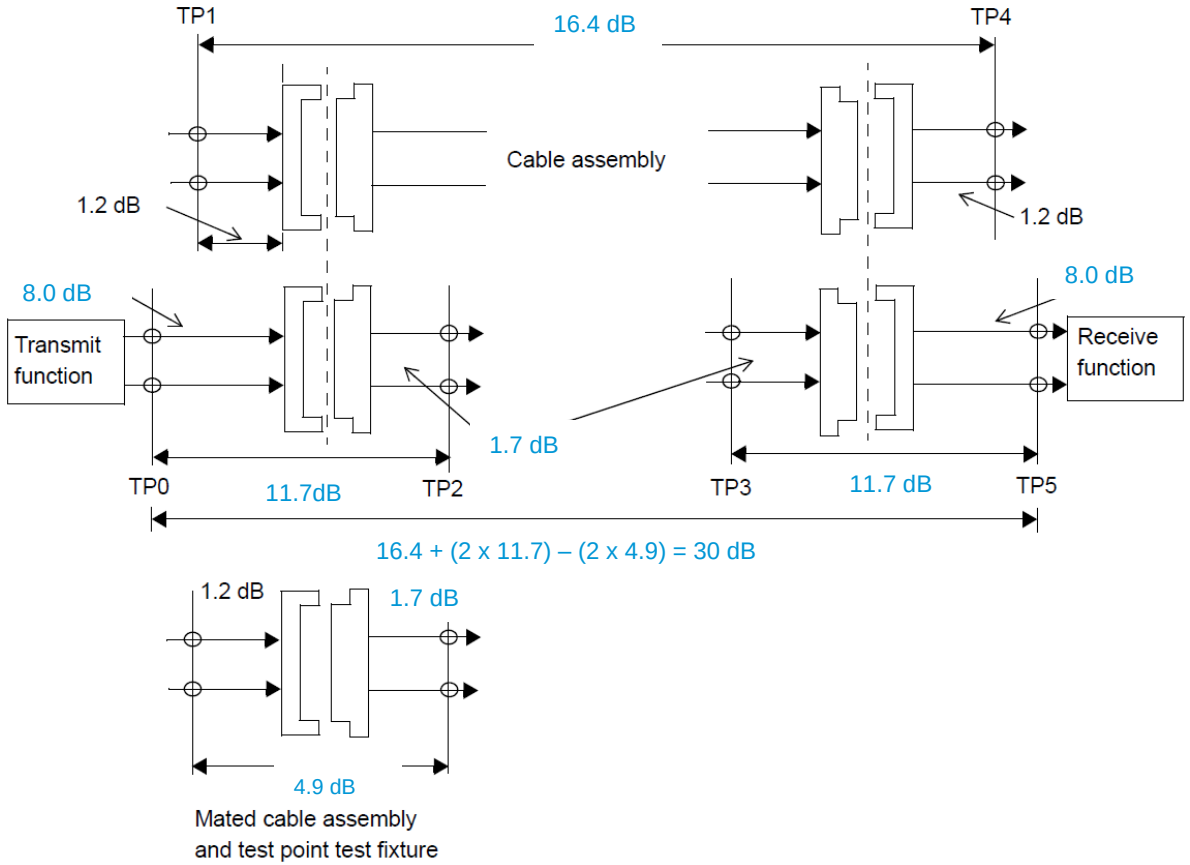
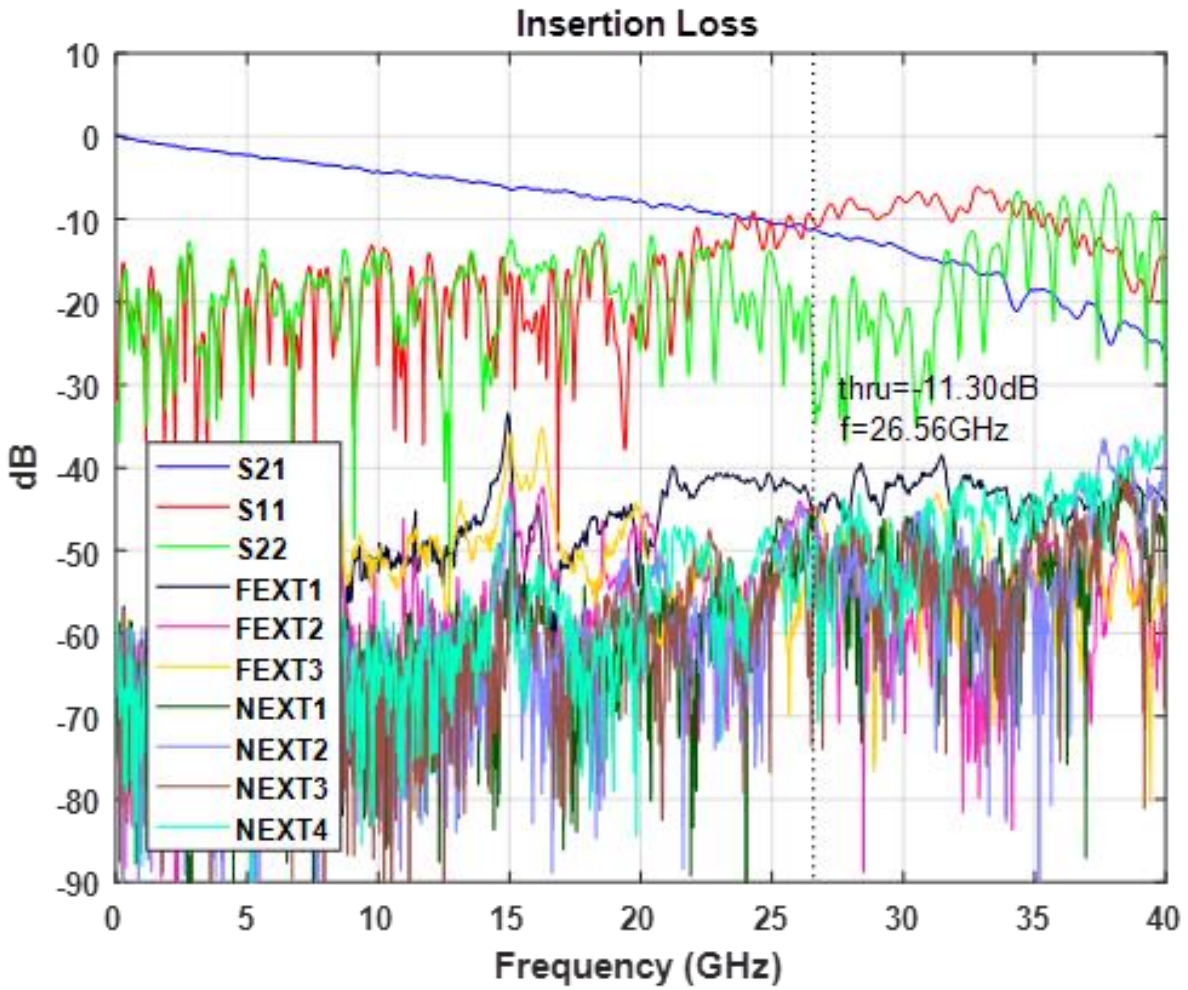


Figure 2: 100GEL CR 30dB insertion loss budget at 26.56 GHz

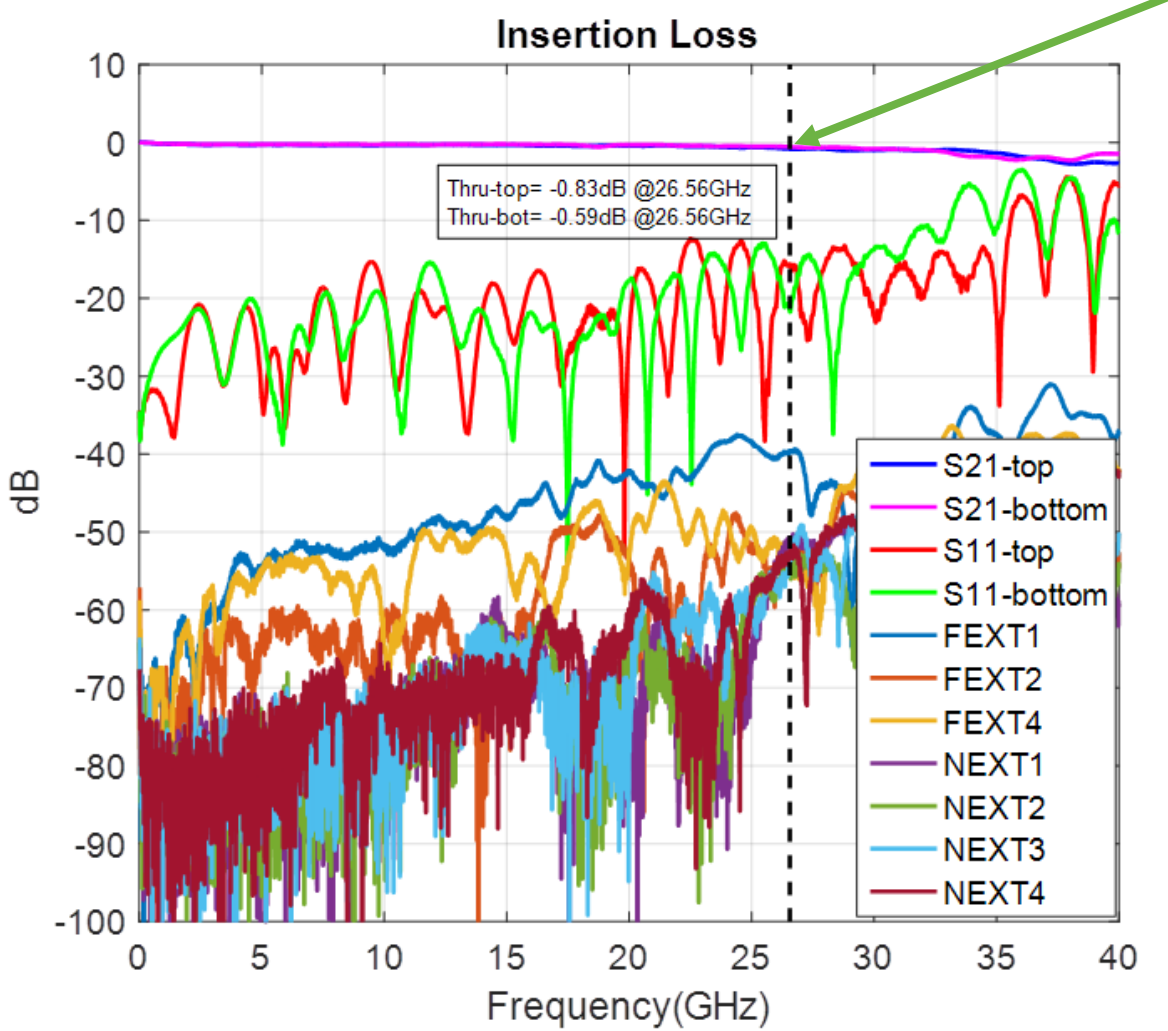
100GEL C2M Channel Characteristics



Remark: Package footprint, Host PCB trace and QSFP Test Fixture included

QSFP56 Connector Only Measurement Data

< 1 dB @26GHz



Summary & Proposal

- Based on Cisco's analysis on current and next generation Serdes, Package & PCB technologies, we propose the TBD numbers in the objectives as follows:
  - Define a single-lane 100 Gb/s PHY for operation over electrical backplanes supporting an insertion loss ≤ **30** dB at **26.56** GHz.
  - Define a single-lane 100 Gb/s PHY for operation over twin-axial copper cables with lengths up to at least **2** m.

Backup Slides

400GAUI-8 C2M IL Budget

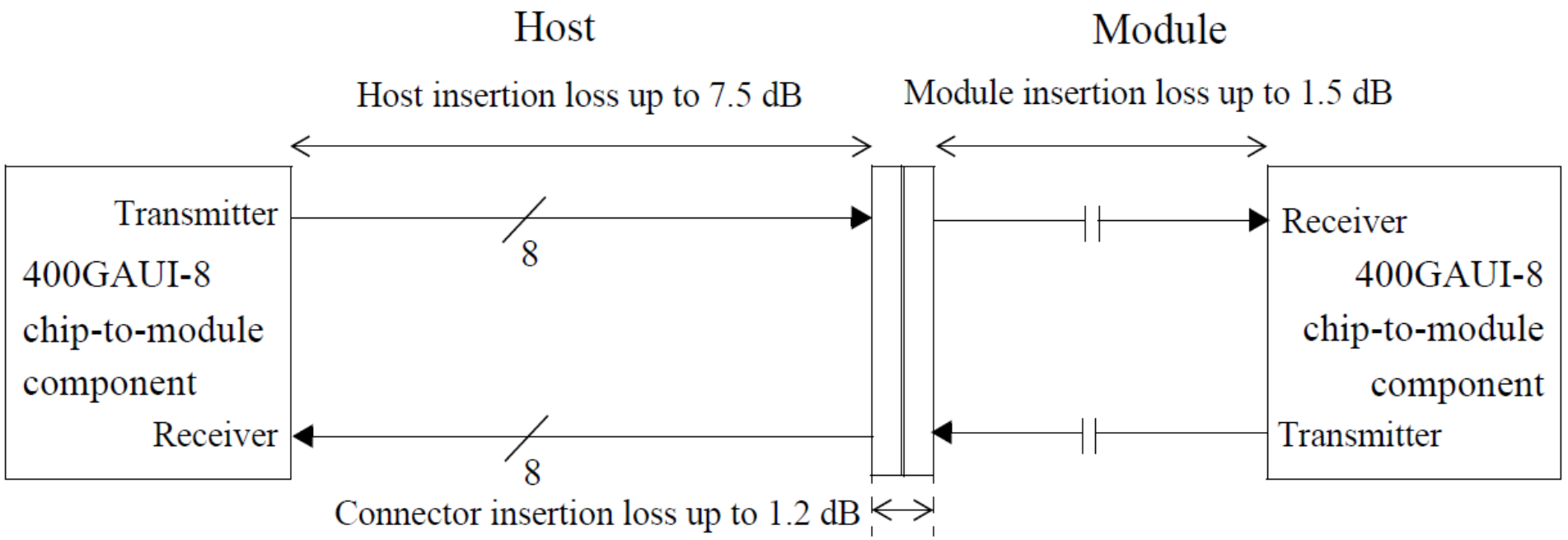
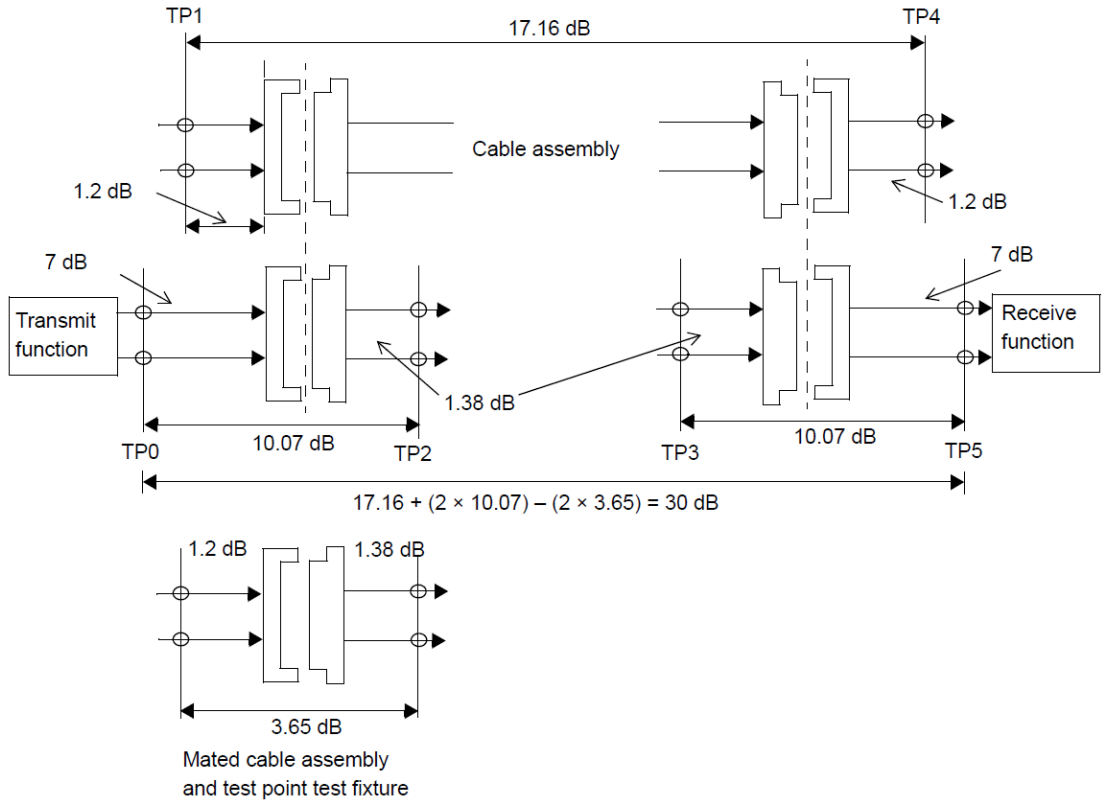


Figure 120E–3—400GAUI-8 chip-to-module insertion loss budget at 13.28 GHz

Total channel link budget (ball to ball) = 10.2dB at 13.28GHz

Source: IEEE802.3bs

200GBASE-CR4 Channel IL Budget



NOTE—The connector insertion loss is 1.07 dB for the mated test fixture. The host connector is allocated 0.62 dB of additional margin.

Figure 136A–1—30 dB channel insertion loss budget at 13.28 GHz

Source: IEEE802.3cd

Thank You !