FEC Schemes for 100G Electrical Link

Phil Sun, Credo Semiconductor

February, 2018

Introduction

- KP4 FEC was adopted for 50GBASE-R PHYs.
- It is more costly to achieve same BER for 100Gbps single-lane electrical link [sun_100GEL_01b_0118]. Stronger FEC may be desired for some cases.
- On the other side, FEC cost and latency budget is tight. FEC backward compatibility shall be considered. [stone_100GEL_01_0118]
- Considering these constraints and current simulation results, this contribution discusses KP4 and 2-way interleaved KP4 FEC schemes for 100GEL project.

CredŐ

What we have now?

- KP4 FEC, RS(544, 514, m=10, t=15), was adopted by 802.3cd for 50GBASE-KR/CR, 100GBASE-KR2/CR2, 200GBASE-KR4/CR4, and etc.
- 2-way interleaved KP4 FEC was adopted by 802.3bs for 400G and 200G optical links.
- 1+D precoding is defined and can be optionally turned on for 50G PAM4 signal based C2C, backplane, or DAC cable links. For example:
  - 50GBASE-CR, 50GBASE-KR, 100GBASE-CR2, 100GBASE-KR2
  - C2C: 50GAUI-1, 100GAUI-2
- Interleaving effectively alleviates burst error penalty.
- 1+D precoding is effective if burst error is caused by 1-tap DFE, less effective for some other burst errors, e.g. those caused by low frequency noise. It doubles BER if errors are random.
- 1+D precoding and interleaving can be turned on at the same time.

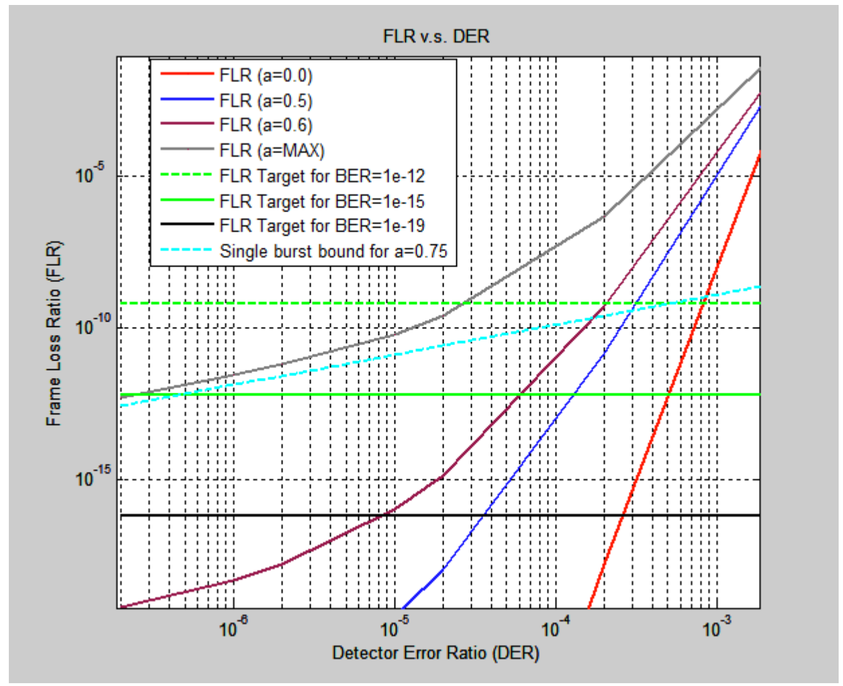
CredŐ

KP4 FEC Performance

- For PAM4 modulation with KP4 FEC, worst DFE error propagation rate (‘a’) is 0.75. In this case, DER needs to be 2.9E-5 to achieve frame loss ratio equivalent to BER 1E-12 (FLR=6.2E-10). Raw BER requirement is 5.8E-5.
- If DFE error propagation rate can be limited to 0.6, DER and BER requirement can be relaxed to 2.1E-4 and 3.2E-4.
- Raw BER requirement needs to be lower (shared) if there are multiple links.
- If 1E-15 post FEC BER is required for some applications, DER needs to be lower.

BER Target	FLR	a=0.75	a=0.6	a=0
1E-12	6.2E-10	2.9E-5	2.1E-4	7.6E-4
1E-15	6.2E-13	2.5E-7	6.0E-5	5.0E-4

DER Requirement For KP4 FEC



KP4 FEC Performance for PAM4

2-way Interleaved KP4 FEC Performance

- For interleaved KP4 FEC, DER requirement is relaxed by more than 1 order for a=0.75.
- Precoding may help to achieve better post-FEC BER.

BER Target	FLR	a=0.75
1E-12	6.2E-10	1.1E-4
1E-15	6.2E-13	3.8E-5

DER Requirement For 2-Way Interleaved KP4

Latency, Cost, and Backward Compatibility

- 2-way interleaved FEC consists of two 50G KP4 FEC.
- KP4 FEC latency for 100G is “typically” around 110ns. 2-way interleaving adds extra 50ns or higher.
- Two schemes have similar hardware cost, considering breakout may be required.
- 100G KP4 (no interleaving) is required to talk to existing FEC for 100GBase-R. Hardware of 2-way interleaved FEC can be reused.

CredŐ

Summary

- KP4 and 2-way interleaved KP4 FEC schemes are discussed for 100G electrical link.
- Compared to precoding, 2-way interleaved scheme (plus precoding) can effectively relax DER requirement.
- Backward compatibility cases need to be further studied.

Thanks!