

# Chiplet package study

---

IEEE 802.3 100 Gb/s Electrical Lane Study Group (.ck) ad hoc call

May 9, 2018

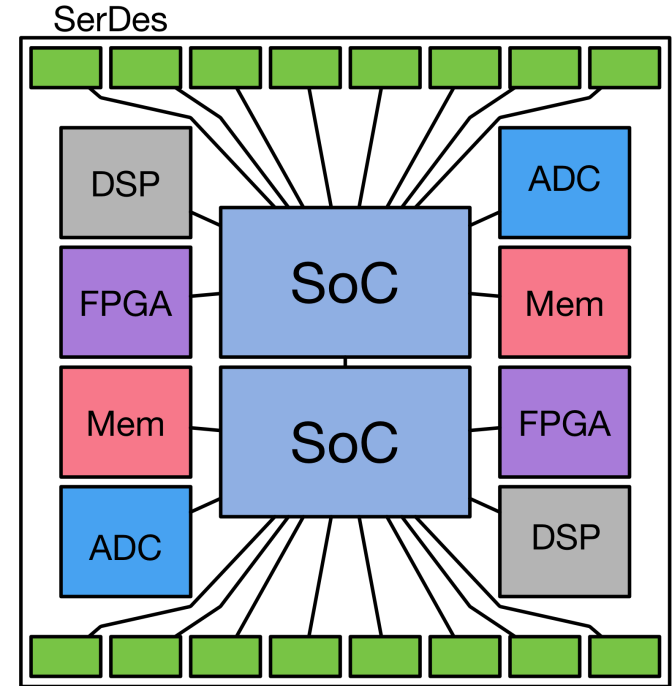
Brian Holden, VP of Standards

Kandou Bus SA

# Chiplet Technology

- A trend in IC technology is to move away from monolithic chips toward the use of chiplets tied together on an MCM
- Chiplets allow the:
  - Combination of many dies into large packages
  - **Improvement in yield and cost** because of a smaller central die(s) – a major factor
  - Distribution of heat away from a single die
  - Use of the best semiconductor process for each die
  - Enabling of multi-vendor ecosystems
  - **I/O subsystem dies containing SerDes to be placed around the perimeter, creating smaller virtual packages**

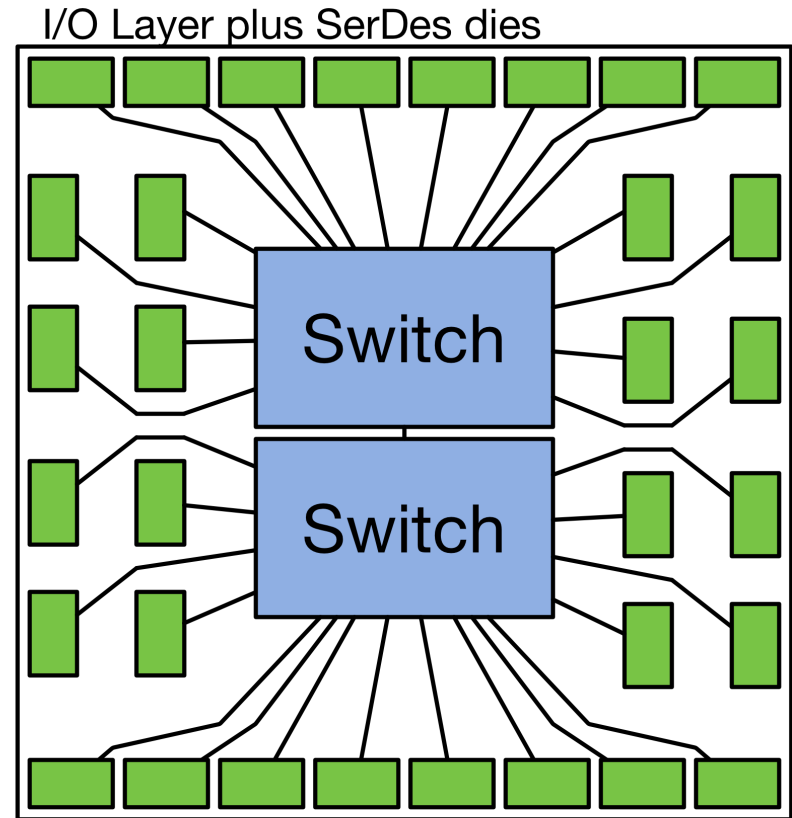
Big, 70mm packages are routine



Non-interposer MCMs can easily use 20 or more dies plus passives

# Chipllets in Switches

- The Ethernet I/O Subsystem including the SerDes can be put on a chiplet
  - Chiplet can have the PCS, FEC and long-reach SerDes and use a fat-pipe packet protocol between devices with a little speed-up factor
  - **Raises yield of switch device**
  - **Use of thin-pipe protocol (i.e. PCS/FEC on main chip) wastes this possible yield gain**
  - 1600 Gb/s is one useful chiplet size
  - Switch-to-chiplet link can use a Femto SerDes
    - A chord signaling Femto SerDes is one example
    - Femto SerDes can reach to the corners of a 70 mm package

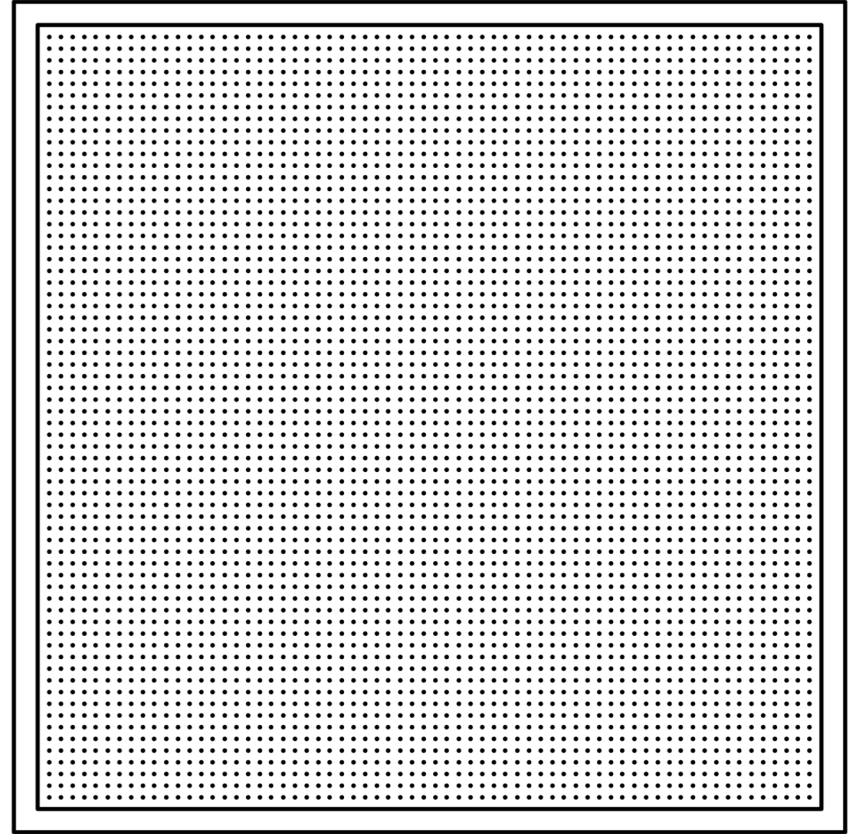


# Detailed package study

---

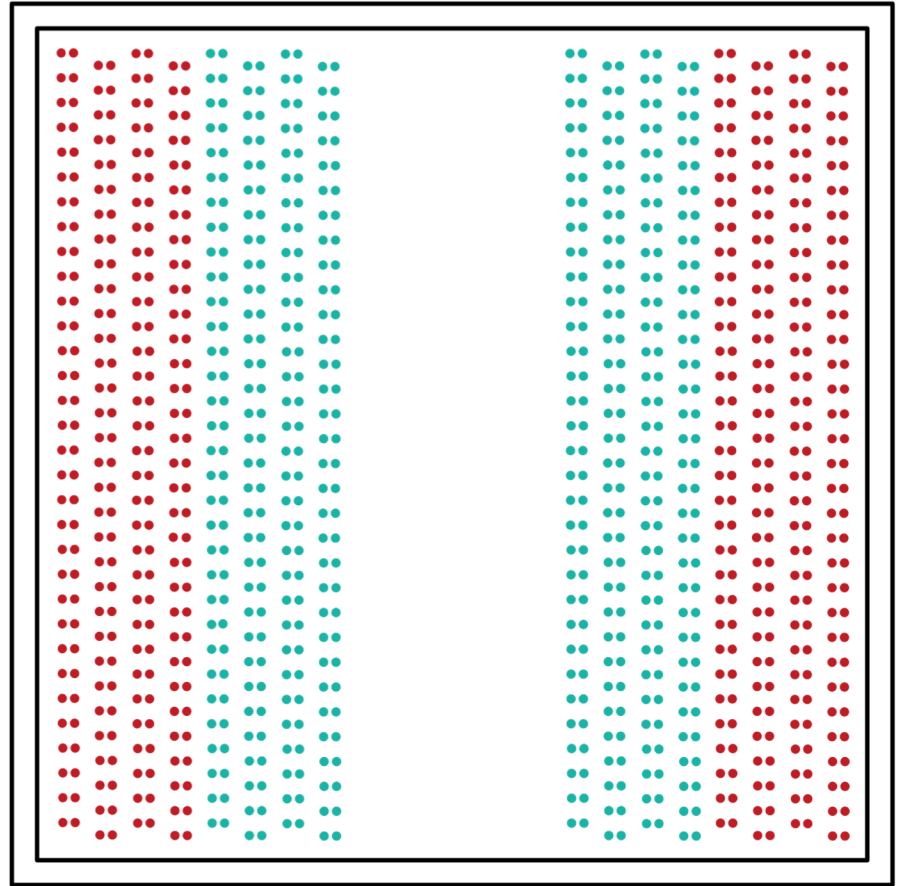
# Package analyzed

- 71 mm BGA package analyzed
- 1 mm ball pitch
- 2.5 mm keep-out



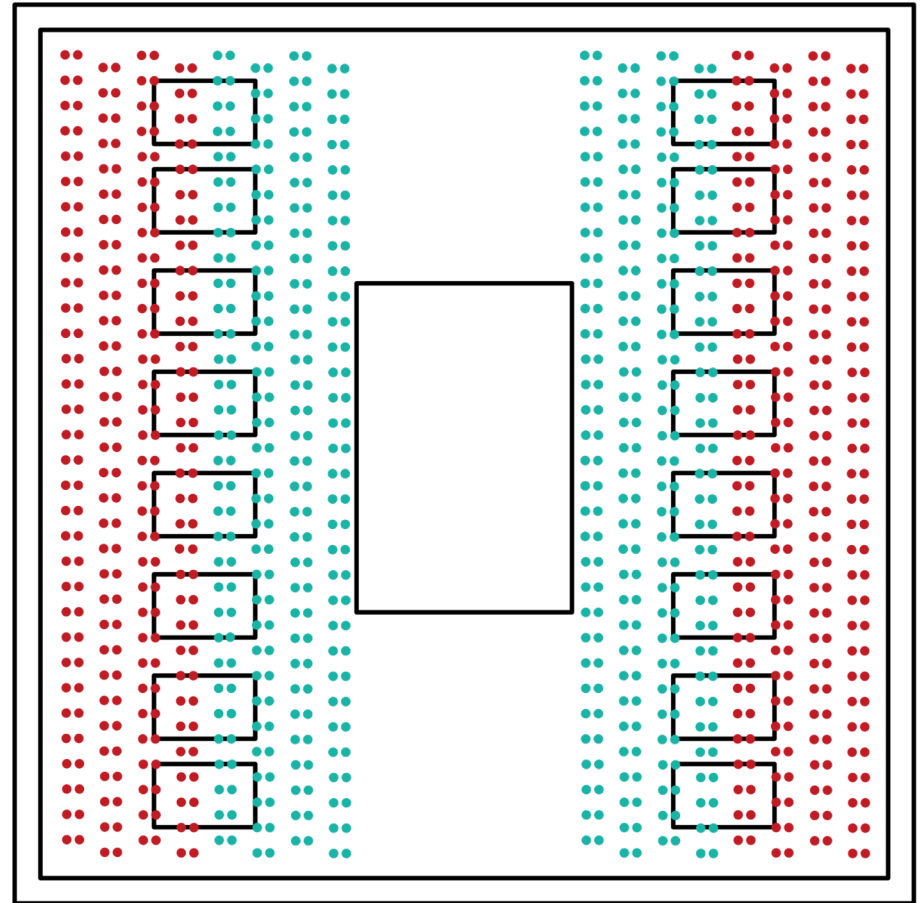
# 25.6 Tb/s Switch Chip analyzed

- 256 Tx and 256 Rx pairs



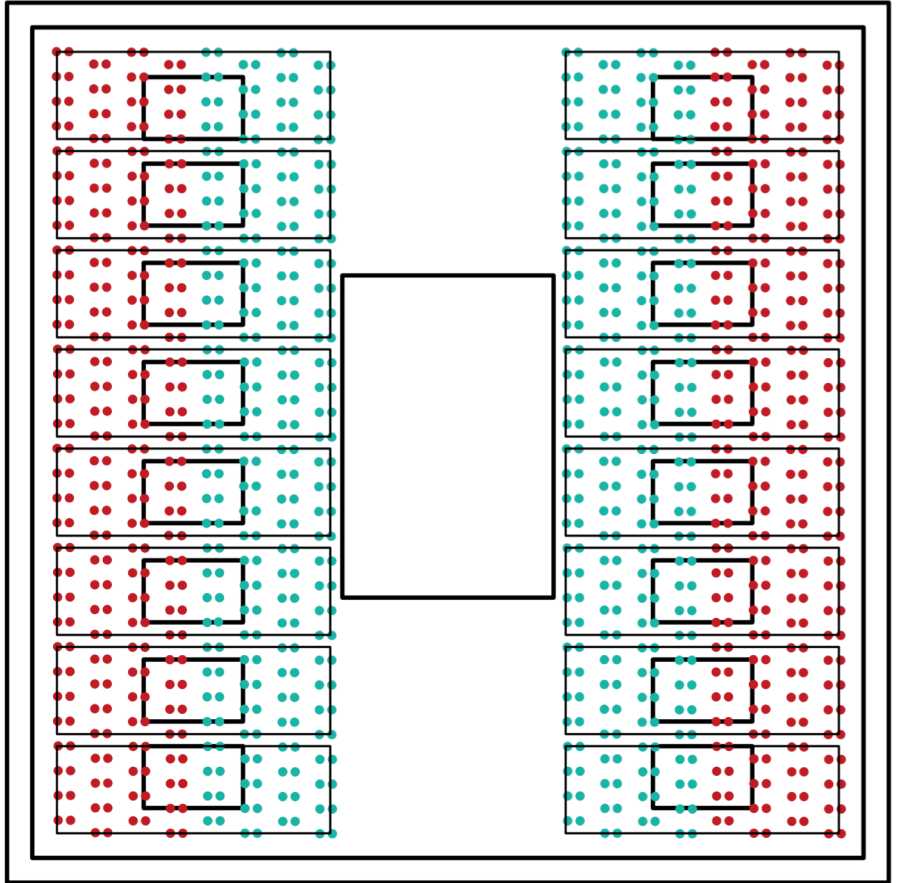
# 16 I/O chiplets

- 16 I/O chiplets containing the full I/O subsystem (PCS, FEC, SerDes, FlexE, SyncE, etc.)
- Central switch chip
- CNRZ-5 Femto SerDes connecting the switch chip to the chiplets
  - Fat-pipe packet link with some overspeed
  - Line protocol not yet applied
  - Not protected by link FEC, uses lightweight FEC



# SerDes traces in tight zones

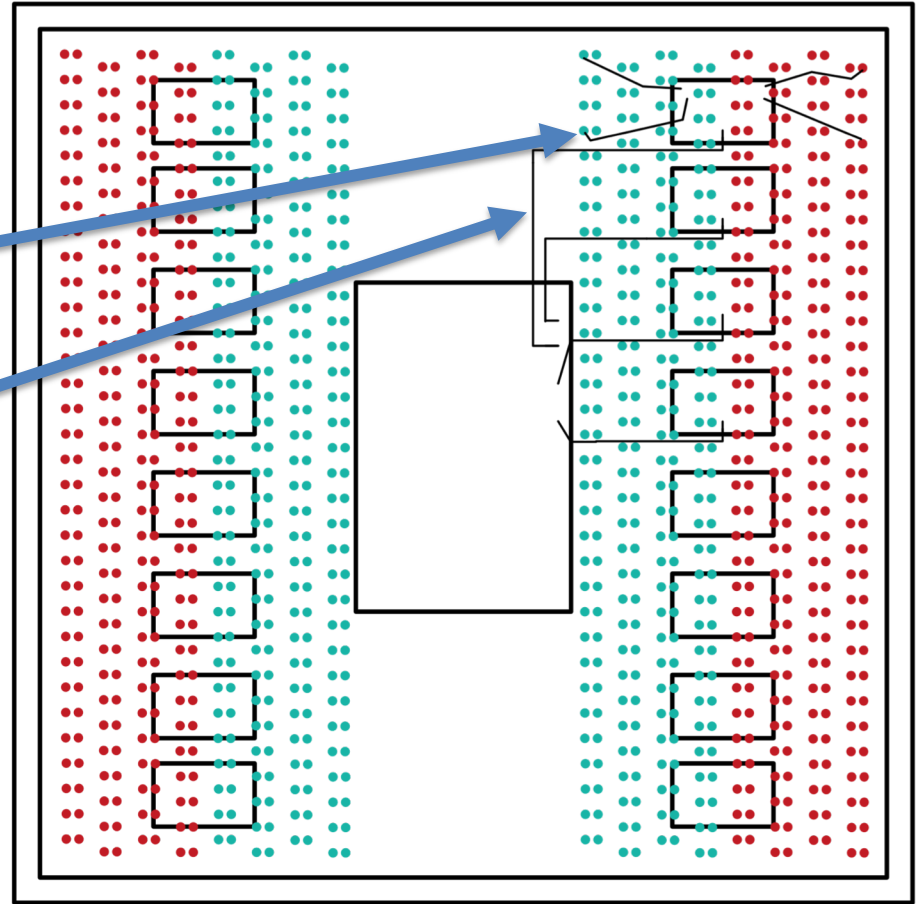
- Package loss constrained by test-chip-like package traces





# Short maximum length traces

- Max SerDes trace is about 11 mm
- Max CNRZ-5 trace is about 34 mm

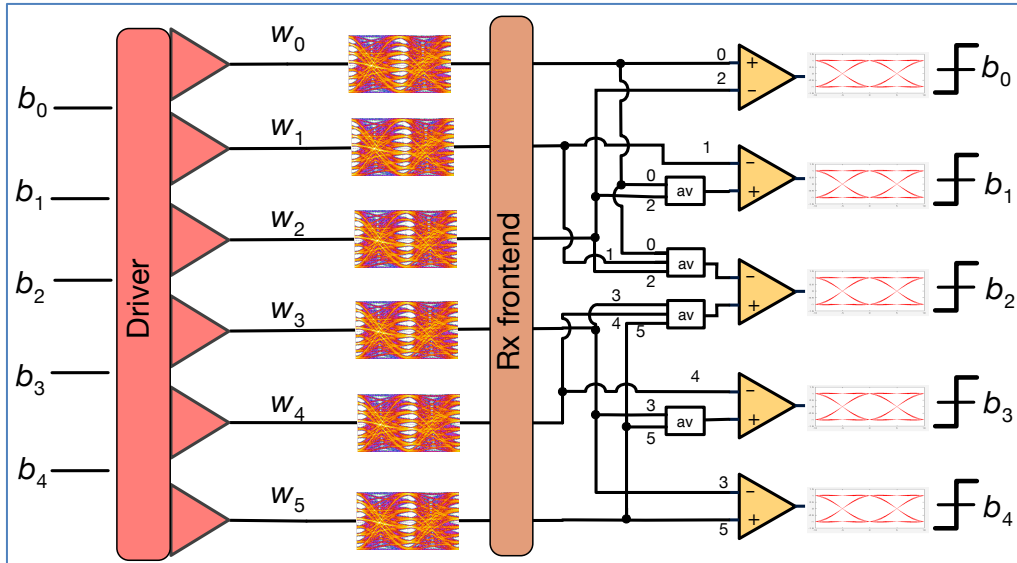


# Example Femto SerDes technology

## Chord signaling

---

# CNRZ-5

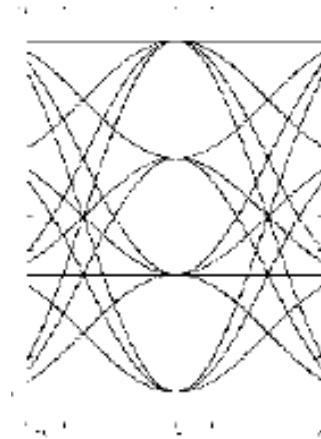


## Advantages:

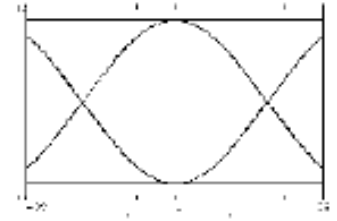
- Ideal for shorter connections including die-to-die interconnect inside a package.
- Balanced values on wires reduce SSO Noise and EMI.
- Tolerates common mode noise similar to differential signals.
- Values at slicers are binary.
  - Similar to NRZ signaling
  - ISI Ratio = 1
- Comparators are self-referencing.

# Key Advantage of CNRZ-5 over PAM-4: ISI Ratio

- Inter Symbol Interference Ratio (ISI Ratio):
  - Inherent property of any given code
  - A rough definition is that it is the code's ratio between the largest and smallest eyes at the decision point
- Energy from the larger eyes bleeds over and tends to close the smaller eyes
  - High ISI Ratio codes require more energy to be spent on ISI equalization
  - High ISI Ratio codes are more vulnerable to reflections



PAM-4's ISI  
Ratio = 3



CNRZ-5's ISI  
Ratio = 1


# OIF & JEDEC

- OIF: ENRZ, CNRZ-5's cousin code, is a part of the OIF's published CEI 4.0 specification
  - Full Interoperability Agreement at 56 Gb/s equivalent throughput
- The OIF announced the CEI-112 in MCM project
  - Kandou has been active in this project
- JEDEC: Both ENRZ & CNRZ-5 published in JESD-247



Implementation Agreement OIF-CEI-04.0 Common Electrical I/O (CEI)

---



**OIF** OPTICAL  
INTERNETWORKING  
FORUM

1  
2  
3  
4  
5  
6  
7  
8  
9  
10  
11  
12  
13  
14  
15  
16  
17  
18  
19  
20  
21  
22  
23  
24  
25  
26  
27  
28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49

**IA Title: Common Electrical I/O (CEI) -  
Electrical and Jitter Interoperability  
agreements for 6G+ bps, 11G+ bps,  
25G+ bps I/O and 56G+ bps**

**IA # OIF-CEI-04.0**

**December 29, 2017**

Implementation Agreement created and approved  
by the Optical Internetworking Forum  
[www.oiforum.com](http://www.oiforum.com)

Optical Internetworking Forum - Clause 0 : Document Structure and Contents 1

# IP Disclosure

- Kandou Bus, S.A. discloses that we own intellectual property related to Chord Signaling and the PHYs described in this contribution.
  - We are committed to adhering to the bylaws of all standards organizations to which we contribute and maintain membership including RAND licensing of our intellectual property.
  - We are committed to being good corporate citizens.

# Thank you!

---

## QUESTIONS?