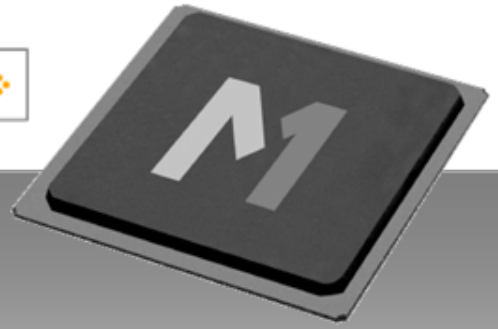
CAUI Loss Budget



Aug 8 2012

MINDSPEED

Agenda

- Recap and new presentations
  - latchman_01_0312.pdf
  - rabinovich_01_080912
- Discussion

Summary from last telecon

- Keep chip-module CAUI 4 budget which is compatible with 802.3bj and VSR
- Make chip to chip spec
  - Compliance points are different relative to chip-module
  - Could allow for higher loss budgets for chip-chip applications

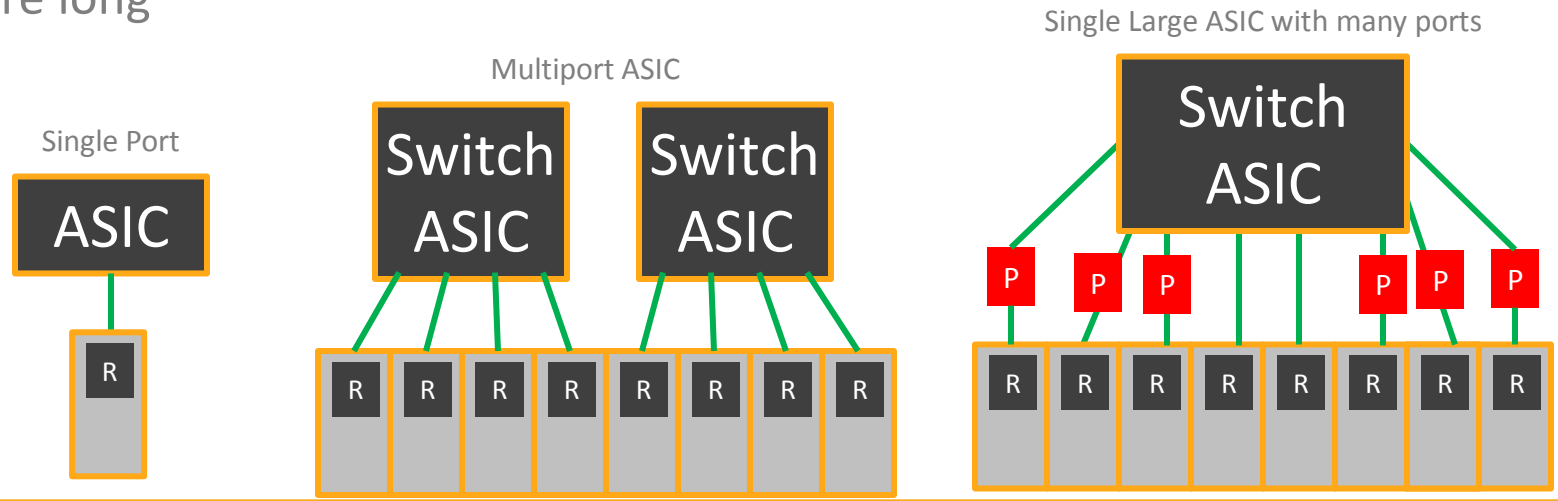
- Question: Is there a need for a second chip-module loss budget?
  - If yes, add another CAUI 4 chip-module budget
  - If no, focus on the above two budgets

Pros and Cons: Single CAUI-4 Chip – Module Loss budget (8.5dB)

Pro	Con
Maintains interoperability with 802.3bj	May need PHY for longer trace lengths
Lower power in module	
Less Silicon Area in Module	

Consider:

- Not all applications require 250mm reach, and in applications that do, not all links are long

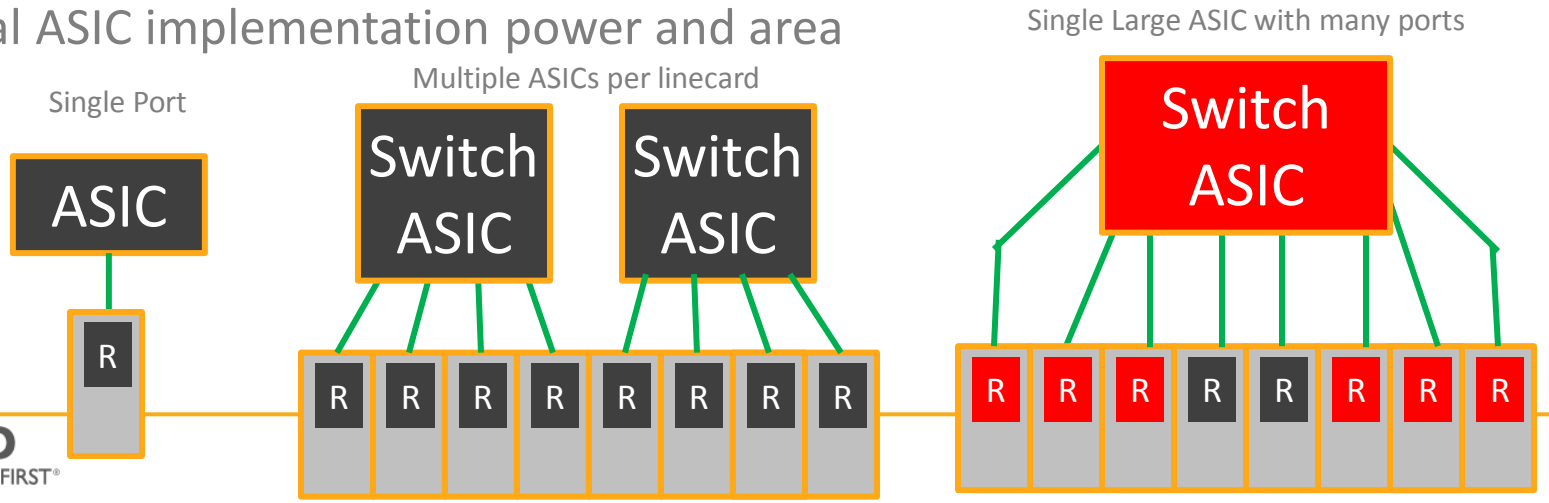


Pros and Cons: Two CAUI-4 Chip – Module Loss budgets (8.5dB, ~17dB)

Pro	Con
Enables repeater less design for longer trace lengths	Creates two port types that are not compatible with each other. Impact upon interoperability between host with longer link, and partner with shorter link compliant to CR4 needs to be considered. How does a CR4 compliant partner accommodate the additional link budget?
	Higher power module (R power increase of 25% - 45%) when functionality is used
	More silicon area in every module

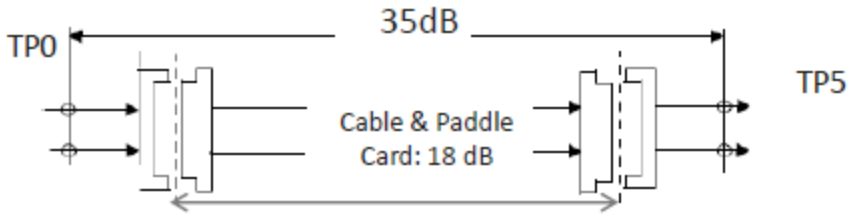
Consider:

- Higher power for module may reduce overall density
- Potential ASIC implementation power and area



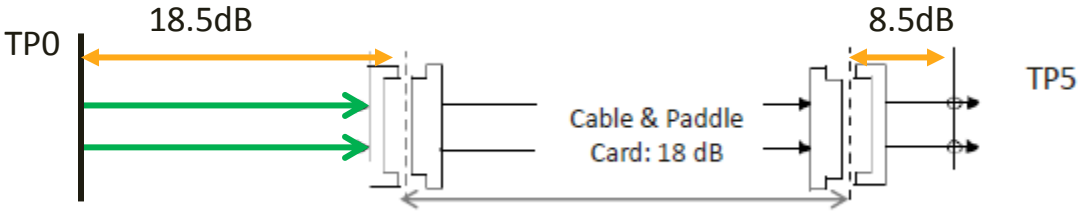
CR4 Compatibility Issue

- CR4 budget:



CR4 Budget: 5 m cable assembly link budget example with 8.5 dB host loss: 35 dB @12.89 GHz (FEC Required)

- Implication of higher loss CAUI-4



45dB link budget significantly higher than 802.3bj baseline

Additional Thoughts

- Single CAUI4 Chip – Module budget
  - System designers have flexibility to implement their system which meets interoperable chip-module loss
    - Keep losses low to keep within budget
      - 8.5dB host loss budget assumes Meg6_HighSR-narrow (1.7dB/in @14GHz)
      - Extend reach by using ImpFR4_LowSR-narrow (1.55dB/in @ 14GHz) or ImpFR4_LowSR-wide (1.27dB @ 14GHz) or Meg6_LowSR-Wide….
    - Use PHYs if you have to (similar to architecture used at 10G)
    - Use other design techniques to support longer reach while meeting CR4 compliance requirements
  - Adding another chip-module loss budget: con's out weigh the pro
    - Interoperability issue makes it outside the box, increasing the burden on the user
    - High loss links likely a minority, but the solution burdens the majority from a power and area point of view
    - If consensus moves in this direction consider 15dB, 20dB and 25dB loss budget
      - 25dB allows for ImpFR4_HighSR-Narrow over 10inches of trace