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### **CAUI-4 PHY Interface Options**

- How many PHY interfaces do we need to specify?
- Chip-to-Chip Specification
- Chip-to-Module Specification
- Summary
- Q&A

How Many PHY Interfaces?

- There are 3 PHY interfaces being considered
  - 1. 802.3bj chip-to-module (copper direct attachment)
  - 2. 802.3bm chip-to-module (module repeater)
  - 3. 802.3bm chip-to-chip
- Question:

Can (and should) we merge some or all of these interfaces in a single PHY interface?



802.3bm CAUI-4 Chip-to-Chip PHY Interface

- Reference: Annex 83A CAUI objective 25 cm (~10 inches)
- Assumptions
  - 1. PCB IL 1.6dB/inch @14GHz
  - 2. 1dB IL for 2 vias

For 12 inches ILmax = 1dB (vias) + 19.2dB (PCB loss) = 20.2dB ~ 20dB (1)

(1) Consistent with latchman\_0726.pdf



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#### 802.3bj and 802.3bm Chip-to-Chip PHY Interface Overlap

- 802.3bm should overlap 802.3bj
- Accommodate benefit of repeater within module



	Total Channel IL Budget (dB)	IL Contribution (dB)				Host Board	
Scenarios		Connector Loss	MCB Loss	2 Via Loss	Host PCB Loss	Maximum Length (inch) (1)	Comments
1	10	1.2	1.5	1	6.3	4	802.3bj (2)
2	15	1.2	1.5	1	11.3	7	
3	20	1.2	1.5	1	16.3	10	Consistent with CAUI Annex 83A Consitent with 20dB IL budget for to chip-to-chip

(1) Assumed PCB IL 1.6dB/inch @14GHz

(2) From latchman\_0726.pdf



Summary - Proposal

CAUI-4 PHY Interface Proposal

- Define 2 PHY interfaces :
  - 1. 20dB total channel IL (normative): "CAUI-4 Interface" port
    - Chip-to-chip or chip-to-module channel
      - a. Chip-to-chip channel
        - 20 dB host board IL including 2 vias (normative)
        - 12 inch host board channel length (informative)
      - b. Chip-to-module channel
        - 17.3 dB host board IL including 2 vias (normative)
        - 10 inch host board channel length (informative)
  - 2. 10dB total channel IL (normative): "100GBASE-CR4 Interface" port
    - Chip-to-chip channel
      - Low Power Mode (10GBASE-T PHY precedence)
      - 7.3 dB host board IL including 2 vias (normative)
      - 4 inch host board channel length (informative)
      - Consistent with 802.3bj
- Interfaces could share the same PHY pinout, i.e., 2 instantiations in same PHY
- Dual-PHY interface modules power mode configurable via MDIO
  - Specify management register map bits (normative)



#### Summary - Addressing Compatibility Issues

- The host CPU already knows whether the port is short or long
  - Host CPU configures the host PHY interface appropriately
- Host port interface is displayed as a CAUI-4 or 1000GBASE-SR4
- If module can support either interface
  - Host CPU configures module PHY interface appropriately
- If module supports one interface or the other but not both
  - Port may not work
  - Precedence: same SFP+ port socket may support 10GBASE-SR/-LR modules but it may not support LRM and/or SFP+ Annex E (direct copper attachment)
  - Caveat Emptor ("Buyer Be Aware")



CAUI-4 PHY Interface Options

# Thank you !

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