

# Study of PAM modulation for 100GE over a single laser

Sudeep Bhoja, Broadcom

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# Contributors

- Howard Frazier, Broadcom
- Ali Ghiasi, Broadcom
- Hari Shankar, Inphi
- Francis Ho, Inphi
- Beck Mason, JDSU
- Kevin Zhang, JDSU
- Arlon Martin, Kotura
- Vipul Bhatt, Lightwire
- Chris Bergey, Luxtera
- Brian Welch - Luxtera

# Supporters

- Mark Nowell, Cisco
- Gary Nicholl, Cisco
- Matt Traverso, Cisco
- Harold Kamisugi, Sumitomo Electric (SEI)
- Scott Kipp, Brocade
- Ted Sprague, Infinera
- Matt Brown, APM

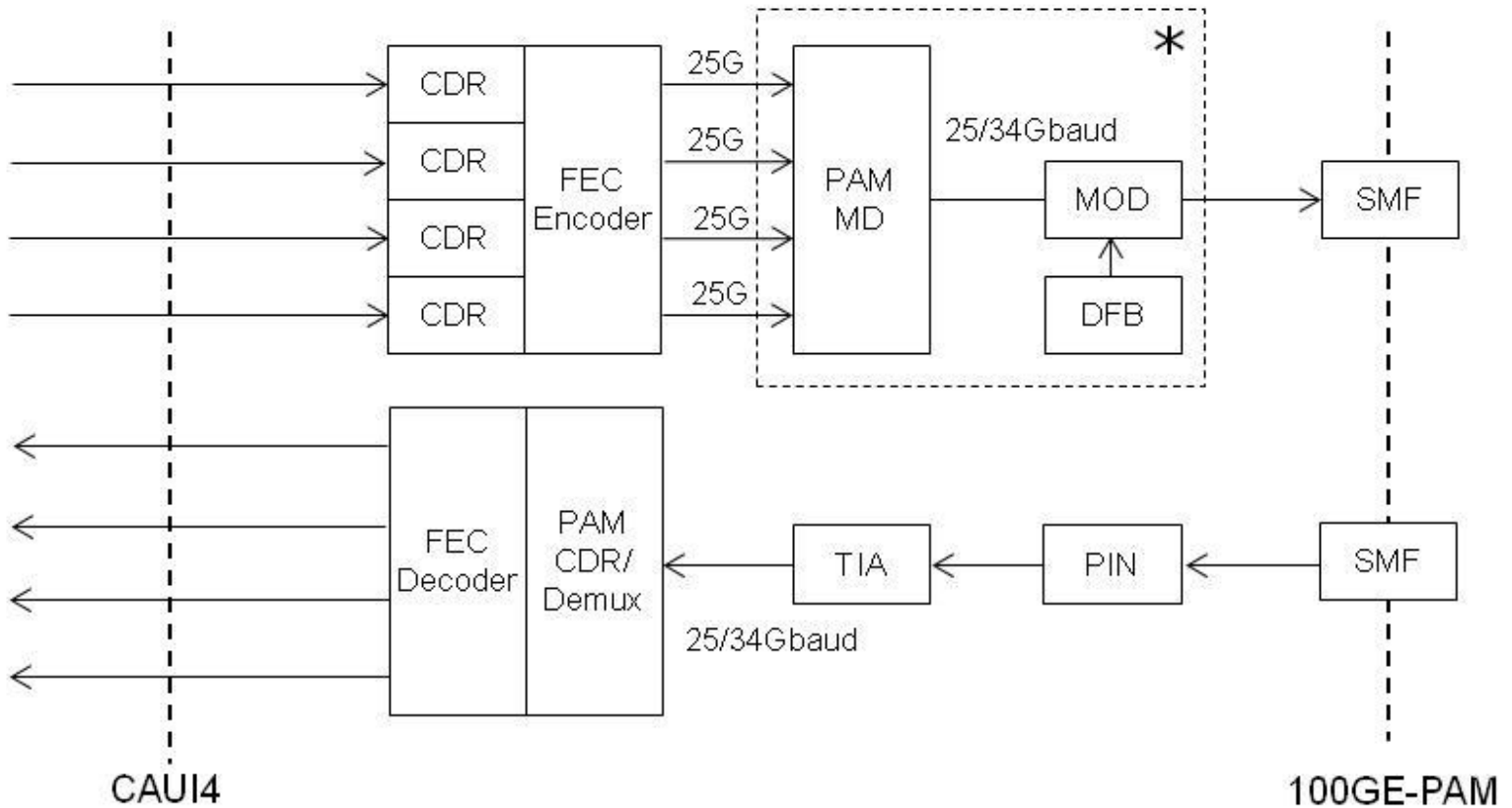
# Outline

- Introduction
- PAM8 System Model
- Building Blocks
  - 2 Examples of PAM Transmitters
  - 2 Examples of Multilevel CDR/Rx
  - FEC
- PAM8 Link Budget
- PAM16 System Model & Link Budget
- Summary
- Next Steps

# Introduction

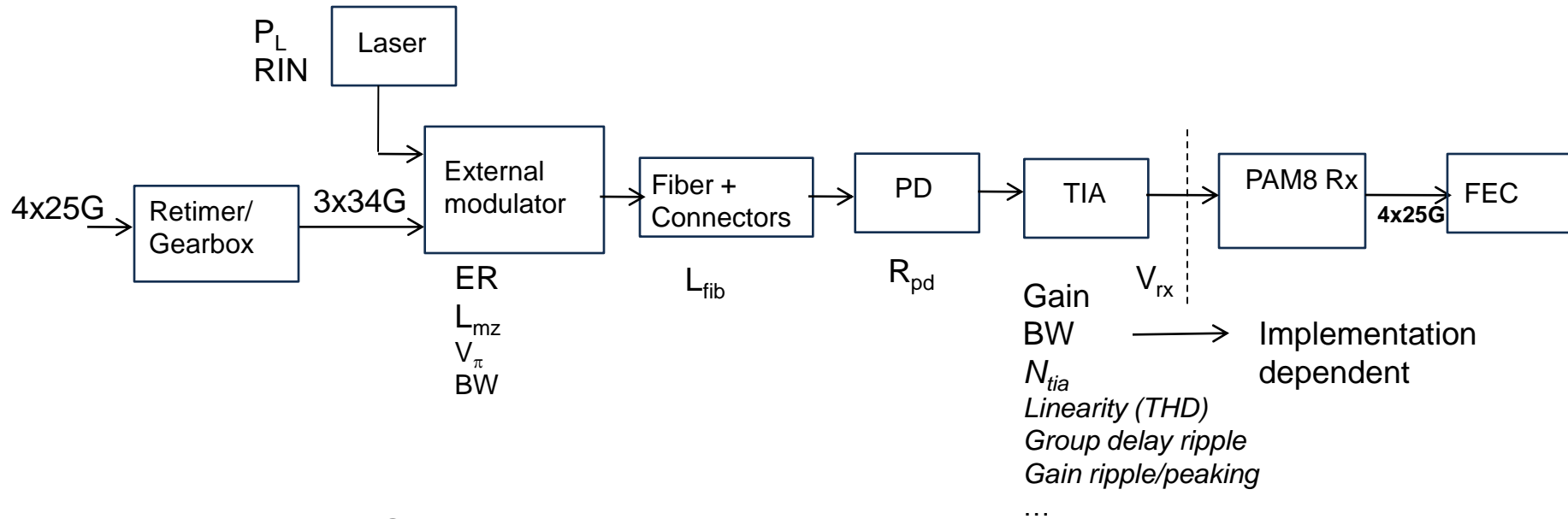
- Nowell\_01\_1111 suggested that alternate schemes might help deliver step function reduction in cost over 100GBASE-LR4
  - The number of lasers has direct impact on cost
- This work investigates feasibility of PAM modulation over a single laser
- PAM8 and PAM16 modulation are investigated
  - Wavelength: 1310nm
  - Optical Loss Budget: 4dB
  - Link length: 500m to 2km
  - Externally modulated laser
- PAM8 and PAM16 modulation are investigated

# PAM Block Diagram



\* Multiple Implementations possible

# PAM8 System Model



- Tx includes a 4:3 Gearbox inside the module
  - Converts 4x25.78125 Gb/s to PAM8 at 34.375 Gbaud
  - Single Laser externally modulated to 8 PAM
  - Baud Rate 34.375 Gbaud, 3 bits/baud
- A single PAM8 Rx CDR recovers the data and de-multiplexes to 4x25G
  - Host based FEC targets input BER of 1E-5, output BER 1E-15

# Example Multilevel Modulator - I

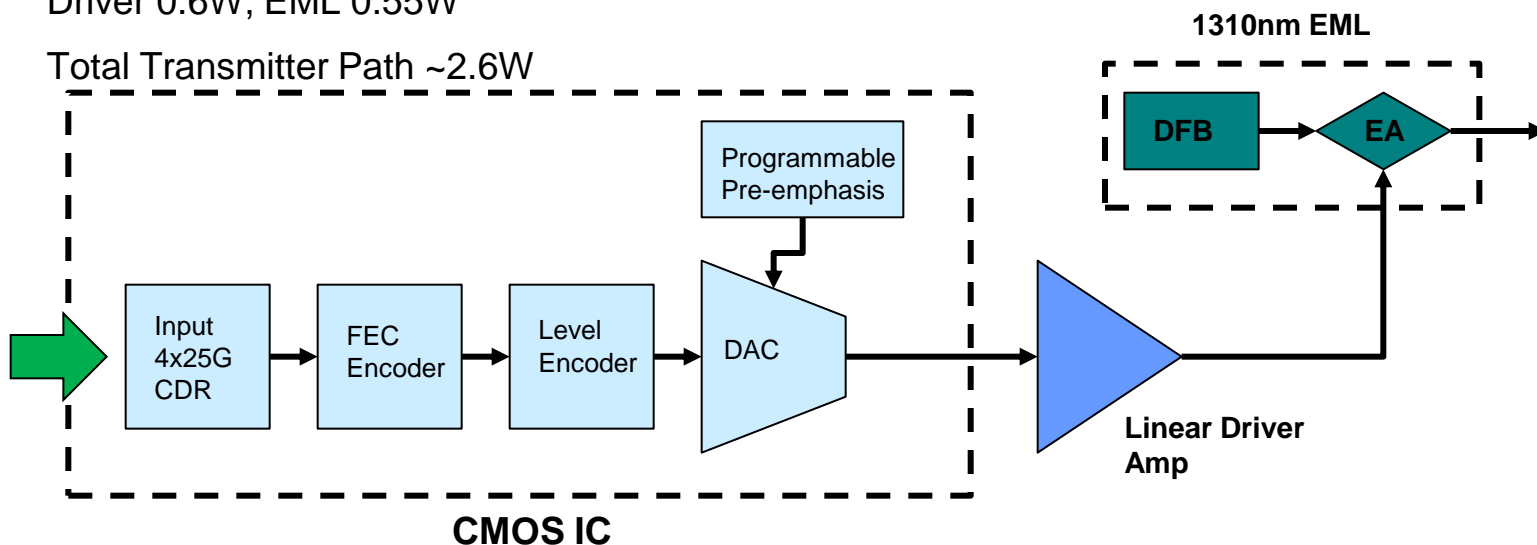
- Example of digital generation architecture for multilevel modulation
  - Simple single 1310nm EML laser source
  - CMOS IC with quad CDR, FEC encoder, level encoder, and DAC
    - Level encoder and higher resolution DAC enables
      - Digital linearization of modulator transfer function
      - Multilevel coding with non-equal level spacing for optimum SNR performance

- Estimated power dissipation

DAC 0.4W, Quad CDR 0.8W, FEC and Encoder 0.25W – 1.45W

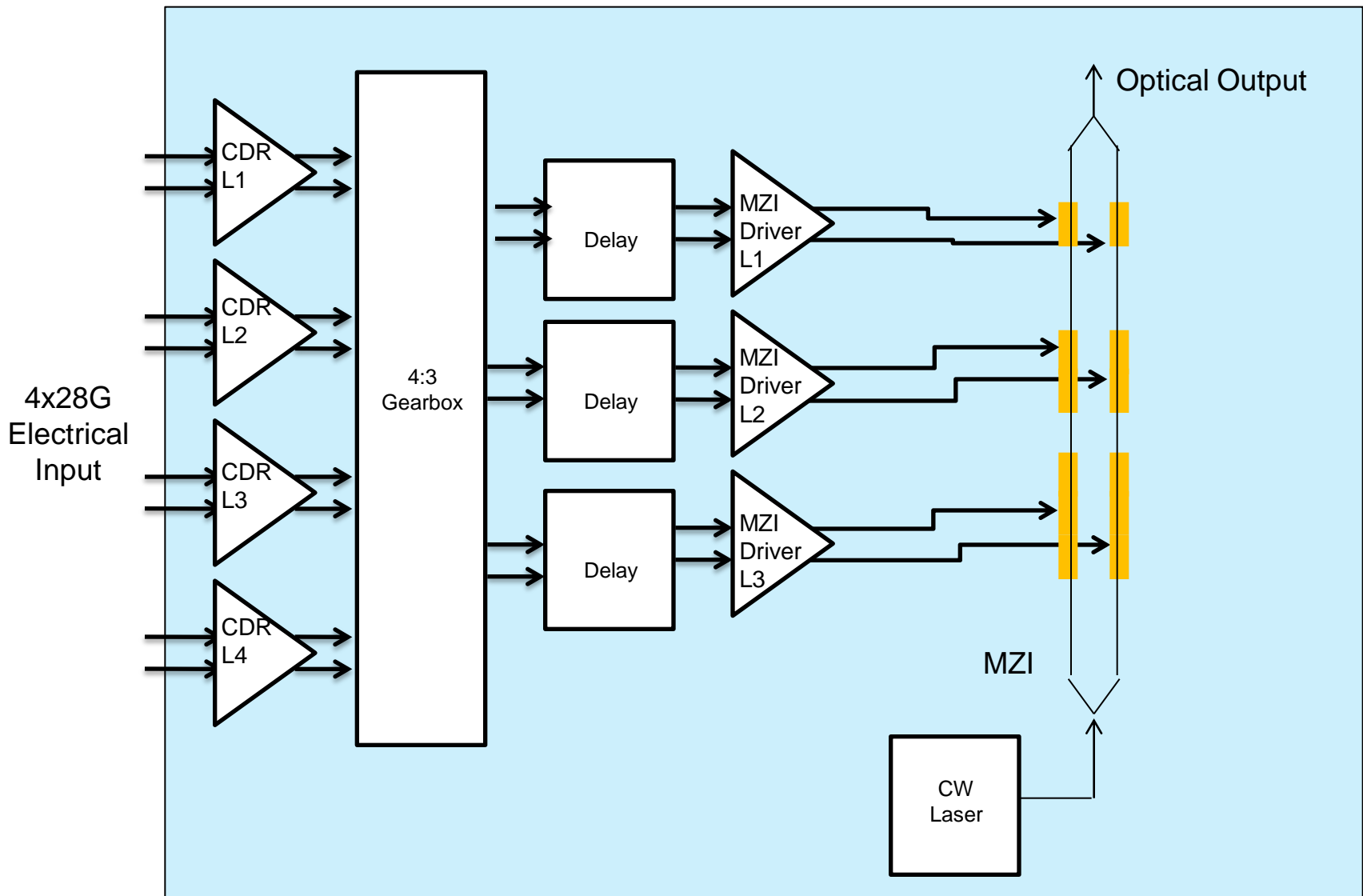
Driver 0.6W, EML 0.55W

Total Transmitter Path ~2.6W



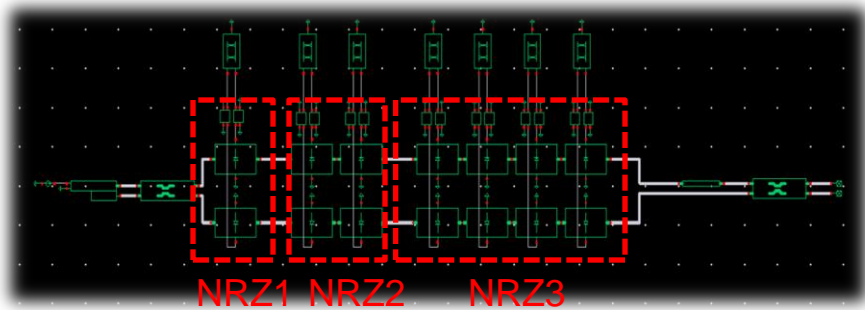


# Example PAM8 Tx II – Multi-segmented MZI

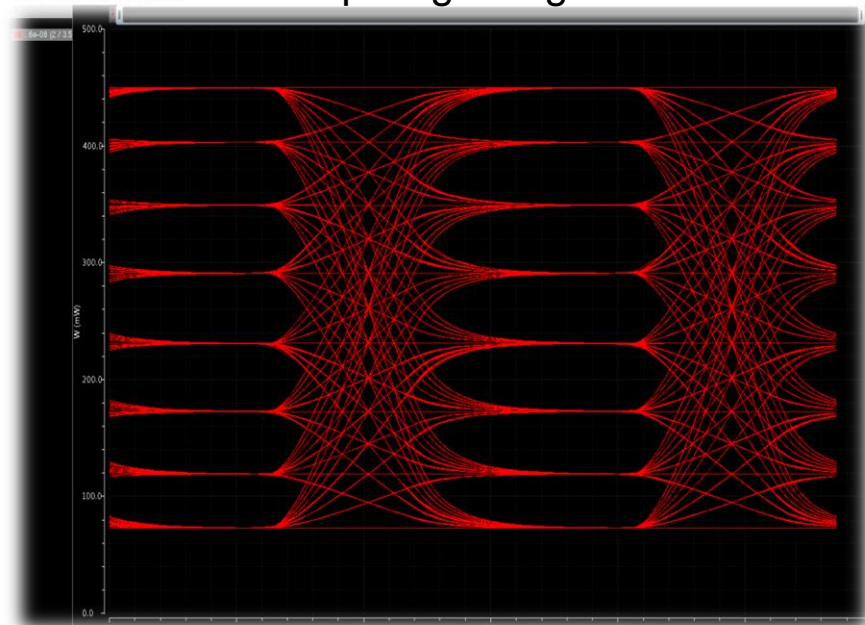


# PAM-8 Transmitter in Silicon Photonics

Opto-electronic Schematic



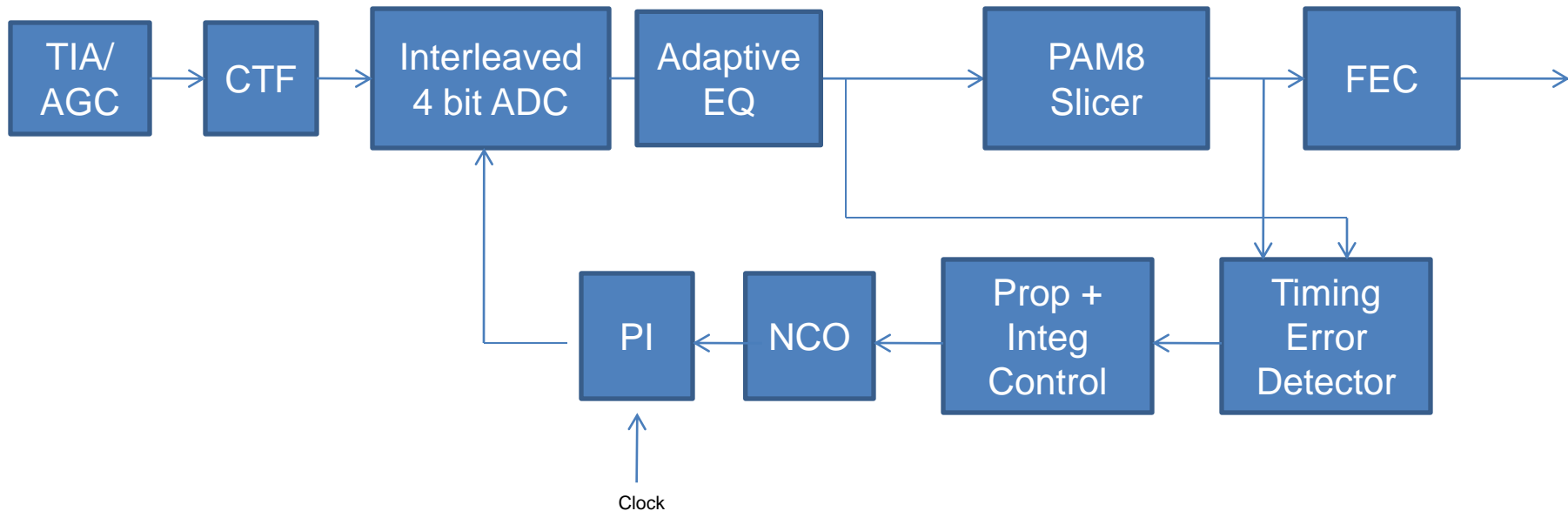
PAM-8 at 35 Gbps signaling rate



## Multi-segmented MZI:

- Accepts direct NRZ encoding
- Allows for non-linear modulator drivers
  - Low Power (CMOS drivers)
  - Low Headroom
- Enables low parasitic interconnects between electronic and photonic building blocks
- Allows for better electro-optical phase matching

# Example Digital Multilevel CDR/RX



- PAM8 requires a 7 level slicer to recover data
- 1 sample/bit baud rate timing recovery is commonly used for multilevel Clock Data Recovery
- 4 bit ADC sampling at 34.375 Gsamples/s

# Digital Multilevel Rx feasibility

- A 34GS/s parallelized baud rate timing error detector <sup>5</sup> and CDR implementation is feasible
- A 5.1 ENOB low power ADC at 10 Gbps KR line rate in 65 nm has been demonstrated in literature<sup>6</sup>
- For coherent receivers in optical communications, a 8 bit ADC at 56 Gbps has been demonstrated showing that higher ENOB, higher speed ADC's are feasible<sup>7</sup>
- Technology changes from 65 nm to 20 nm allow further increases in speed
- ADC POWER: <300 mW (extrapolation from reference 6&7)

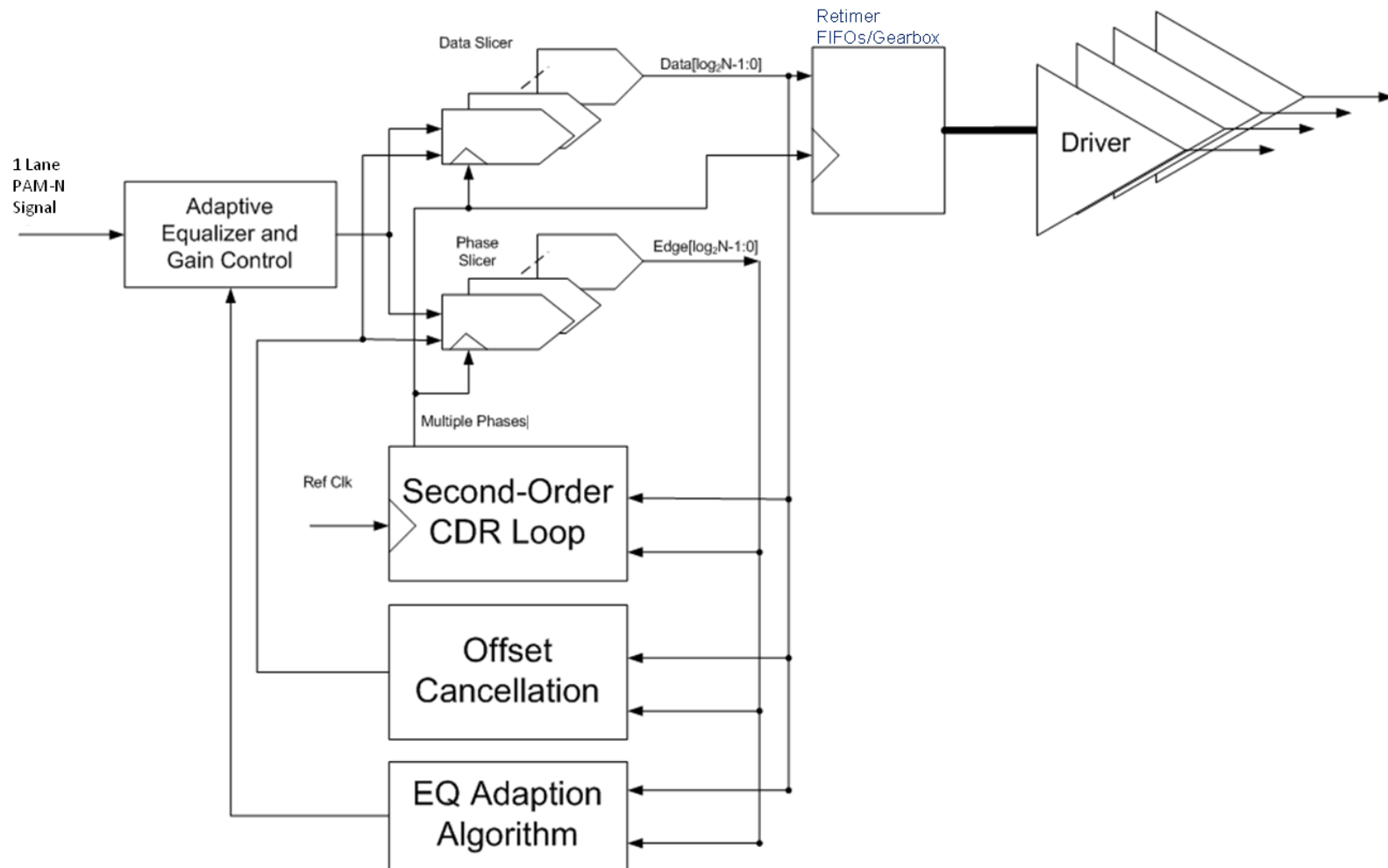
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<sup>5</sup> K. H. Mueller and M. S. Muller, "Timing Recovery in Digital Synchronous Data Receivers", *IEEE Transactions on Communications*, vol. COM-24, pp. 516-531, May 1976

<sup>6</sup> J.Cao et. al., "A 500 mW ADC-Based CMOS AFE With Digital Calibration for 10 Gb/s Serial Links Over KR-Backplane and Multimode Fiber", *IEEE Journal on Solid State Circuits*, June 2010

<sup>7</sup> <http://www.fujitsu.com/downloads/MICRO/fme/dataconverters/OFC-2010-56Gss-ADC-Enabling-100GbE.pdf>

# Example Of An Analog Multilevel CDR/RX



- Analog and digital PAM CDR/Rx architectures are possible

# FEC feasibility

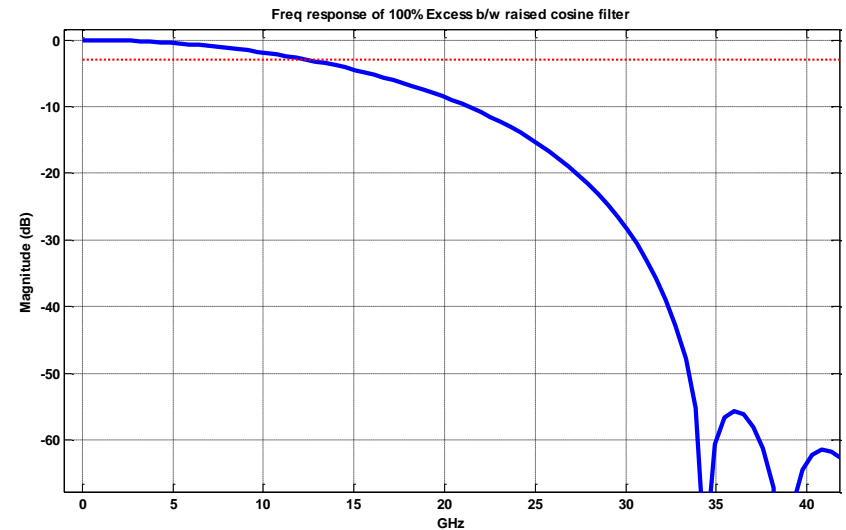
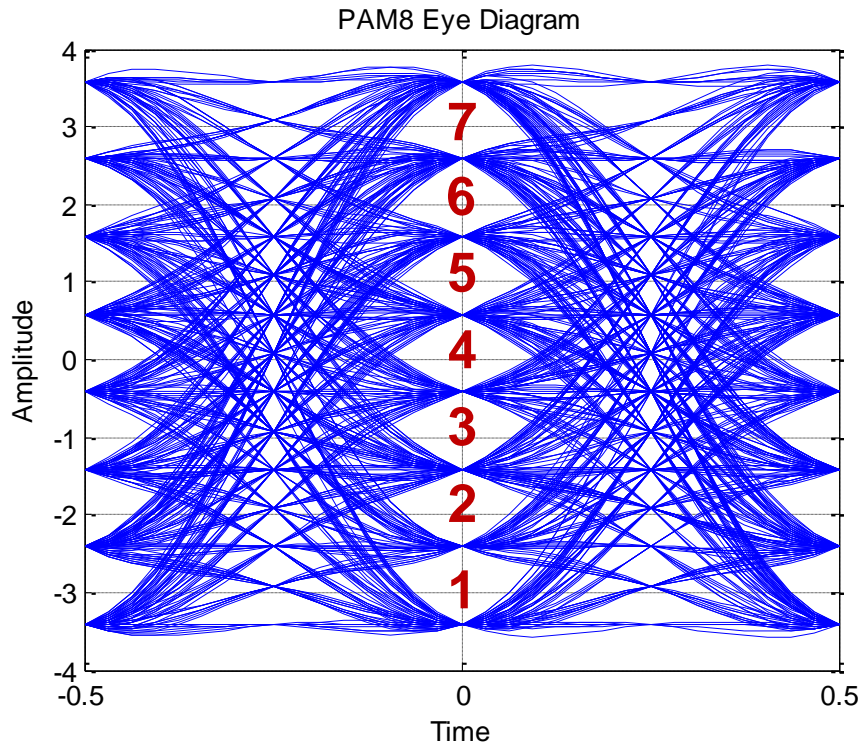
- Block codes which provide 5 dB coding gain are readily available and have been presented at IEEE <sup>9,10</sup>
- G.975 RS(255,239) already implements a FEC with 6dB gain at ~10.5 Gbps
- Example 100G FEC – 0% overhead
  - 512b/514b transcoding to extract overhead information
  - RS(528, 514, t = 7) over GF(2<sup>10</sup>), supports 1E-5 input BER
  - Possibly reuses 100G FEC designed to support front panel DAC, SR4 and backplanes
  - Metrics from synthesis in 40nm (gustlin\_01\_0112)
    - Latency: 99.4ns
    - Total Area (40nm gates): 275K gates
    - Power: 101mW

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<sup>10</sup> [http://www.ieee802.org/3/bj/public/nov11/cideciyan\\_01a\\_1111.pdf](http://www.ieee802.org/3/bj/public/nov11/cideciyan_01a_1111.pdf), R. Cideciyan and J. Ewen, IEEE Nov 2011

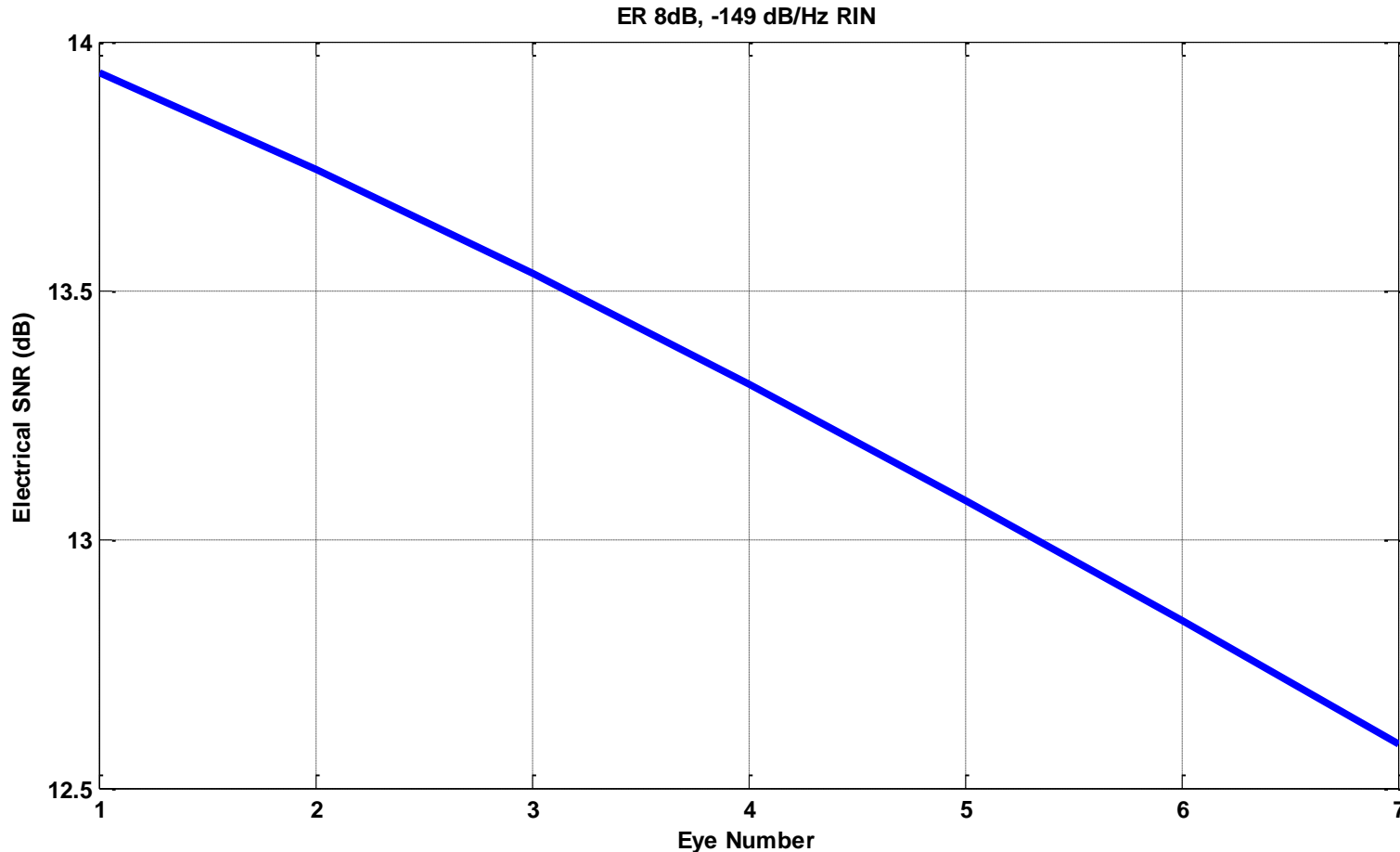
<sup>9</sup> [http://www.ieee802.org/3/100GCU/public/mar11/gustlin\\_02a\\_0311.pdf](http://www.ieee802.org/3/100GCU/public/mar11/gustlin_02a_0311.pdf), S. Bhoja and M. Gustlin, IEEE March 2011

# PAM8 Rx Eye



- 100% Excess Bandwidth – Ideal Raised cosine
  - 3dB BW 12.5GHz, 0.4UI Horizontal Eye Opening (Qualitative Metric. See bliss\_01a\_1111 in 802.3bj for detailed discussion)
- 8.4dB Optical penalty, 7 “inner eyes”
- SNR is computed for each individual eye
$$\text{SNR}_i \text{ (dB)} = 20 * \log_{10} \left( \frac{V_i - V_{i-1}}{\text{Sigma}_i + \text{Sigma}_{i-1}} \right)$$

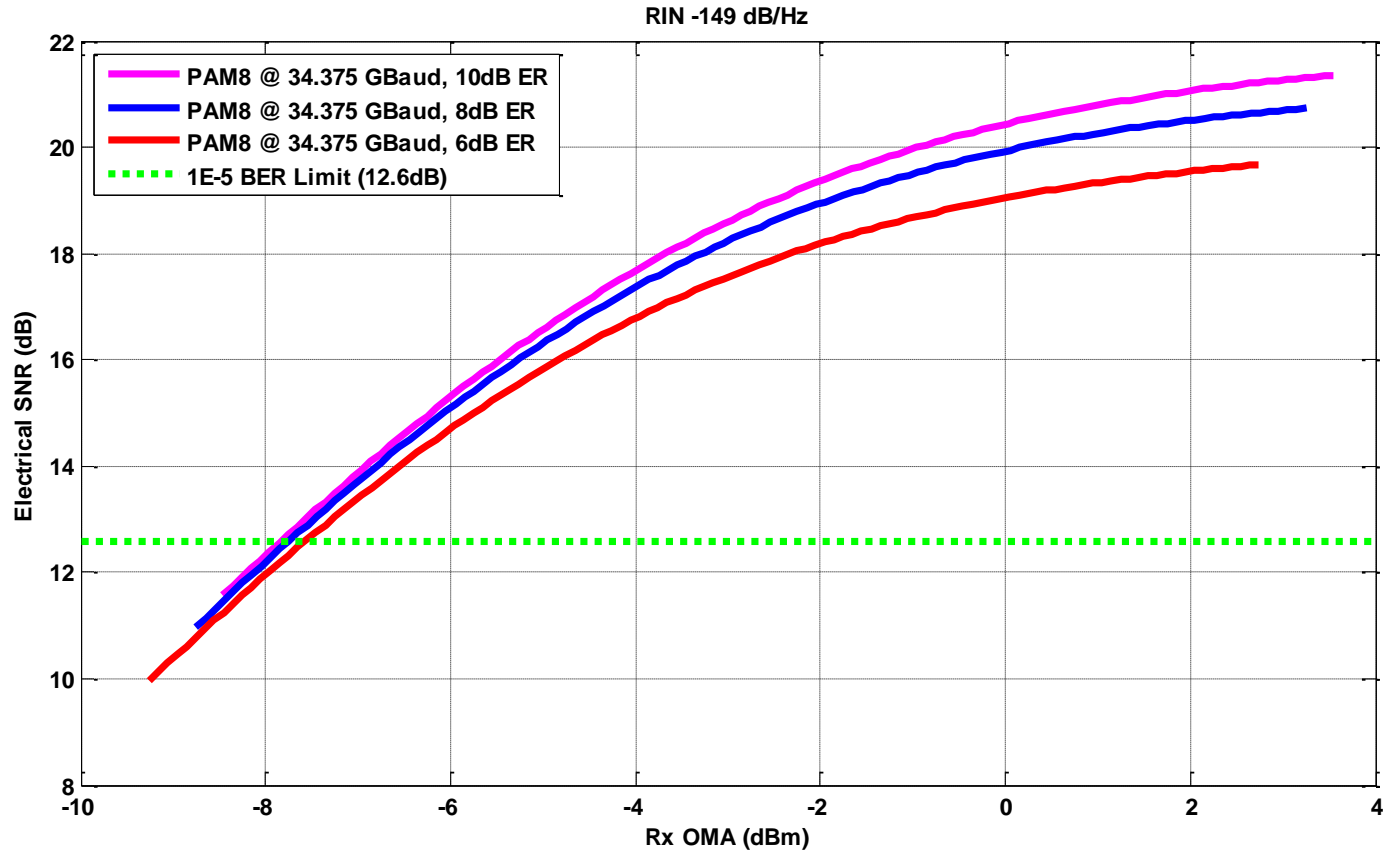
# PAM8 Rx SNR



- Noise is signal dependent resulting in variation of SNR
- Equal spacing at Tx results in 2dB SNR variation among 7 “sub-eye” diagrams
- Worst case SNR assumed in subsequent link budget

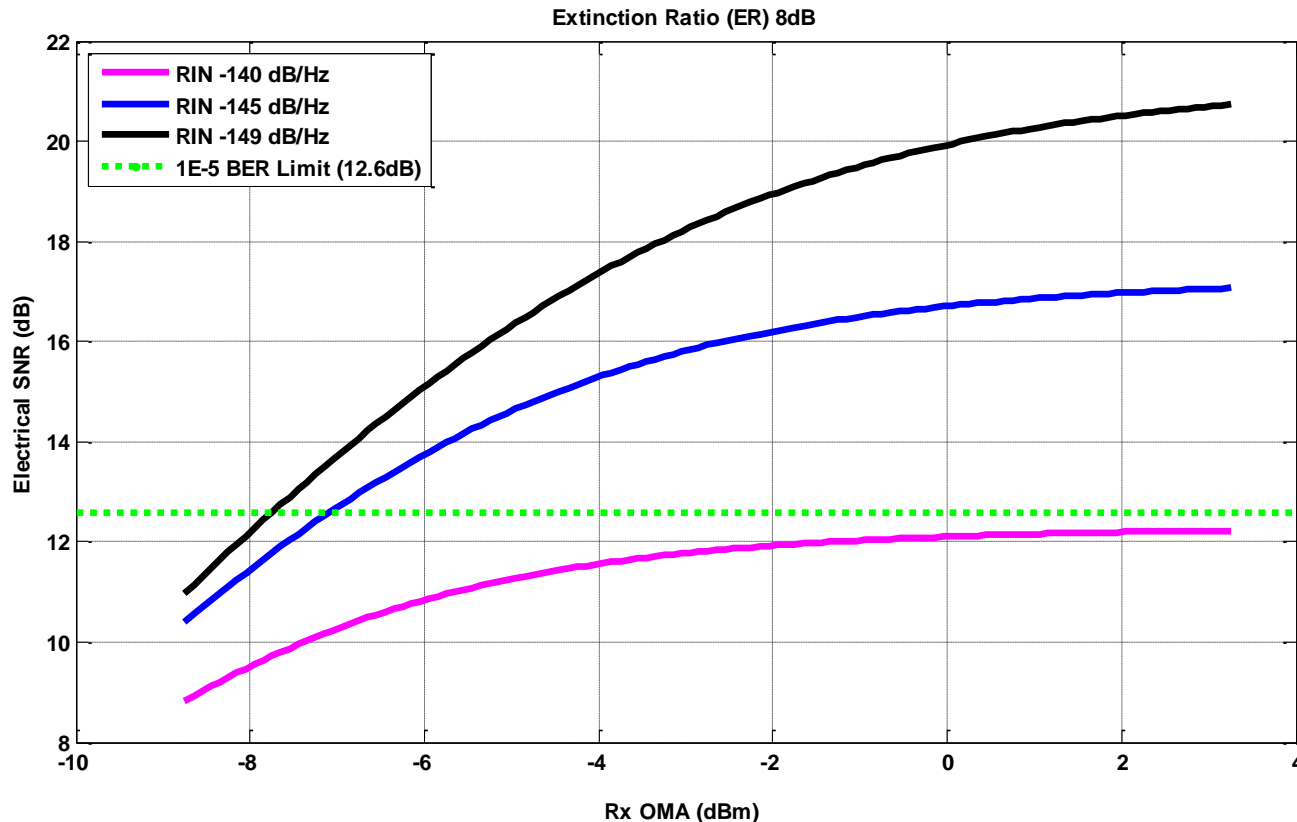


# PAM8 Rx performance (ER)



- Extinction Ratio varied from 6-10dB
  - ER defined as ratio of 7<sup>th</sup> level (P7) to 0<sup>th</sup> level (P0)
- -7.75dBm Rx Sensitivity with RIN, Shot and thermal noise for ER = 8dB

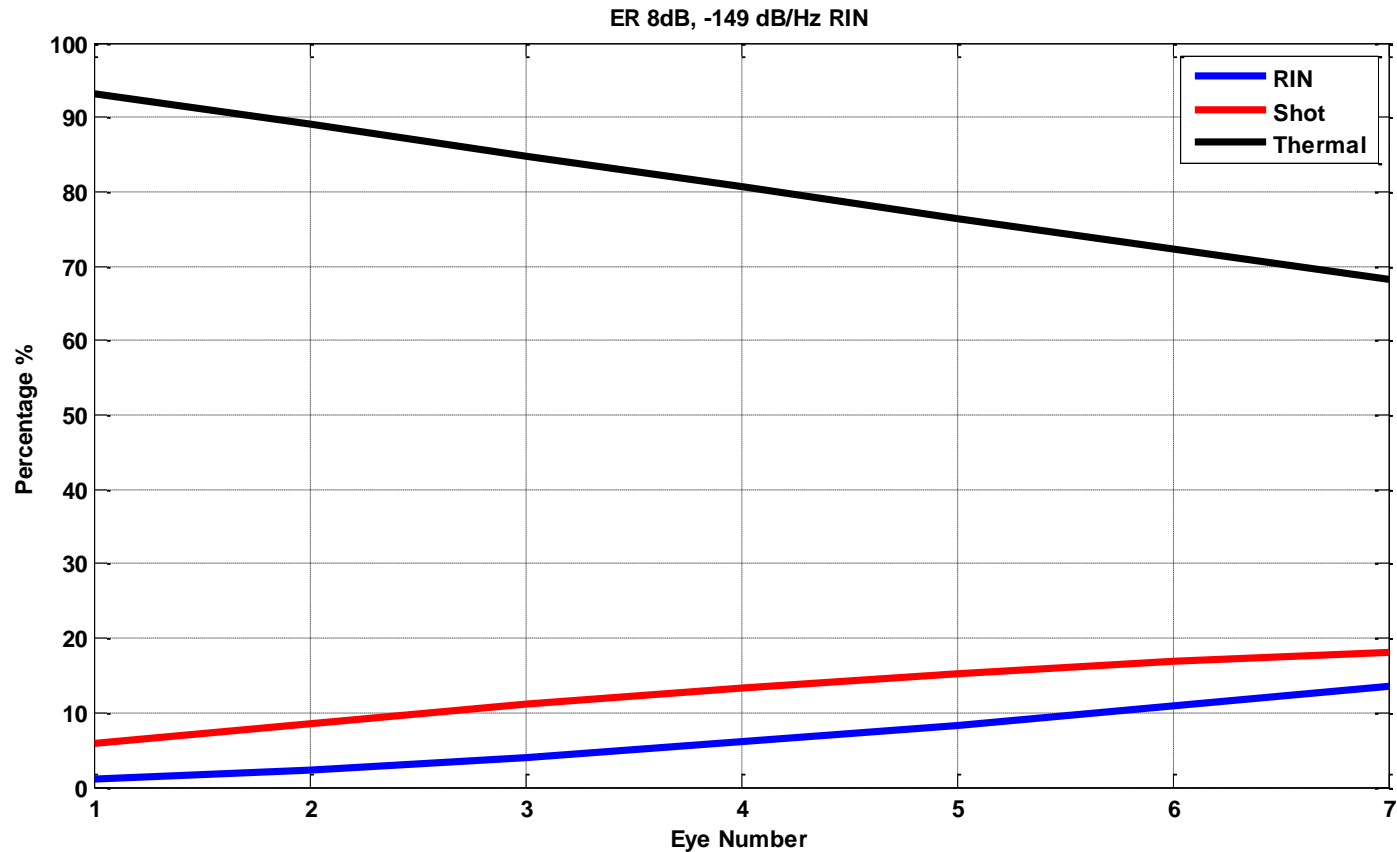
# PAM8 Rx Performance (RIN)



- -140 dB/Hz RIN results in error floors
- -149 dB/Hz RIN provides very good performance.
- RIN can be low when laser operates at high power and CW

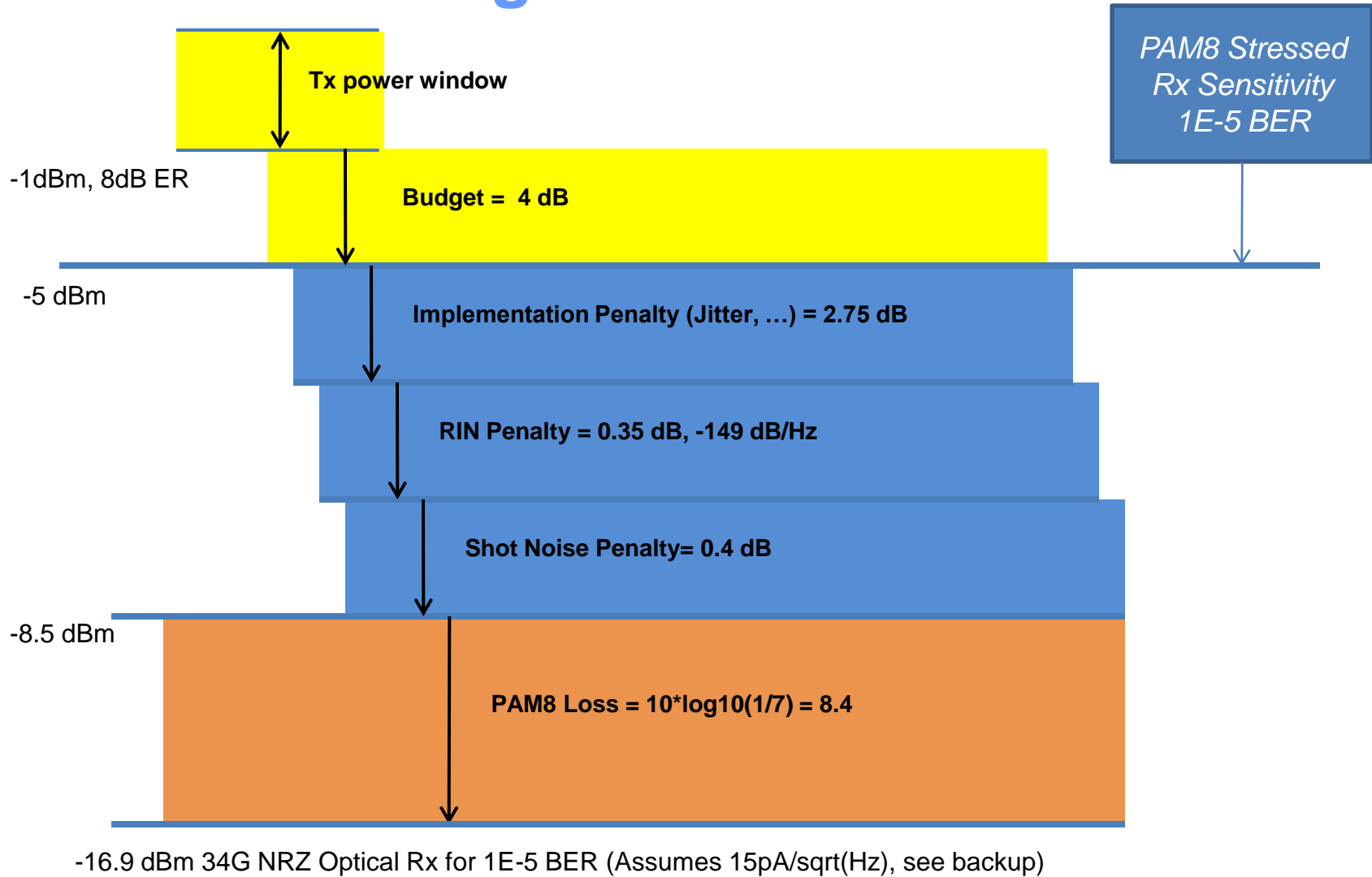
<sup>1</sup> Huang, Jia-Sheng; Su, Hui; He, Xiaoguang; Lei, Chun; Zendejaz, Ruby; Agarwal, Rajiv; Lomeli, Matt; Ye, Jinlin; Chin, Heng; Kim, Harqkyun; , "Ultra-high power, low RIN and narrow linewidth lasers for C-band DWDM +100km fiber optic link," Photonics Conference , 2011 IEEE , vol., no., pp.212-213, 9-13 Oct. 2011

# PAM8 Rx SNR breakdown



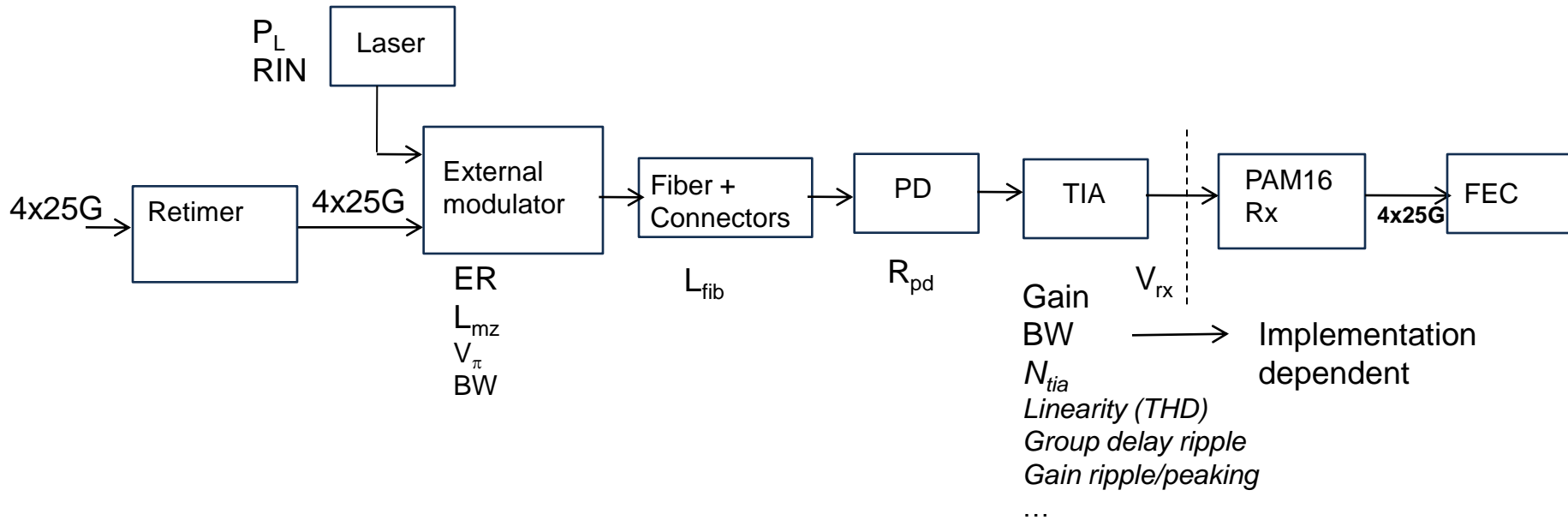
- Rx thermal noise dominates RIN & Shot noise

# PAM8 Link Budget



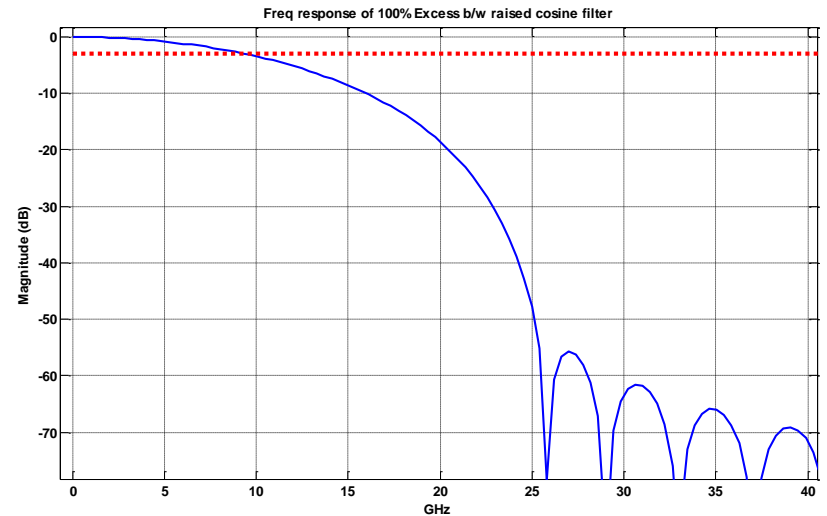
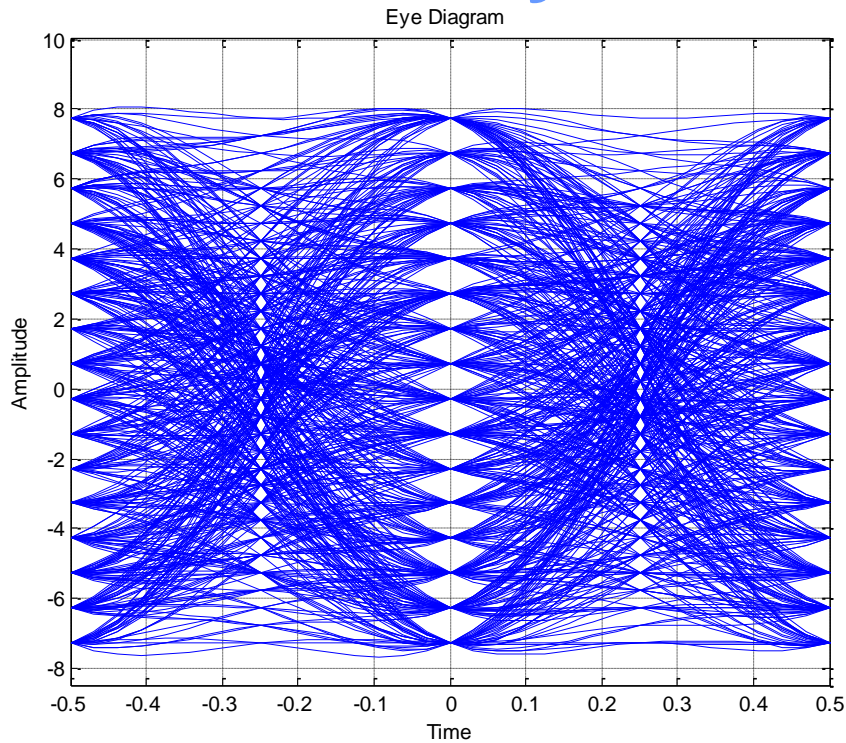
Simply a reference sensitivity of an NRZ signal at 34G

# PAM16 System Model

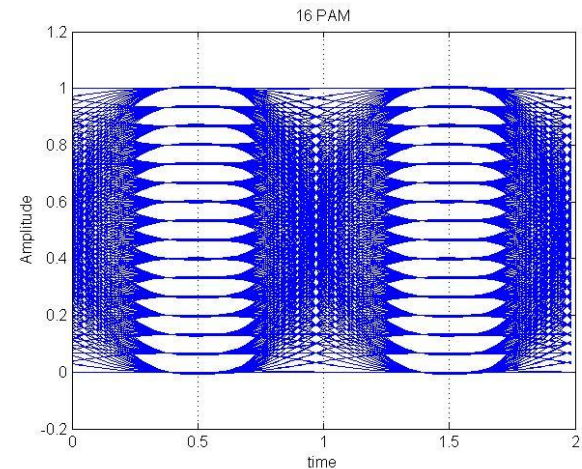


- Tx includes a 4:4 Retimer inside the module
  - Converts 4x25.78125 Gb/s to PAM16 at 25.78125 Gbaud
  - Single Laser externally modulated to 16 PAM
  - Baud Rate 25.78125 Gbaud, 4 bits/baud
  - Optionally a 28Gbaud provides for higher FEC coding gain
- A single PAM16 Rx CDR recovers the data and de-multiplexes to 4x25G
  - Host based FEC targets input BER of 1E-5, output BER 1E-15

# PAM16 Rx Eye

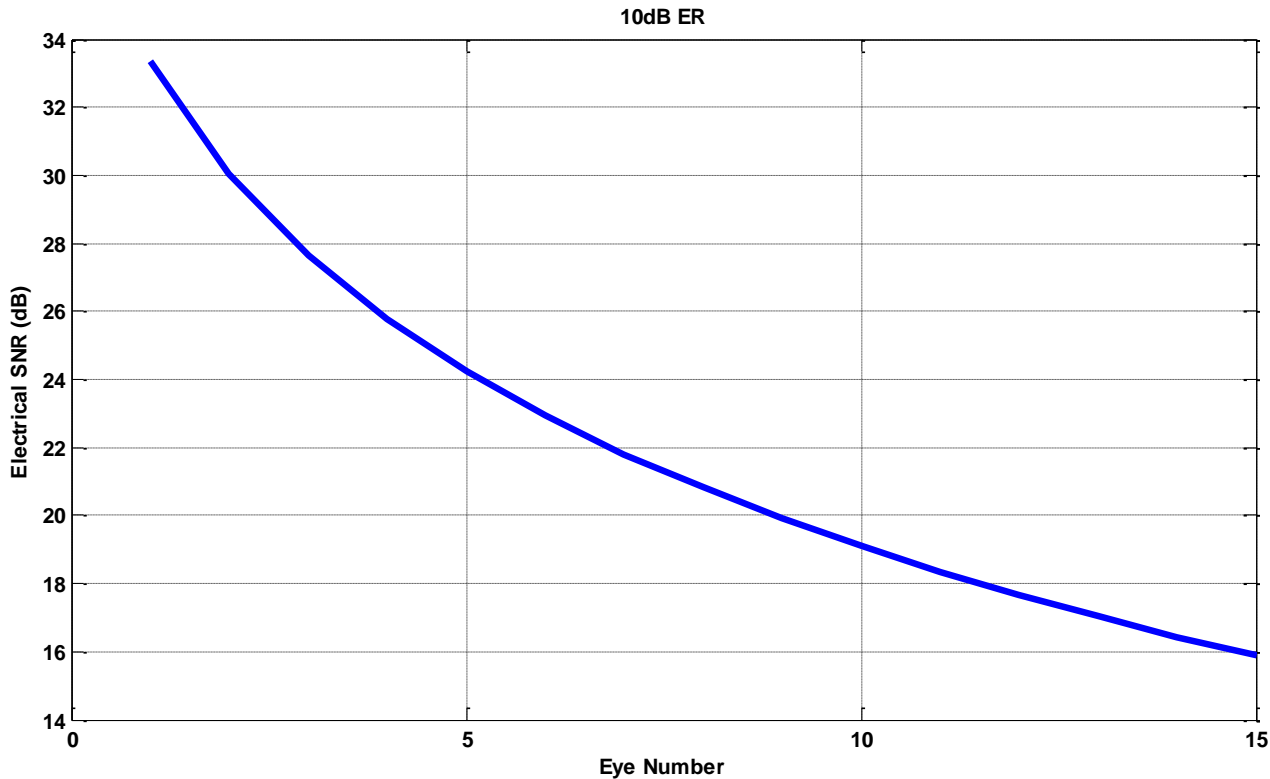


- 100% Excess Bandwidth – Ideal Raised cosine (3dB BW 9.4GHz)
- 11.76dB Optical penalty
- 0.2UI Horizontal Eye Opening. Wider bandwidth can tradeoff horizontal eye opening for reduced noise filtering. Example =>



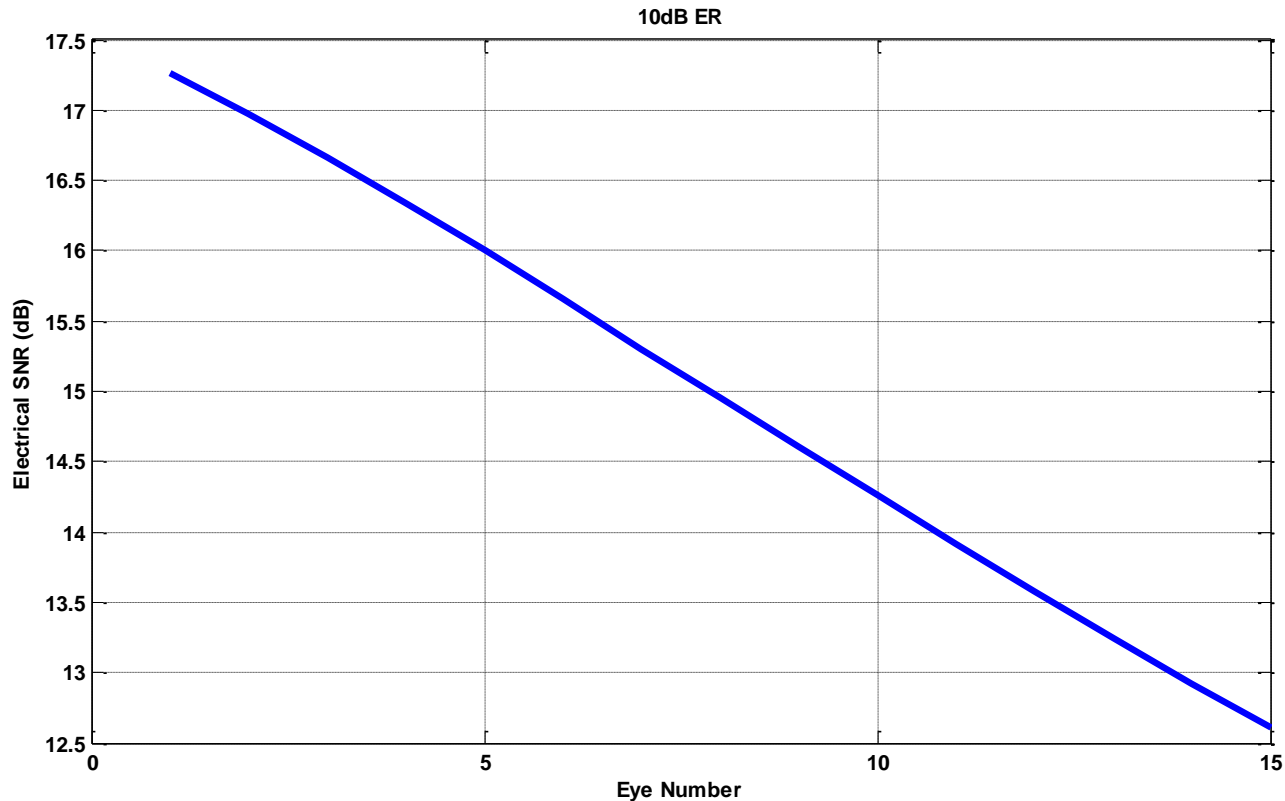
Example: 0.4 UI, Bessel Filter (5<sup>th</sup> Order), BW = 20GHz

# Laser RIN



- RIN @ -149 dB / Hz
- Noise is signal dependent. Wide variation of SNR
- Tx limited Electrical SNR varies from 33dB to 16dB  
Minimum SNR 16dB for outermost level

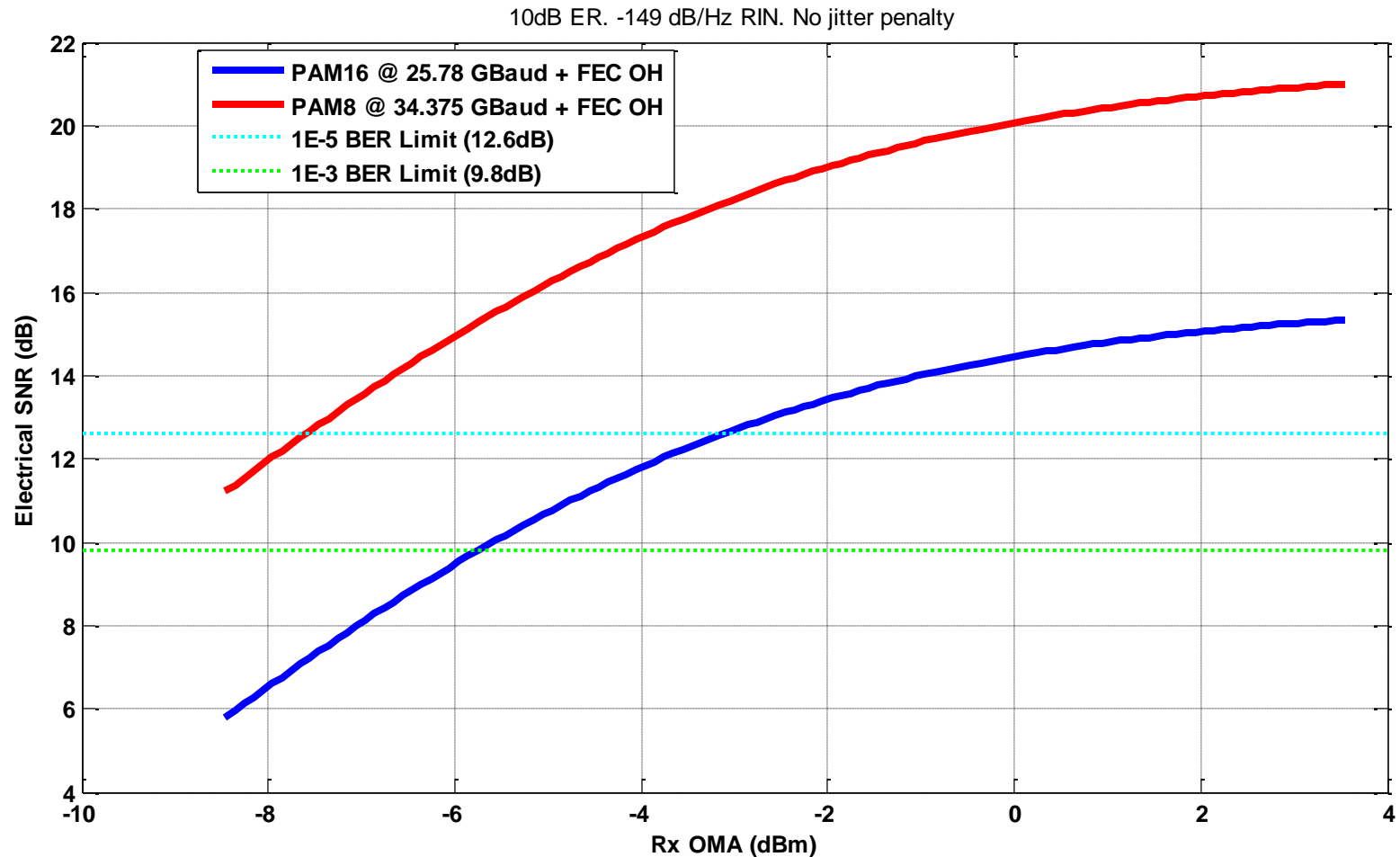
# PAM16 Rx SNR



- Equal spacing at Tx results in 4.5dB SNR variation
- Can we improve PAM16 SNR with unequal spacing at the Tx?

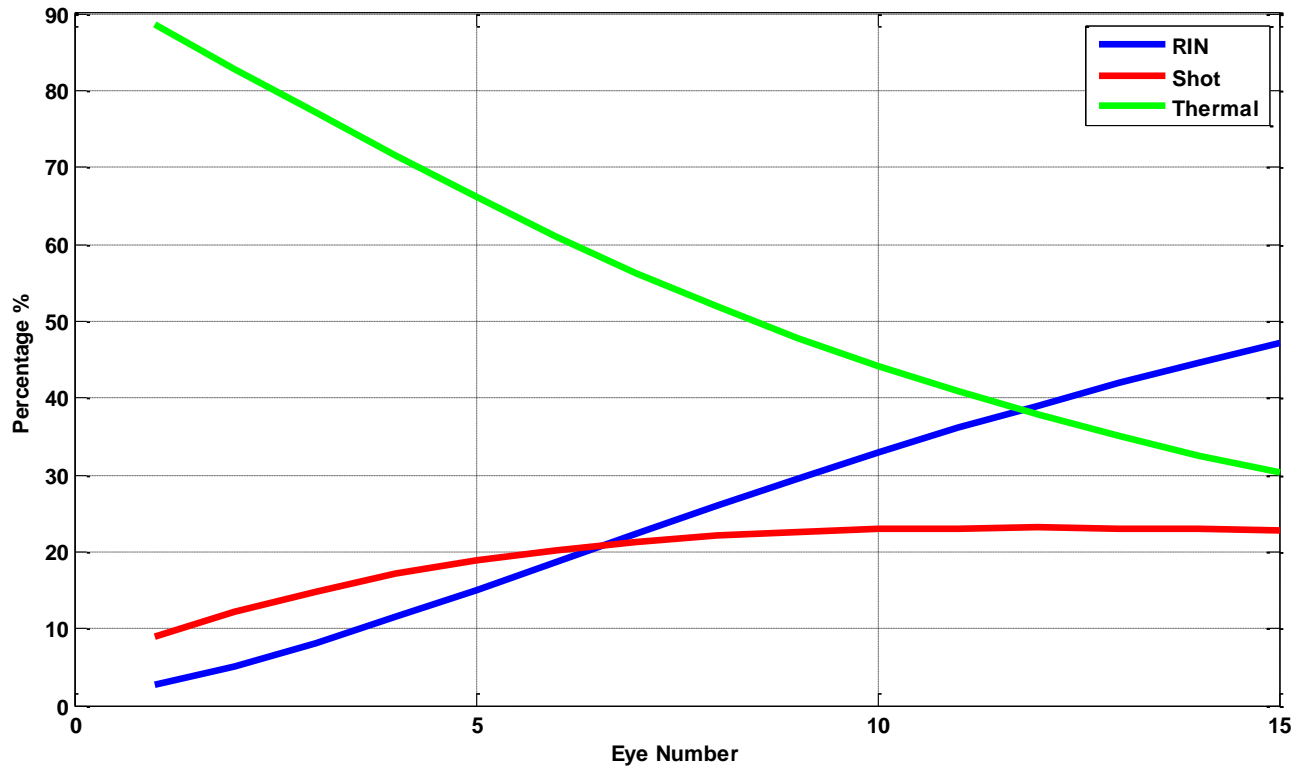


# PAM8 vs. PAM16



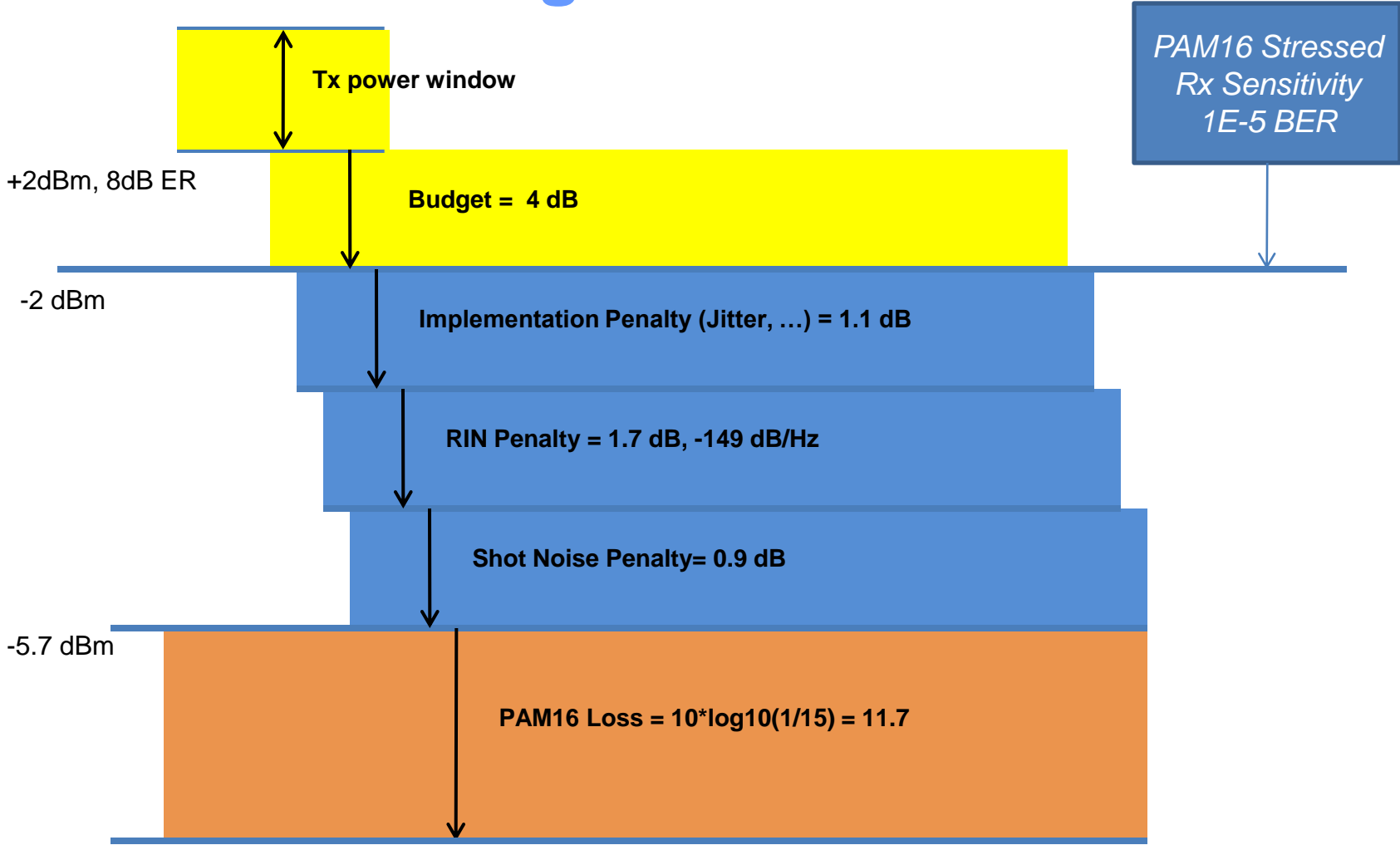
- PAM8 provides 4dB+ margin compared to PAM16
- Assumes equal spacing at PAM16 transmitter

# PAM16 Rx SNR breakdown



- RIN contributes more noise than shot or thermal effects at high levels

# PAM16 Link Budget



-16.4 dBm 25G NRZ Optical Rx for 1E-5 BER...

Simply a reference sensitivity of an NRZ signal at 25G

# Summary

- PAM solution for 100GE using a single laser was explored and is feasible
- Multiple example implementations of external modulators and multilevel CDR were shown
- Link budgets for PAM8 and PAM16 were investigated
- Link budgets look promising, requires further investigation

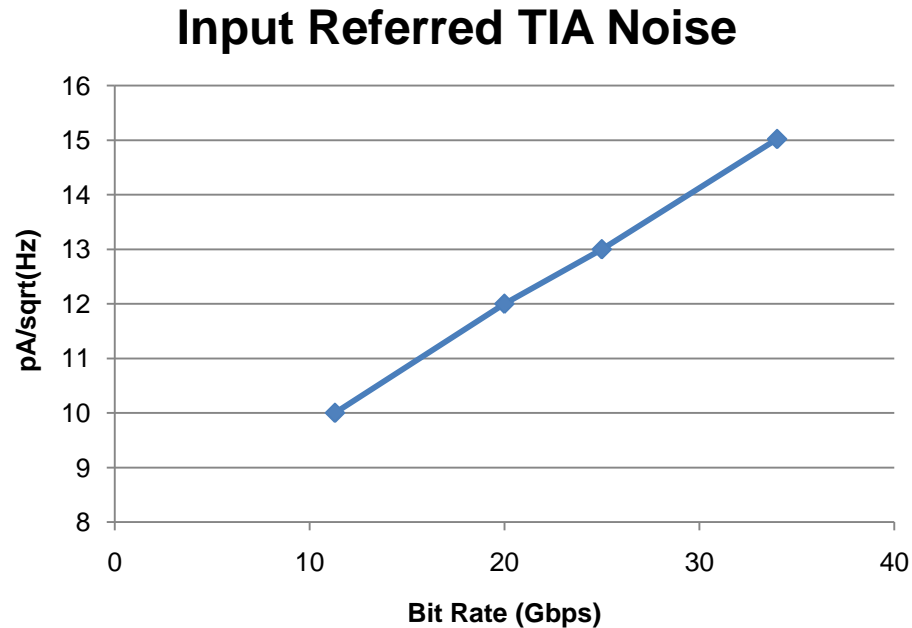
## Next steps

- Investigate unequal transmit level spacing for SNR improvement
- Bandwidth tradeoffs and Jitter
- Higher FEC coding gain via coded modulation for multilevel PAM
- Linearity
- Timing Error/Jitter sensitivity to FEC output BER

# Backup

# 34 GSymbol/sec TIA Noise

- TIA noise numbers are process and node dependent.



Gbps	pA/sqrt(Hz)	Reference
11.3	10	TI part <a href="http://www.ti.com/lit/ds/symlink/onet8511t.pdf">http://www.ti.com/lit/ds/symlink/onet8511t.pdf</a>
20	12	Schmid R., et al, "20 Gbit/s Transimpedance preamplifier and modulator driver in SiGe bipolar technology", Electronic Letters, June 1997
25	13	Chris Cole, "Technical & Economic Feasibility of 40km SMF 100GE Transceivers", IEEE 802.3 Higher Speed Study Group, May 2007, <a href="http://ieee802.org/3/hssg/public/may07/cole_01_0507.pdf">http://ieee802.org/3/hssg/public/may07/cole_01_0507.pdf</a>
34	15.0	Extrapolated value