Measurements Results of 25.78 GBd VCSEL Over OM3 with and without Equalization

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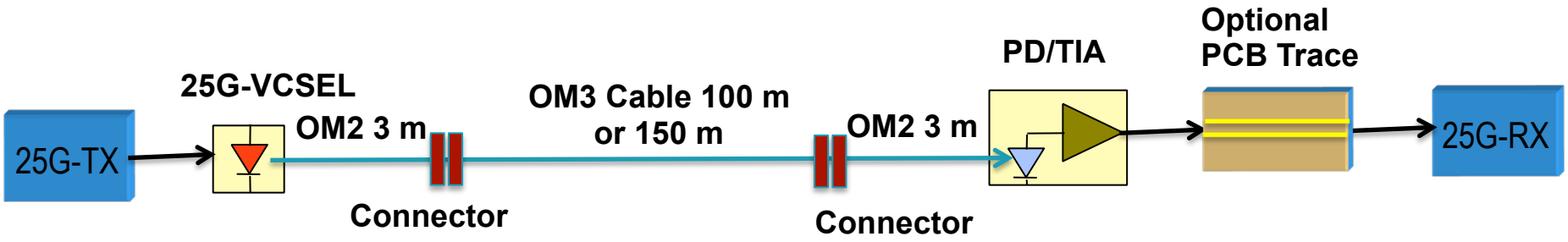
Overview

- Test setup
- Measured and simulated eye diagrams
- Calculated WDP and pulse response
- BER plot
- Example FFE implementation

Authors are specially thankful to Jim Tatum and Jonathan King of Finisar for their contributions and providing VCSELs samples for this work.

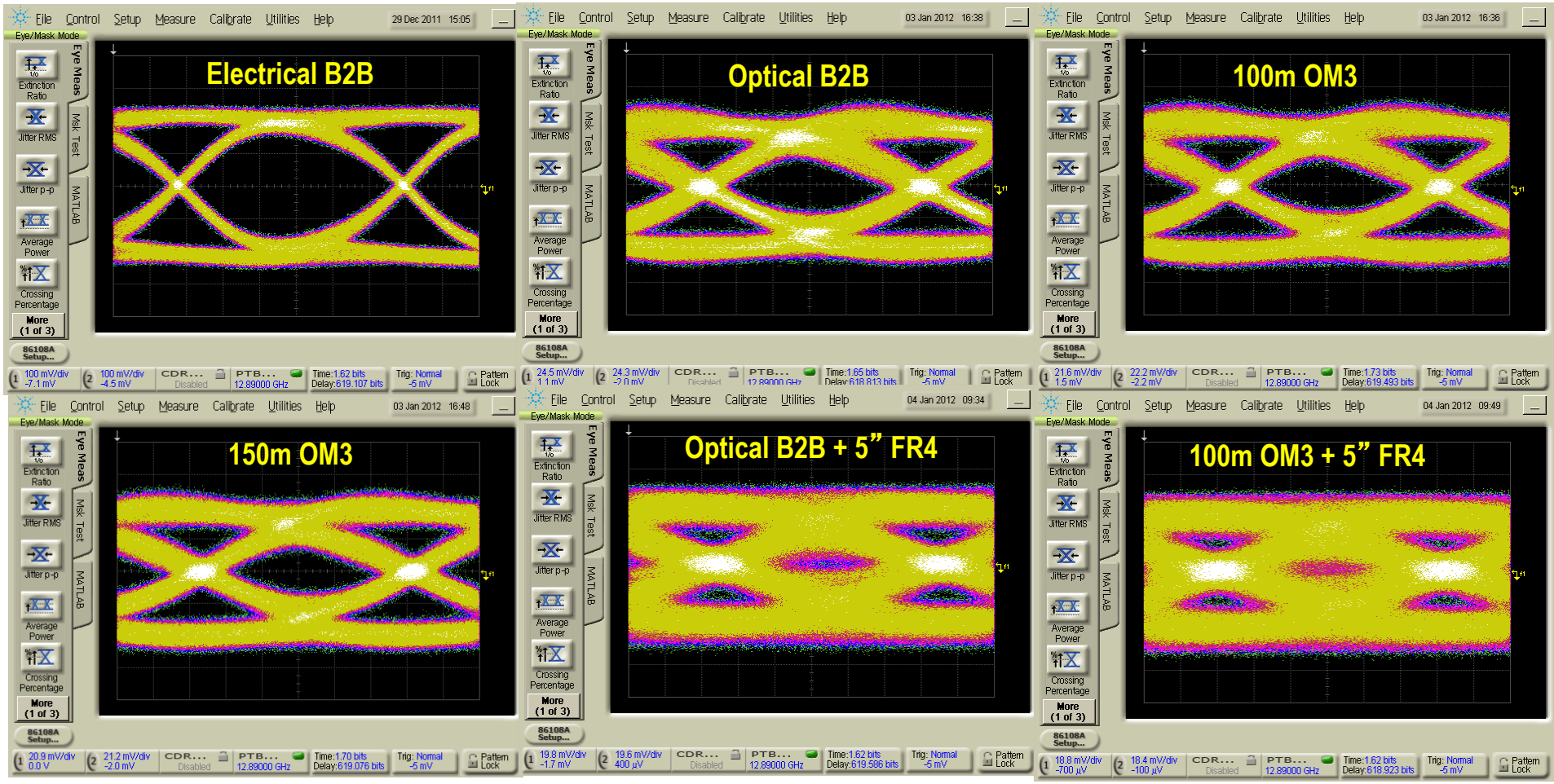
Test Setup

- **The VCSEL was driven directly from a 25.78 GBd SerDes test chip**
  - Laser was biased through bias-T
  - VCSEL was driven singled from the driver with amplitude of 250 mV
  - See little benefit of increasing de-emphasis beyond compensating for the test board
  - Laser test and reliability results are being presented at Photonics West this week by Finisar
- **The VCSEL die output was collimated with NA=0.47 lens then focused with NA=0.23 lens into an 50/120 um OM2 fiber patch cord as shown below**
- **VCSEL was biased at 5 mA with an extinction ration of 5 dB**
- **Optical receiver had a BW of 15.5 GHz, differential conversion gain of ~150 V/W, and a sensitivity of -5.5 dBm**



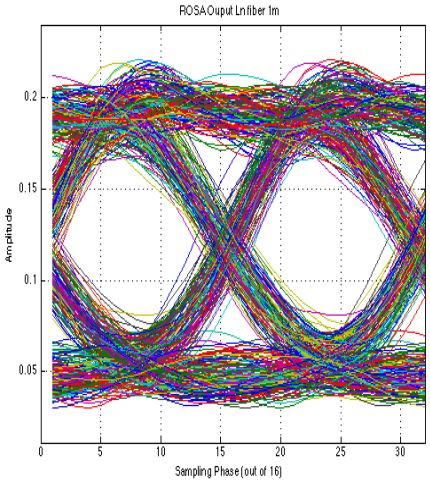
PRBS31 Eye Diagram at 25.78 GBd

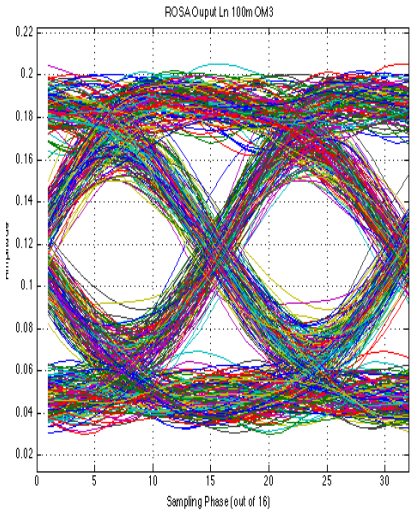
- VCSEL bias current was 5mA with ER ~ 5dB

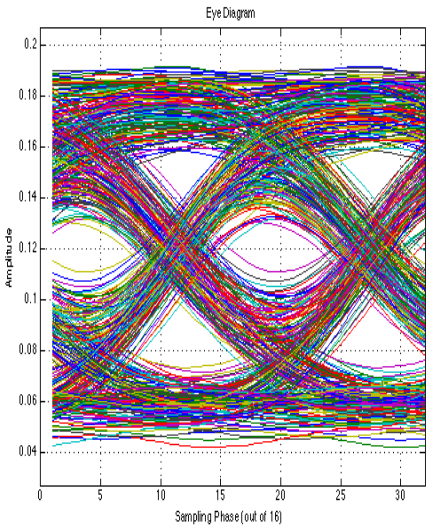


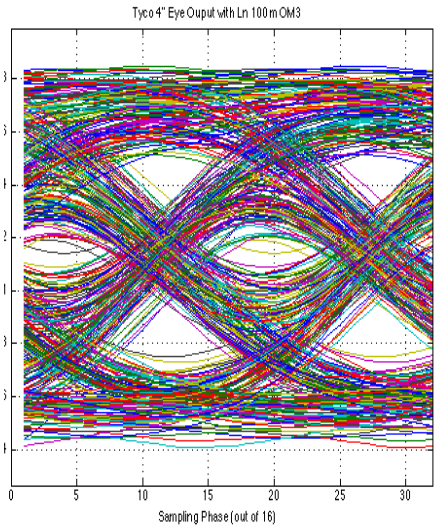
Rate Equation VCSEL Results

- **Results shown respectively for full detail see ghiasi_02_0112**
  - Optical B2B
  - Optical 100 m OM3
  - Optical B2B after 7 dB channel at TP5
  - Optical 100 m OM3 and after 7 dB channel at TP5



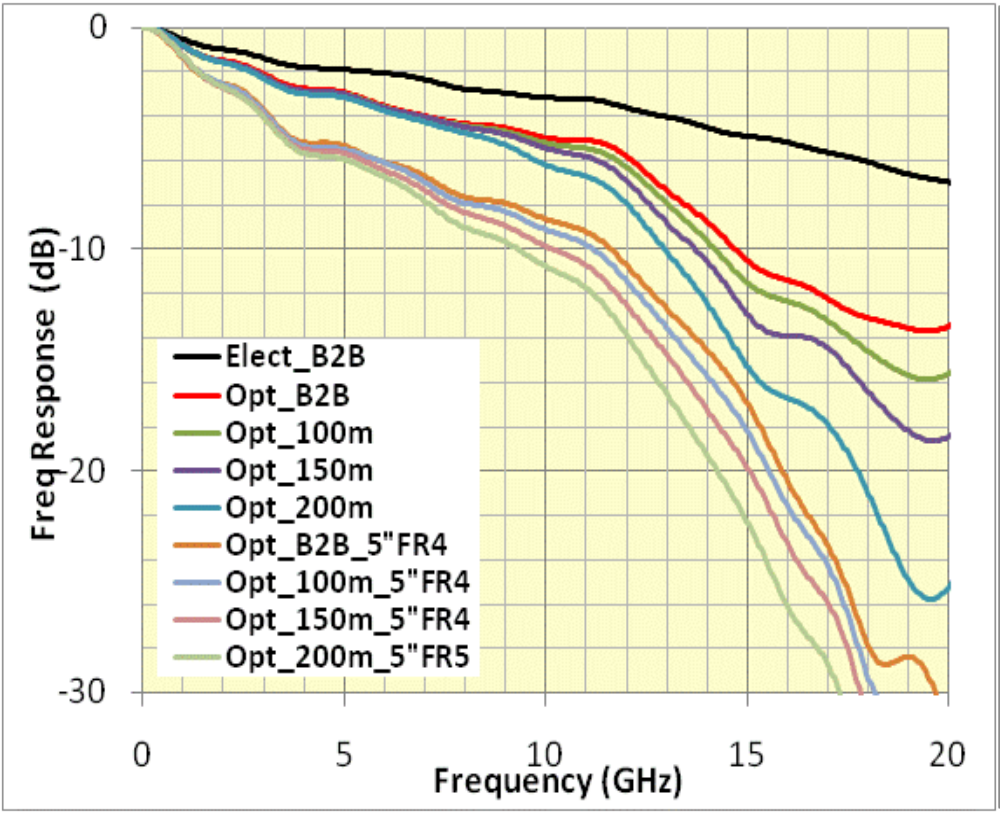


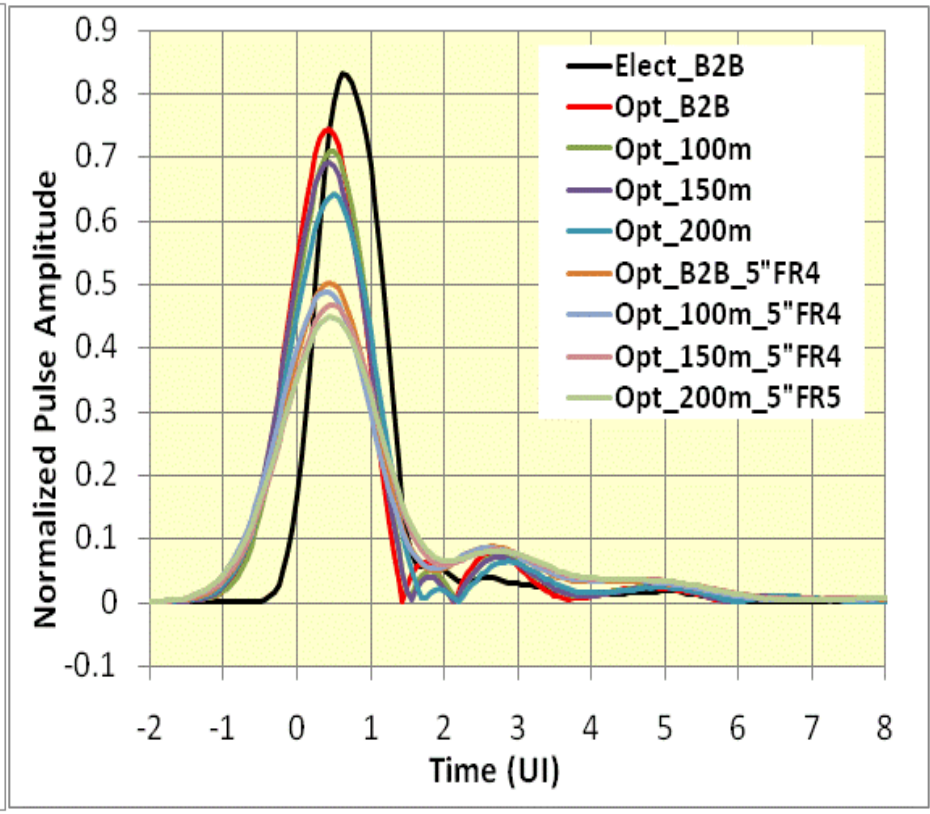




Frequency & Pulse Response

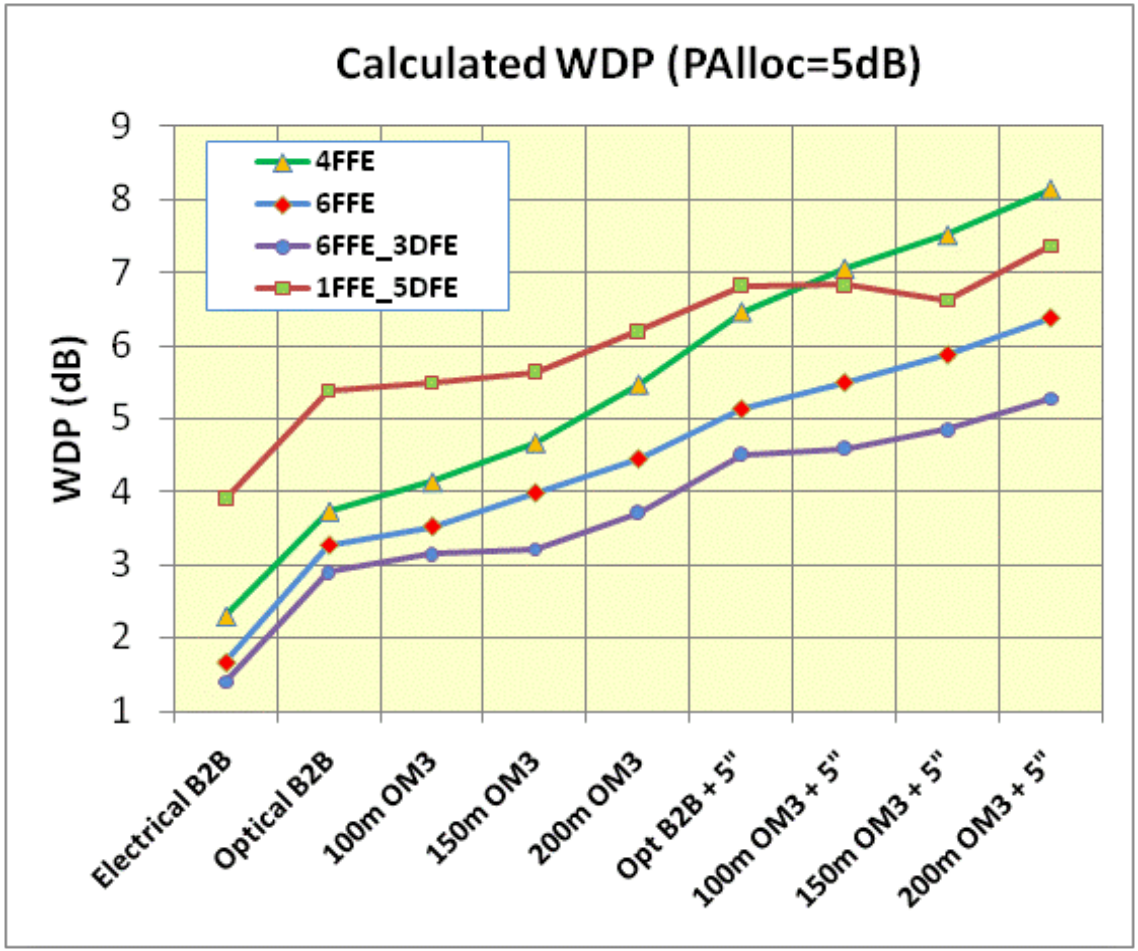
- Calculated from PRBS9 pattern
- 5” FR4 ~ 6.5dB loss at Nyquist





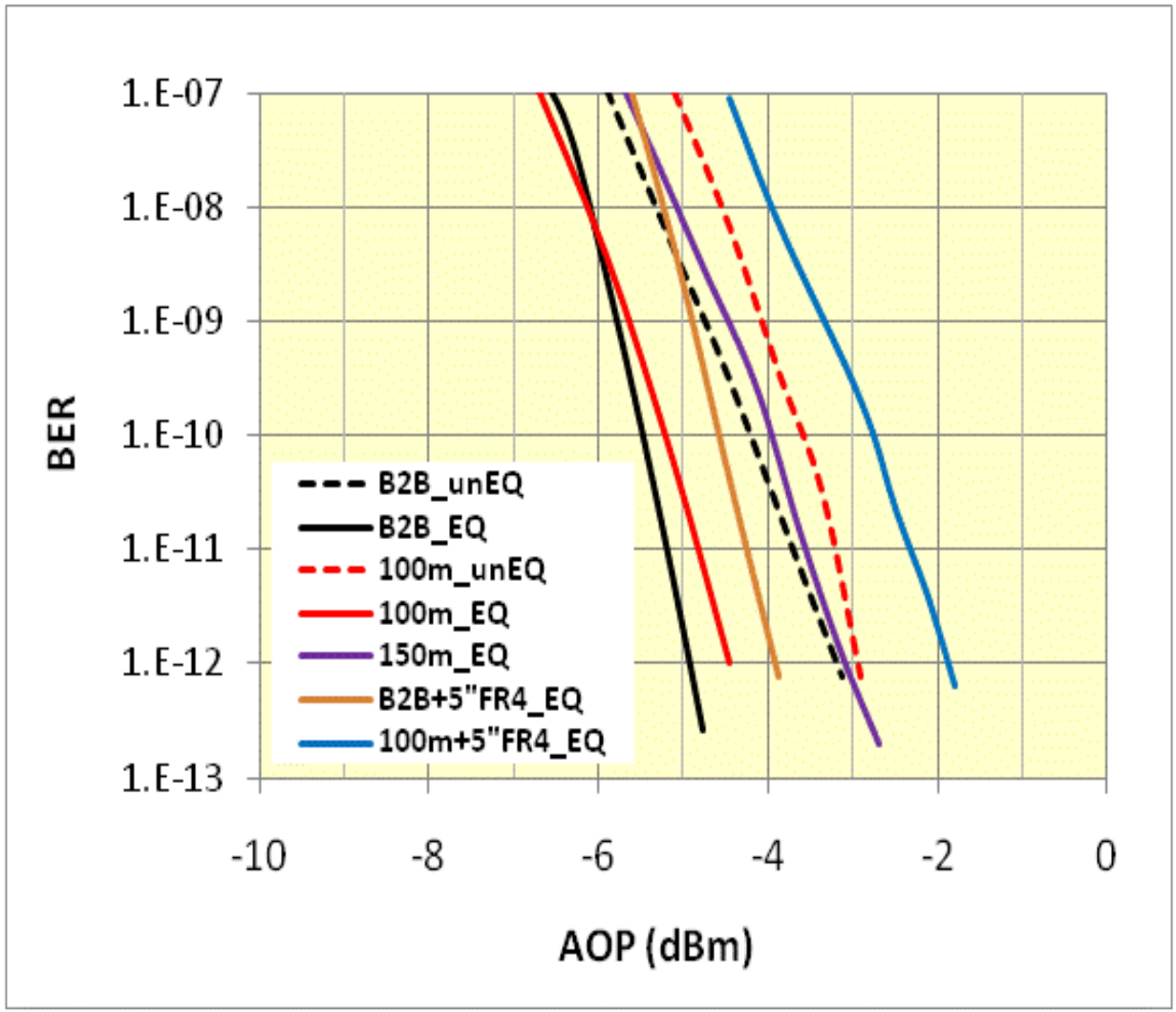
Calculated WDP for Measured Waveforms

- Calculated with SFF8431's xWDP code, Palloc set to 5dB
- Large WDP jump seen from:
  - Electrical to optical B2B
  - Addition of 5" FR4
  - Longer than 150m OM3



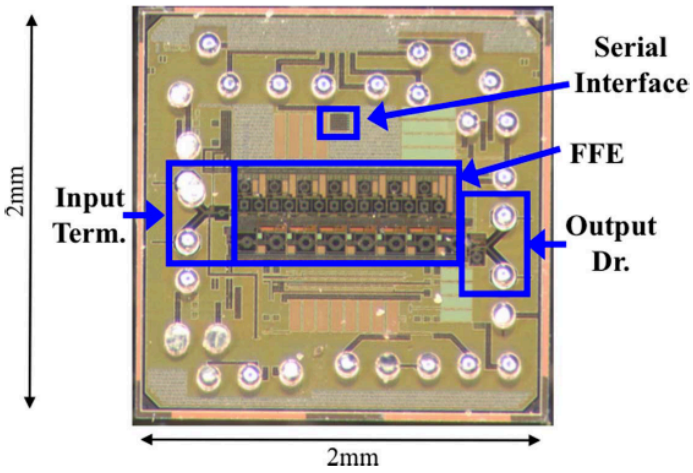
BER for Several Test Cases

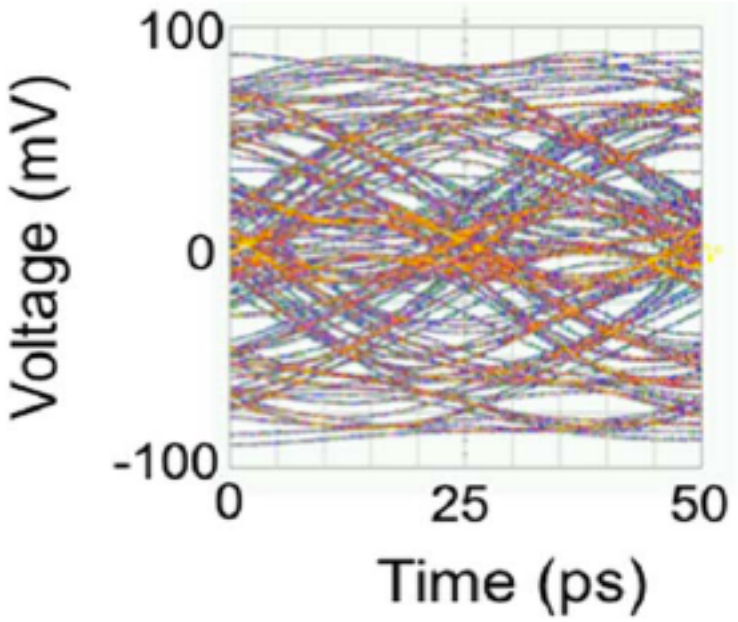
- PRBS31 pattern
- Tx De-emphasis is not set
- CTLE set to compensate for 5” FR4, not used for fiber only
- Equalizer is 1 tap DFE which improves B2B sensitivity by ~ 2dB
- 150m OM3 long term BER → 99.98% EF conf level at 1E-15
- Error floor for 100m OM3 + 5” FR4 ~ 1.1E-14
- Error floor for 200m OM3 + 5” FR4 (not shown) ~ 1.5E-9

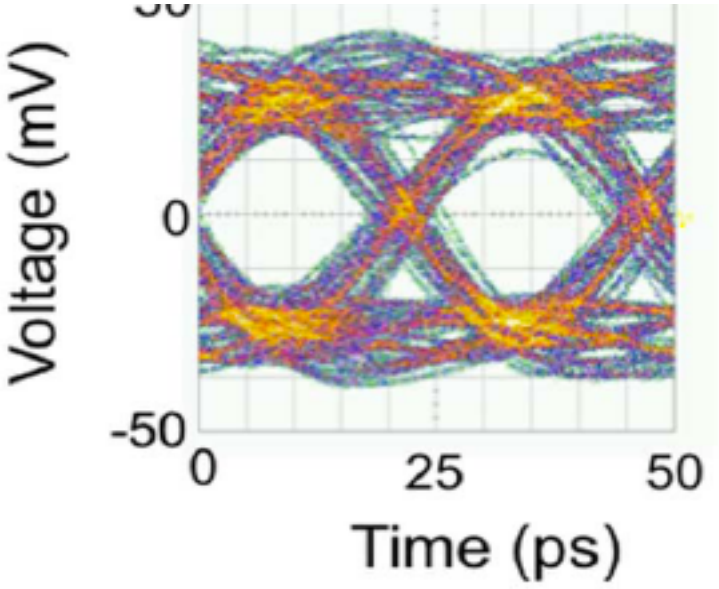


Broadcom/UCI* 40 GBd 7 T/2 FFE

- Chip implemented in standard 65 nm CMOS
- Eye Diagrams at 40 GBd before and after equalization
- PD just 80 mW!
- In 28 nm @25.78 PD <40 mW.







* Afshin Momtaz and Mike Green, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 3, MARCH 2010

Summary

- **The 25.78 GBd test chip receiver which has both CTLE and 1-DFE was used as the receiver**
  - The CTLE provided very little benefit at ROSA output for fiber reach up to 100 m
  - Adding 6.5 dB PCB trace loss only added 1 dB optical penalty
  - When the DFE was turned on, 2 dBo was gained and the link BER was <1E-15 @ 99.98 confidence based on the link operatizing error free for 4 days!
- **B2B Results are better with 5" PCB and EQ with just a modest 1-tap DFE than no EQ at ROSA output!**
  - More optimum EQ such as 6-T/2 would reduce the penalty by additional 2 dBo for the case of retimed
  - More optimum EQ such as 6-T/2+3-DFE estimated to reduce the penalty by additional 2 dBo in case of unretimed
- **In the retime applications adding 6-T/2 FFE to the module in 28 nm CMOS will add <40 mW/ch**
- **In the unretime application the dominant power dissipation will be due to DFE which is needed to support Cu.**