Power and Complexity of 100G-SR4 Implementations

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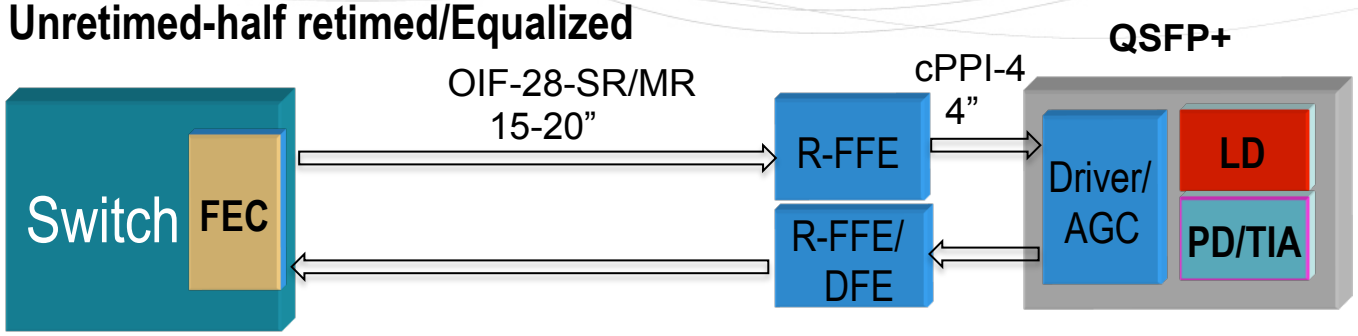
Implication of the Retimed Interface

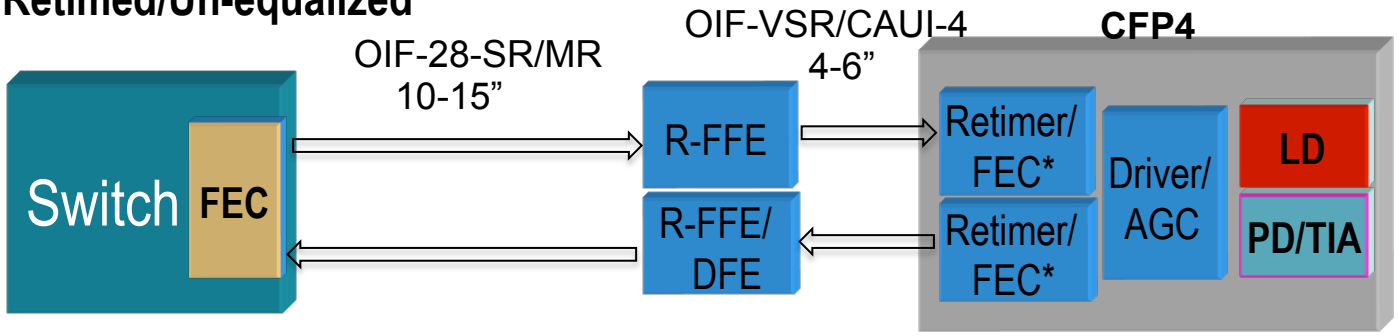
- 100G-SR4 link performance is dominated by the VCSEL response with about 4 dBo of penalty if no equalizer is used
- The next largest source of penalty is the FR4 PCB trace in case of unretimed interface with about 1.5 dBo of penalty
- Operating the link from B2B to 100 m only adds just ~ 1dBo of penalty
- A retimed interface with FEC will be able to support 50-70 m reach but the this implementation will be:
  - Higher cost
  - Higher power
  - Larger size
  - Higher latency
- The key advantages of retimed interface are the simplified interface and low risk interface.

Common 100G-nR4 Implementations

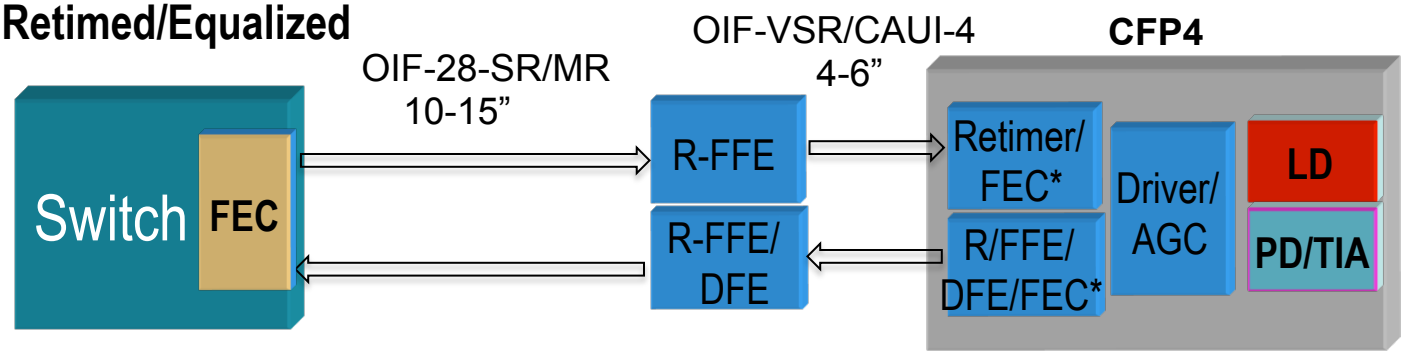
- **Unretimed-half retimed/Equalized**



- **Retimed/Un-equalized**



- **Retimed/Equalized**



- In some retimed application if FEC is required but the host does not support it then module must
- Include FEC which will double the retime PD and not considered in power calculations.

PCB Reach Various Standards

- VSR interfaced in OIF has 10 dB end to end loss budget
- Assuming CAUI-4 has the same loss budget as OIF VSR it means in most applications a Gearbox or 4x25G retimer is placed outside the module
- cPPI-4 tries to take advantage of the retimer in close proximity to the module instead of doubling up retiemrs!

Host Trace Length *	Total Loss (dB)	Host Loss(dB)	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal PCB Loss at 28G/in	N/A	N/A	2.0	1.5	1.2	0.9
OIF 28G-LR with two connector	25.5	23.1	11.6	15.4	19.3	25.7
OIF 28G-SR with one connector & HCB	15.4	12.5	6.3	8.3	10.4	13.9
OIF 28G-VSR with one connector & HCB	10	7.3	3.7	4.9	6.1	8.1
cPPI-4 with one connector & HCB	7	4.1	2.1	2.7	3.4	4.6

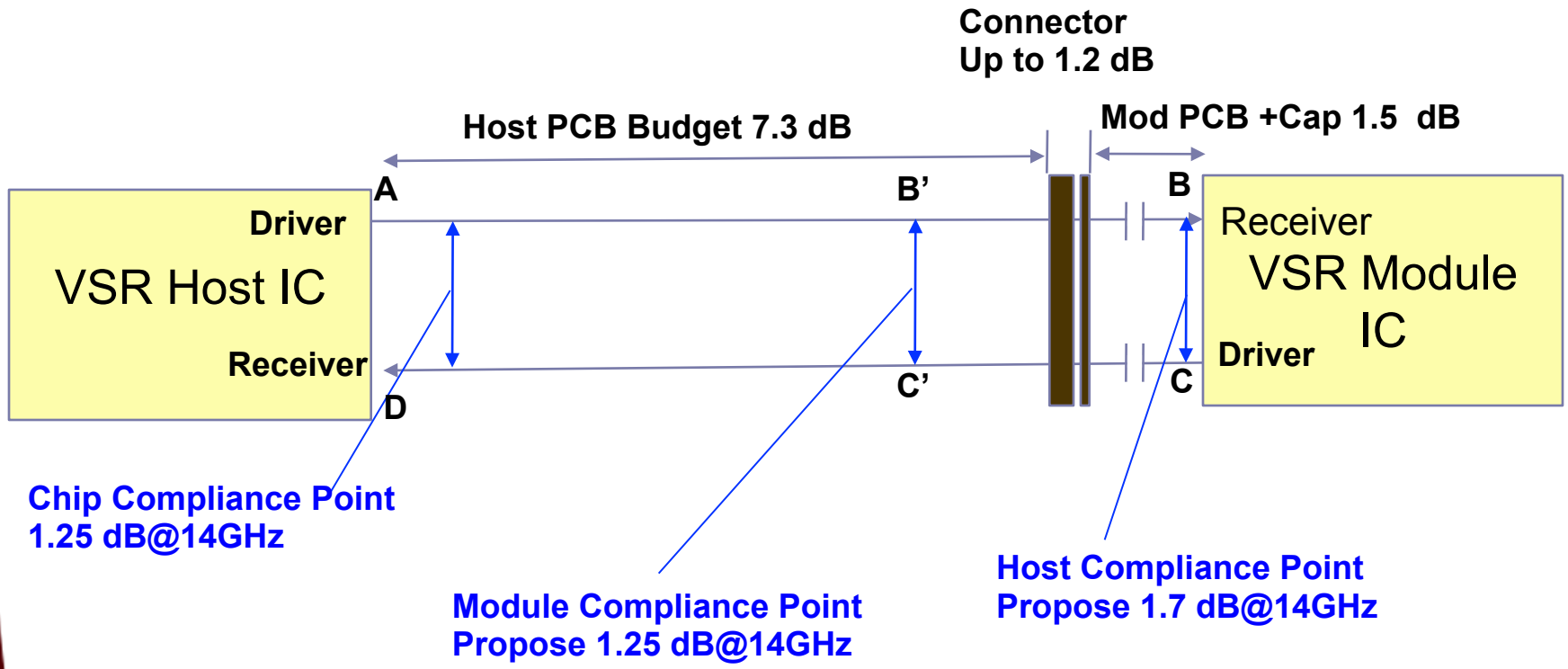
- Assumes connector loss is 1.2 dB and HCB loss is 1.7 dB this table has not allocated loss for any vias.
- Losses for N4000-13SI and Megtron 6 are in line with 100GCU PCB tool assuming low surface finish http://www.ieee802.org/3/bj/public/tools/kochuparambil_01_1211.pdf

Highlight of OIF 28G-VSR

- Host transmitter assumes 3 tap FFE with pre and post
- Transmit amplitude of 600 mV
- Host output measured at HCB output with reference CTLE and must meet certain vertical and horizontal opening
- Module transmitter assumes it will deliver certain vertical and horizontal opening at MCB output
- Assume sensitivity at chip ball is 100 mV when measured with software CTLE
- There is no back channel
  - Host will optimize far end eye through reference CTLE by adjusting pre and post
  - The module will utilize its pre/post or peaking filter and faster rise time to deliver min vertical and horizontal opening at TP4 (MCB Output)
- Specification assumes MCB and HCB similar to 802.3ba
- Good starting point for CAUI-4.

OIF 28G-VSR Architecture and Reference Points

- Follows 802.3 CL83B (CAUI)



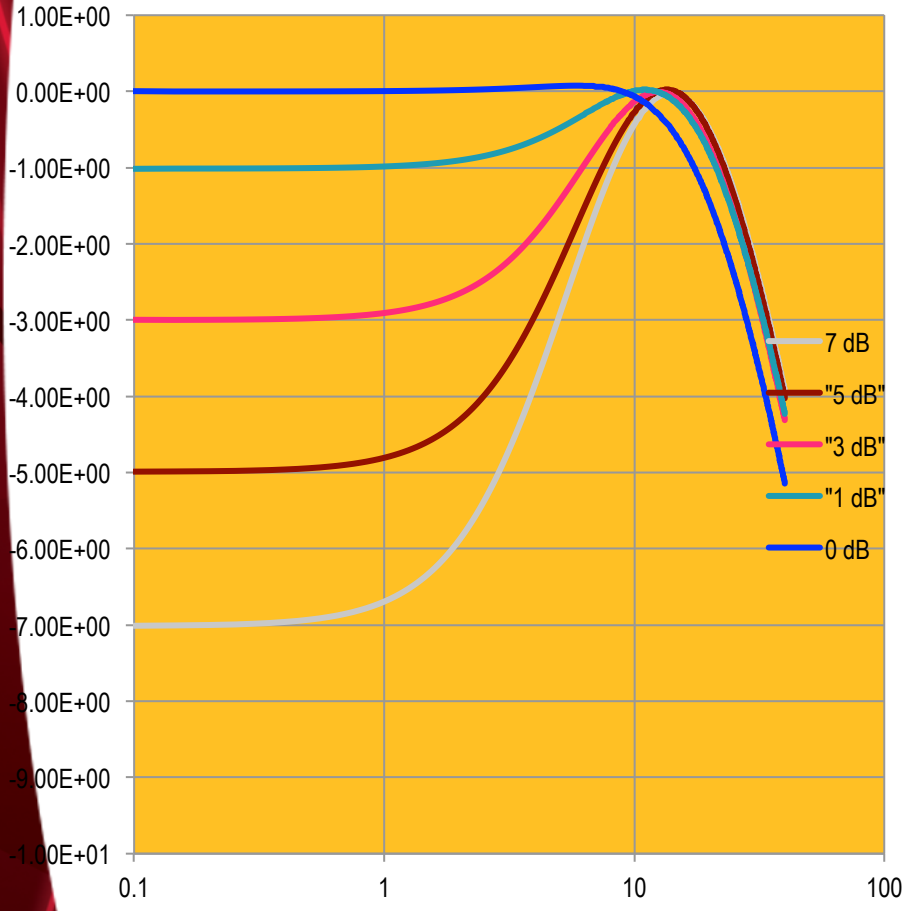
VSR Channel Loss Budget Table

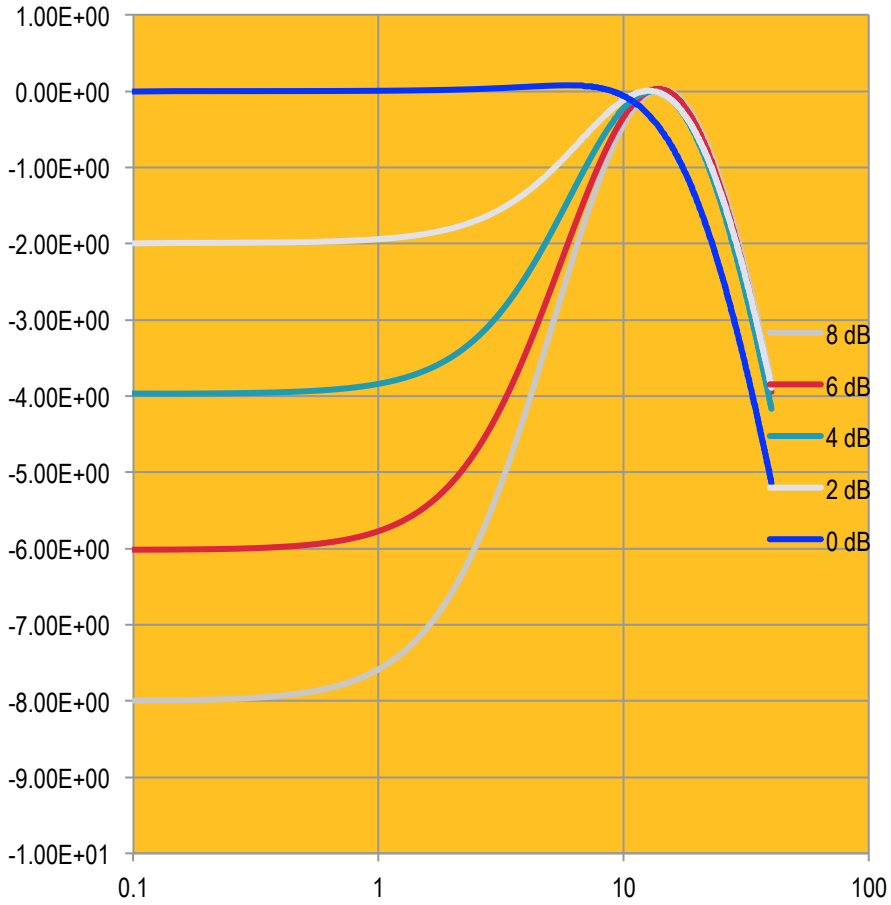
- Assumes 10 dB loss from host IC balls to module IC balls

Traces	FR4-6	N4000-13	N4000-13SI	Megtron 6
Loss at 14 GHz /in	2.0	1.5	1.2	0.9
Worst Case Connector loss at 14 GHz	1.2			
Loss allocation for 2 Vias in the channel	0.5			
DC Block	0.5			
Max Module PCB Loss	1.7			
Host PCB Trace Length Assuming 10 dB Loss Budget	3.0500	4.0667	5.0833	6.7778

OIF VSR Reference Receiver

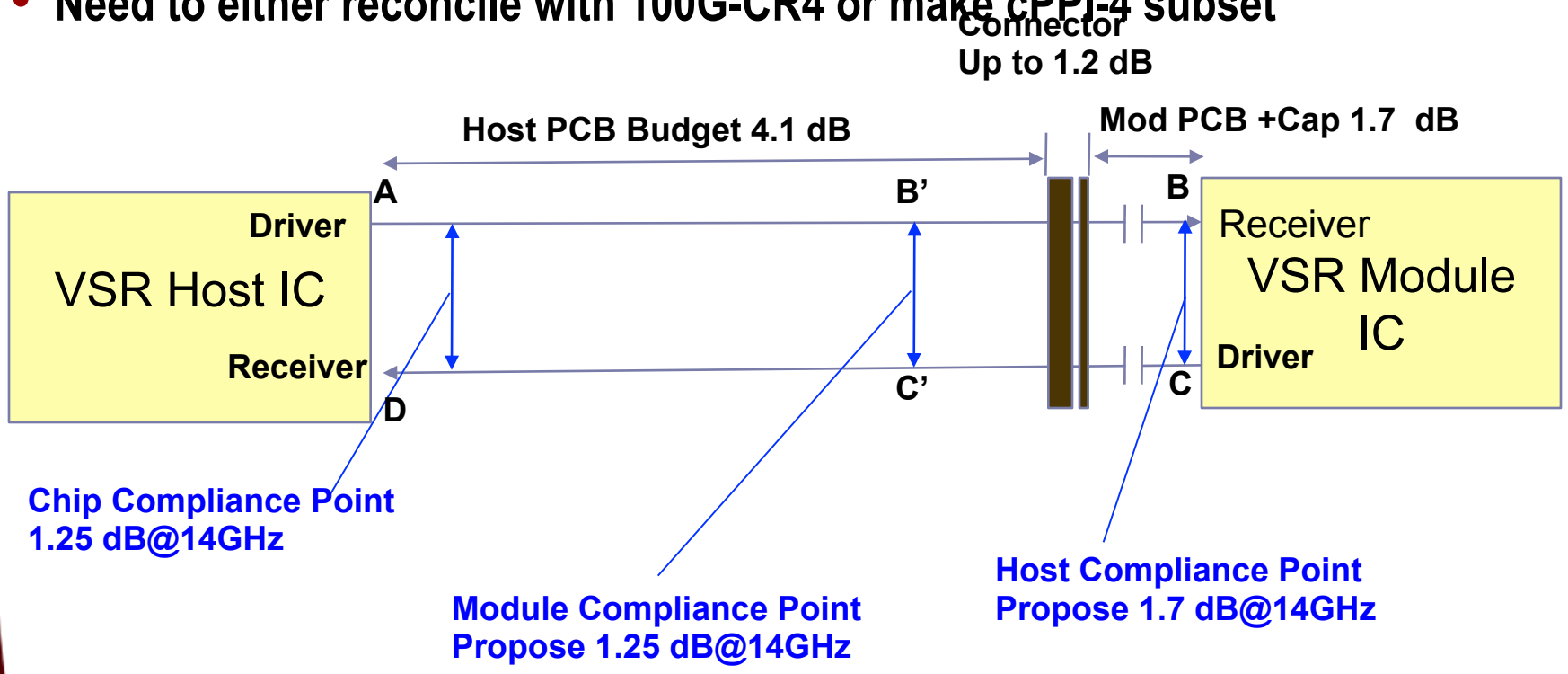
- **Is based on a family of 0-8 dB CTLE having two poles and one zero**
  - Will also submit the same model to be posted under model/channel area





cPPI-4 Architecture and Reference Points

- Follows 802.3 CL86(nPPI) and CL85
- Need to either reconcile with 100G-CR4 or make cPPI-4 subset



cPPI-4 Proposed Channel Loss Budget

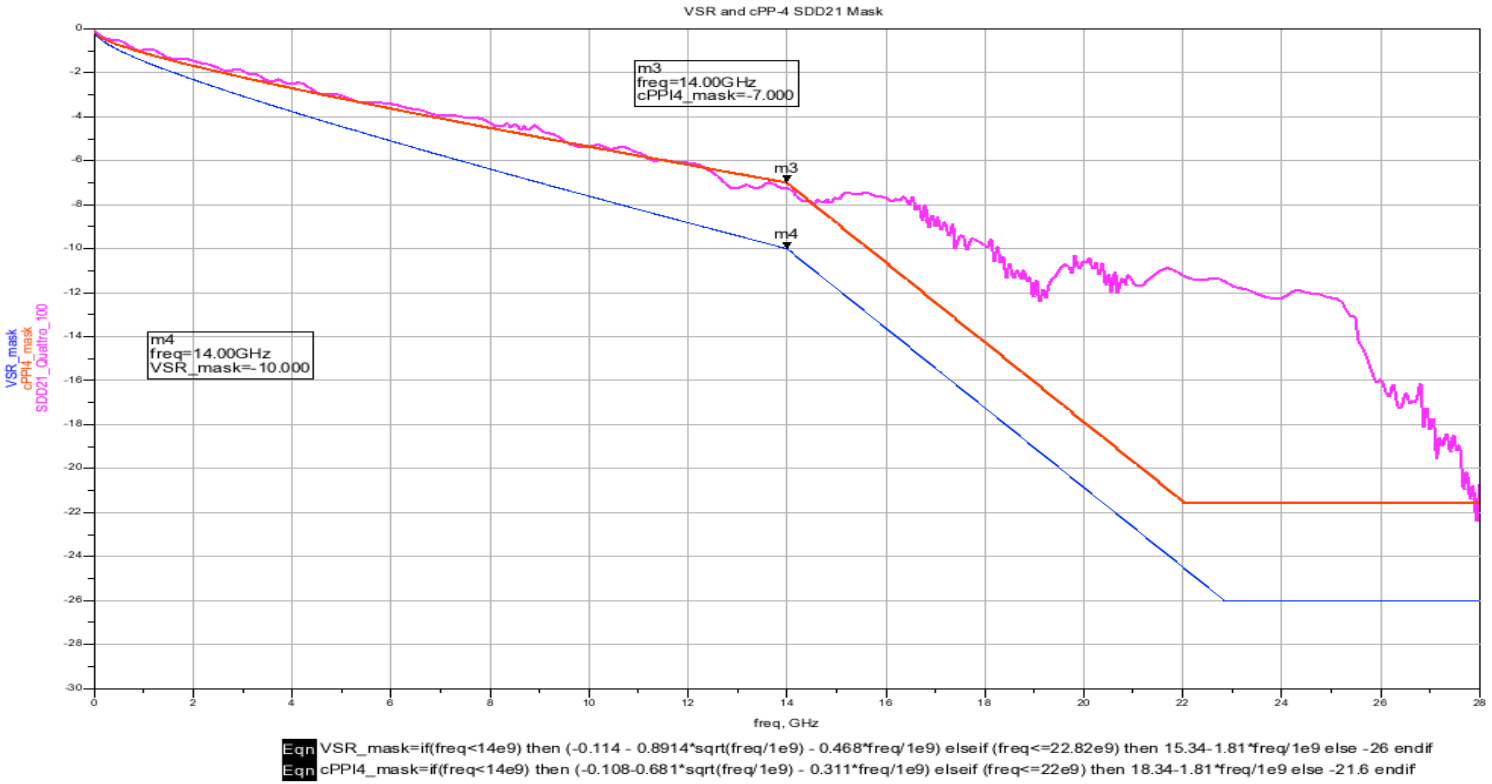
- Attach cPPI-4 with 7 dB loss budget can support unretimed optical PMDs as well as100GCU copper cables

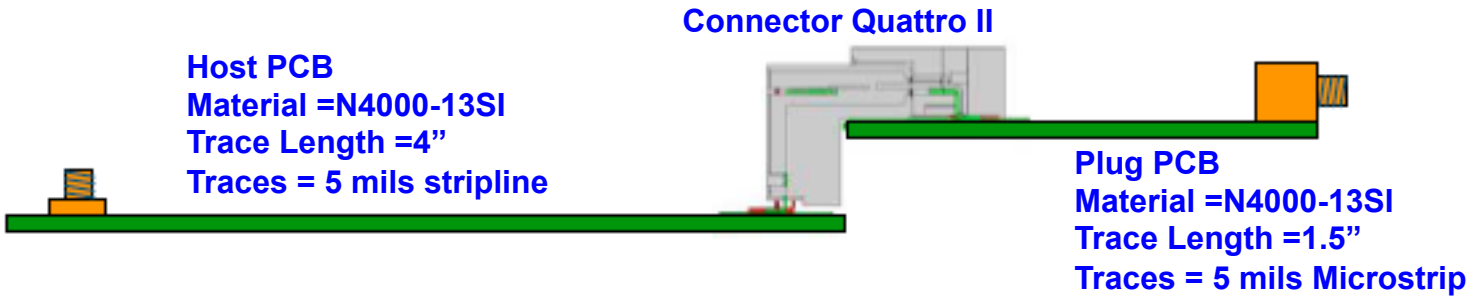
Traces	FR4-6	N4000-13	N4000-13SI	Megtron 6
Nominal Loss at 14 GHz /in	2	1.5	1.2	0.9
Connector loss at 14 GHz*	1.2			
Loss allocation for 2 Vias in the channel	0.5			
Max Module PCB Loss/DC Blocks at 14GHz*	1.7			
PCB Trace Length Assuming 7 dB Loss Budget	1.8000	2.4000	3.0000	4.0000

* For 100 GbE operation since the HCB and connector are specified for operation up to 28GBd there will be 0.2-0.3 dB unallocated margin.

cPPI-4 Channel Based on TE Quattro II

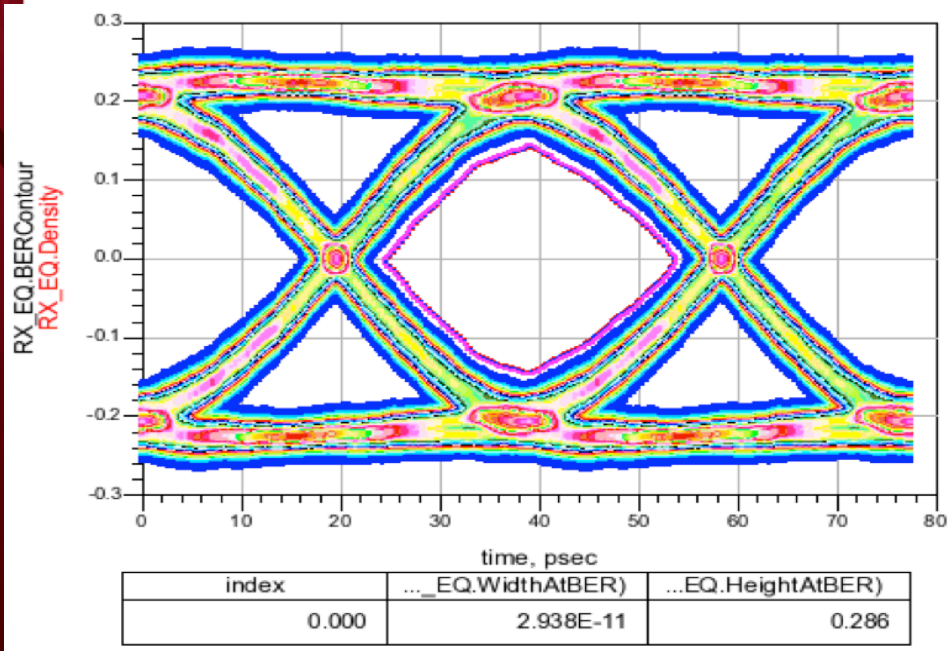
- VSR mask also shown



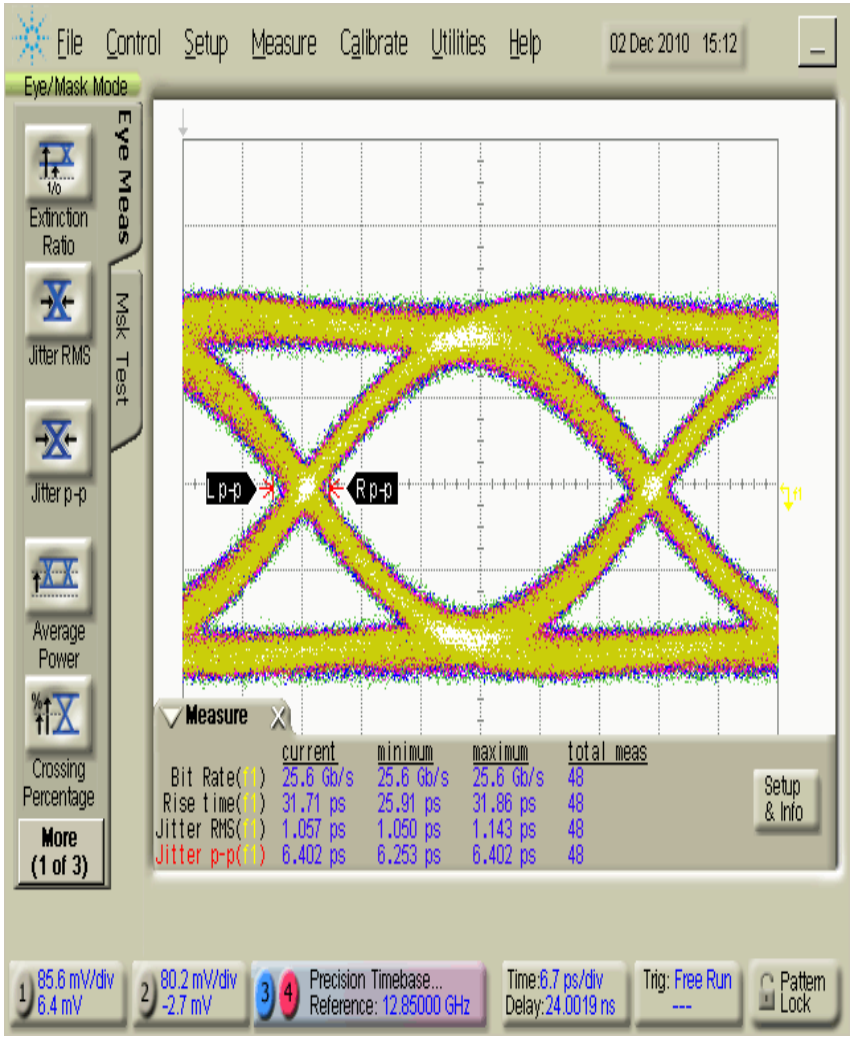


Far End Transmitter Eye

- **Simulated and measured eye for 4” Quattro II Channel at 25.7 GBd**
  - Channel loss 7.1 dB @14 GHz

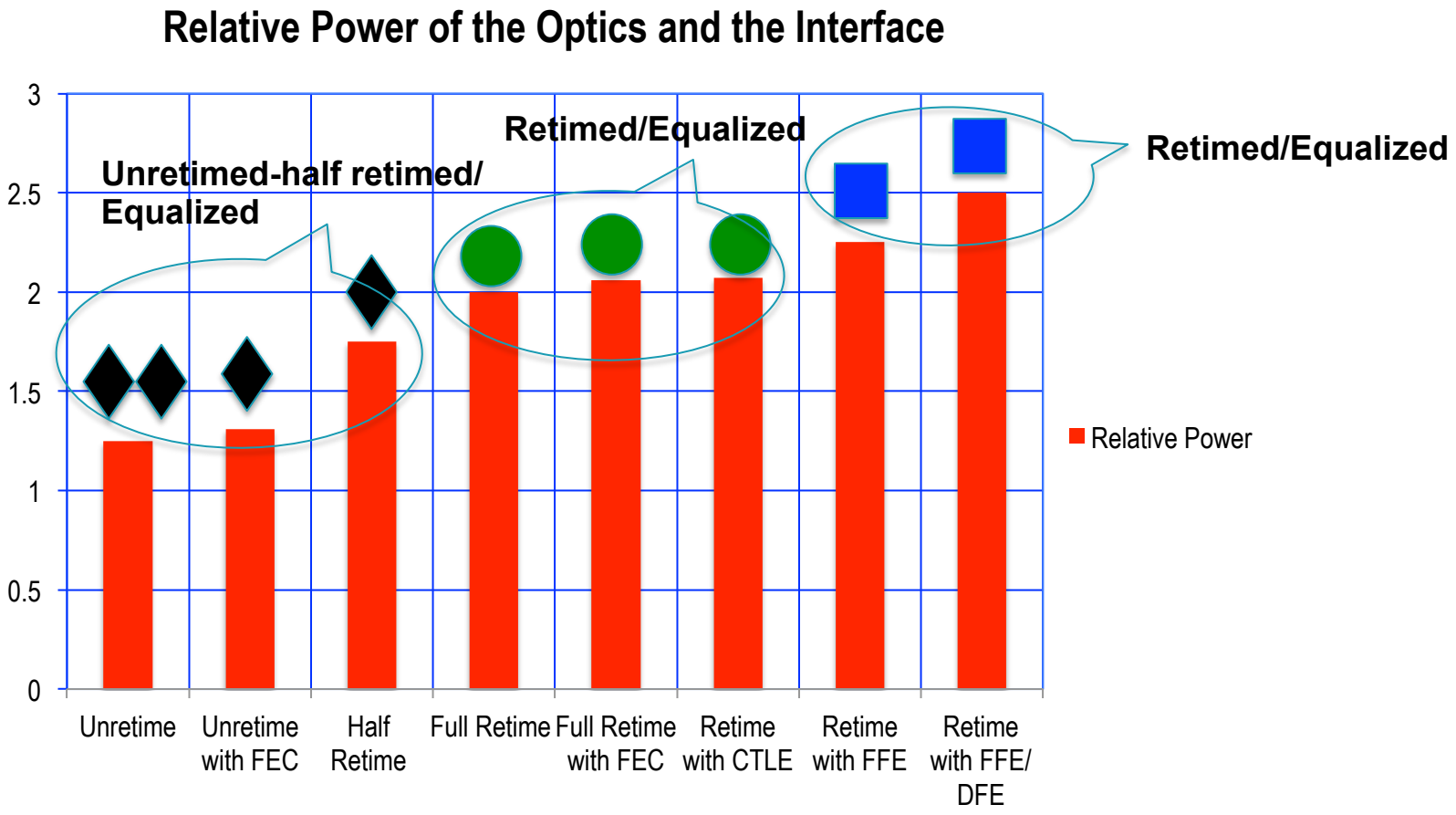


index	..._EQ.WidthAtBER)	...EQ.HeightAtBER)
0.000	2.938E-11	0.286



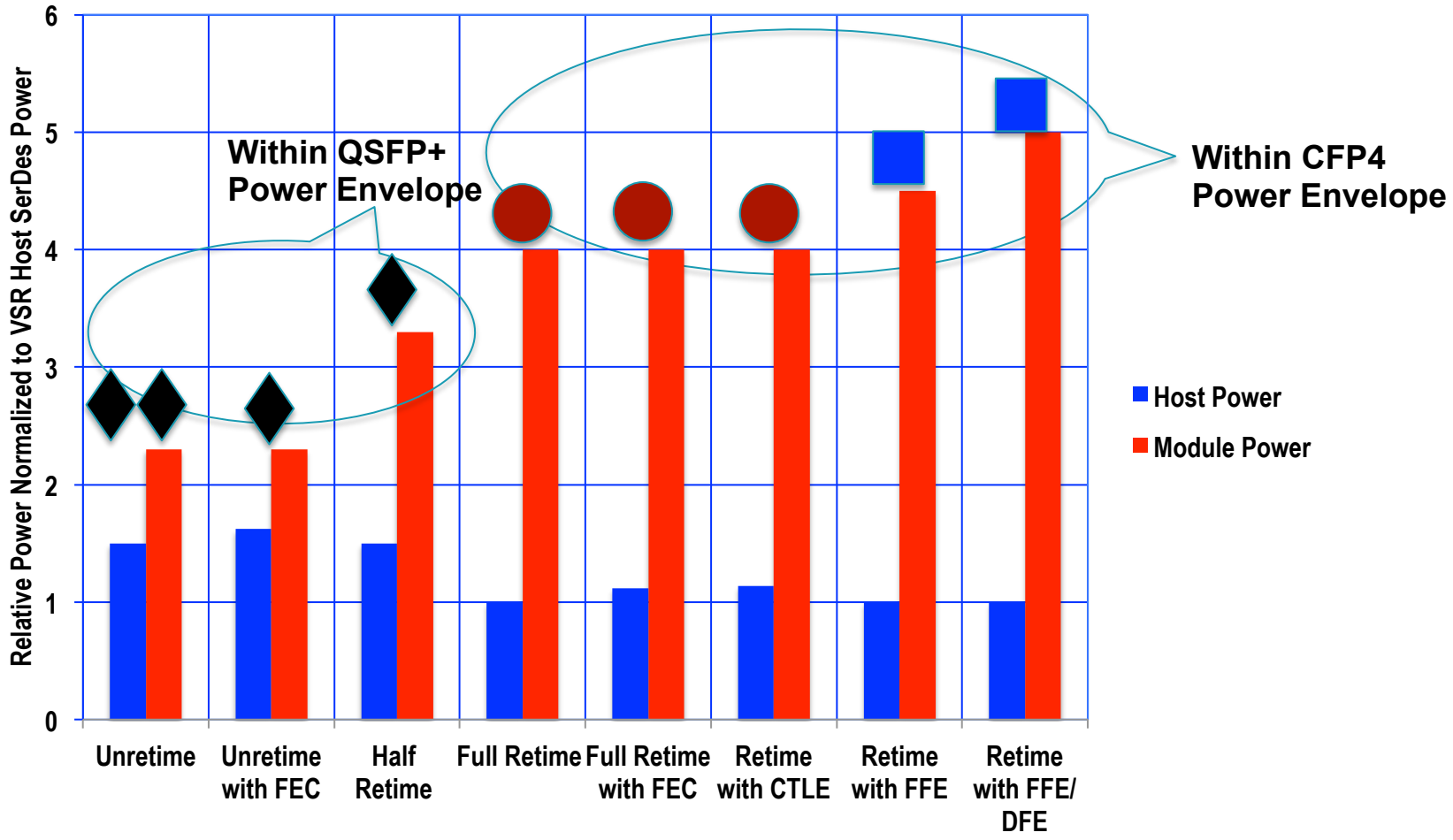
Solution Power Consumption

- Relative power include any host EQ power premium above VSR SerDes
- Alpine ski trail marking is used to show complexity of each solution



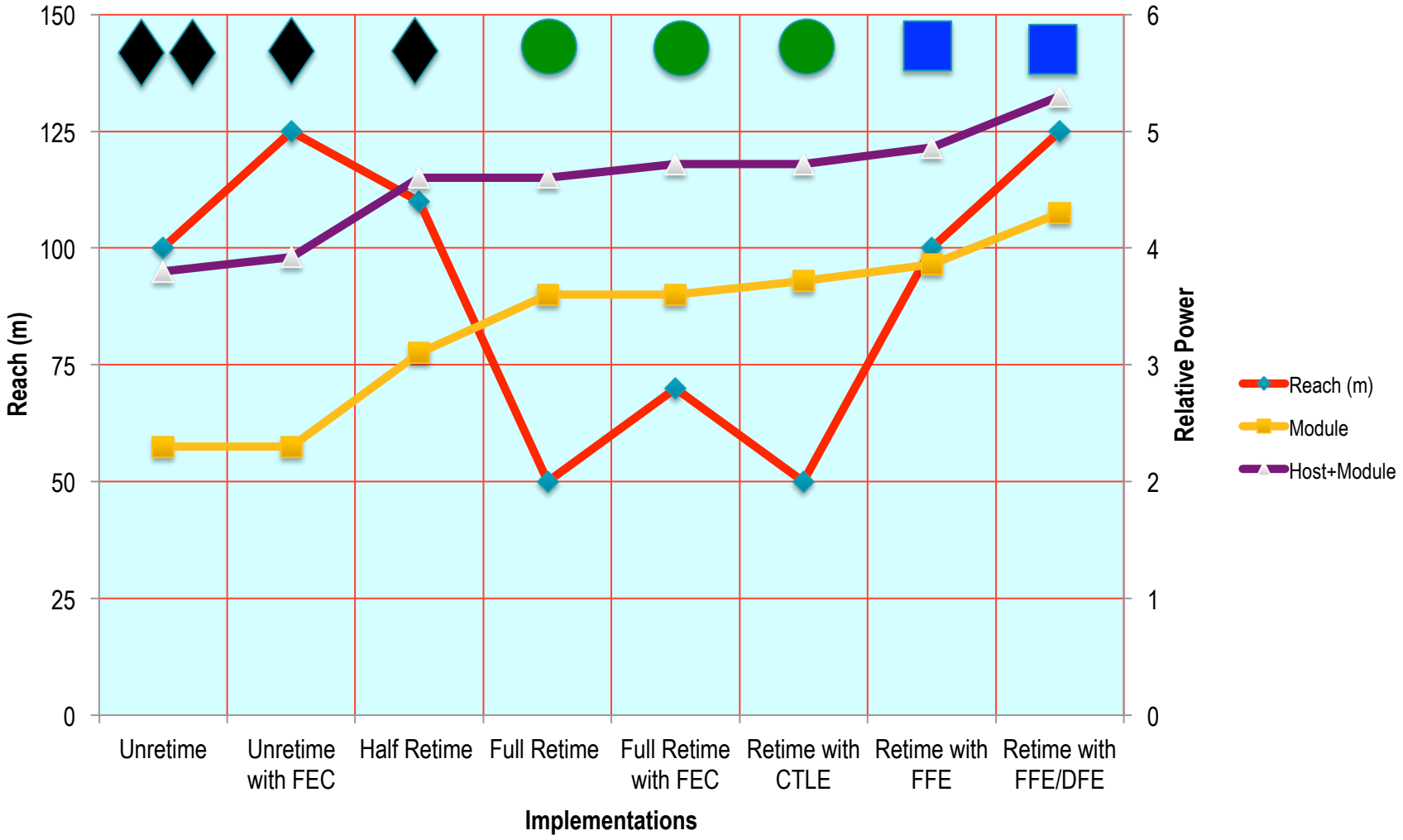
Power Comparisons

- Relative power include any host EQ power premium



Reach and Host/Module Implementations

- Fiber Reach assumes OM3



Summary

- **Measured and simulated VCSEL results show feasibility of unretimed cPPI-4 interface based on modest host EQ of 6-T/2 FFE+3 DFE**
  - Please see ghiasi_01_0112 and ghiasi_02_0112
  - Host EQ not only makes cPPI-4 feasible but also can address VCSEL slow fall time, Chromatic dispersion, photo detector capacitance, and meet full 100 m on OM3 or 150 on OM4
- **Link could operate to full 100 m of OM3 without FEC addressing latency sensitive applications as well**
  - Need to quantify the MPN penalty at these longer reach with equalized receiver
- **The unretimed 25G link link will have the lowest cost, power, and size as SFP+ has shown at 10G**
- **Do not see any significant power or cost saving between 30 m vs 70 m retimed solution**
- **The unretime/half retime are more complex to define and require more focus effort, even if we don't define it in 100GNGOPTX we should take advantage of EQ to facilitate VCSEL/PD impairments and support full 100 m on OM3 or 150 m on OM4.**