

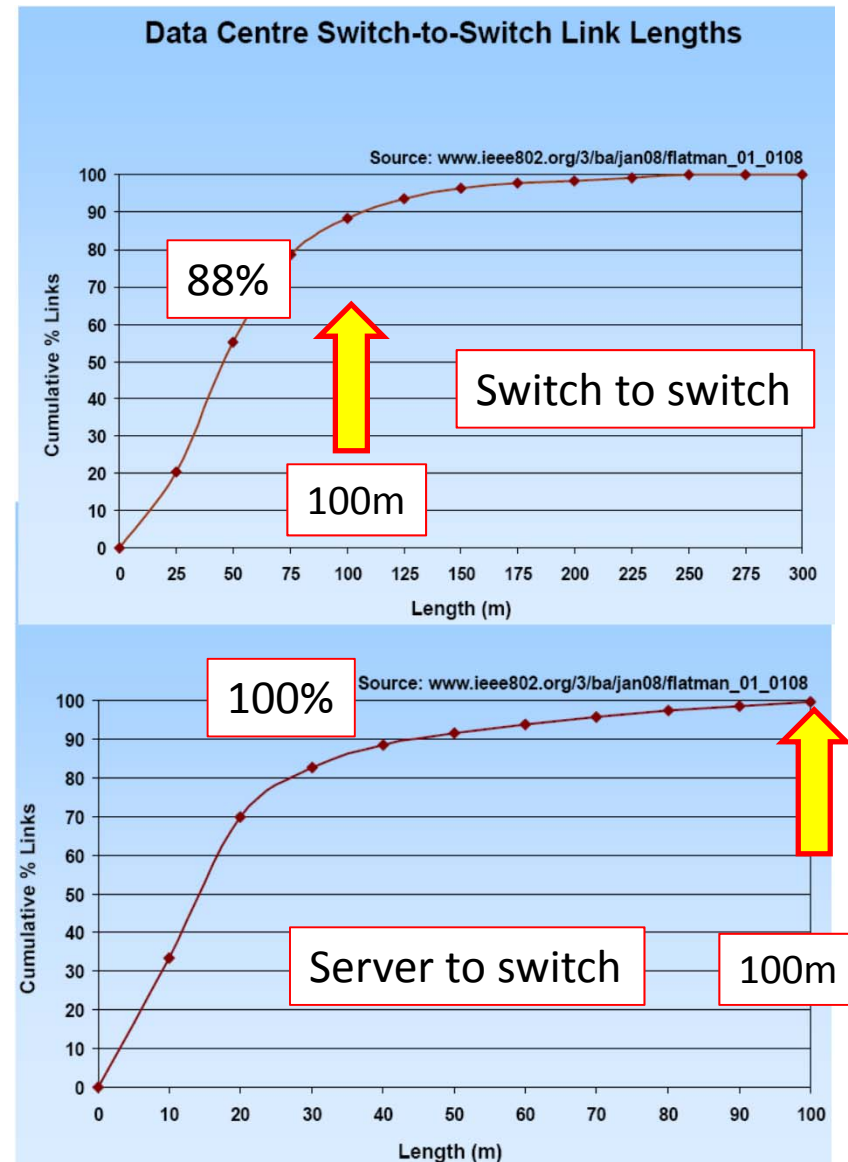
Supporting material for a 100Gb/s MMF objective

24th January 2012

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Applications - recap

- Data Center link lengths
 - 100 m covers ~90% of switch to switch links
 - 100% of server to switch links
 - **Flatman_01_0911**
 - **Kolesar_01_0911**: good agreement for single link length distribution
 - Andy Moorwood, Infinera: “10’s of metres, weighted to low end... 100m reach on MMF may be good enough”
 - **From “Intra and Inter Rack Connectivity Requirements”, OIF Workshop January 16th 2012**
 - Mark Nowell, Cisco: “... at least 100m on latest multi-mode fibre”
 - Q&A after presentation of **Nowell_01_0911**
- Fiber Channel objective: 100m on OM4
 - Higher rate, but single channel
- HPC/server environment: <50-75m
 - **Pepeljugoski_01_1111**



Technical feasibility – recap

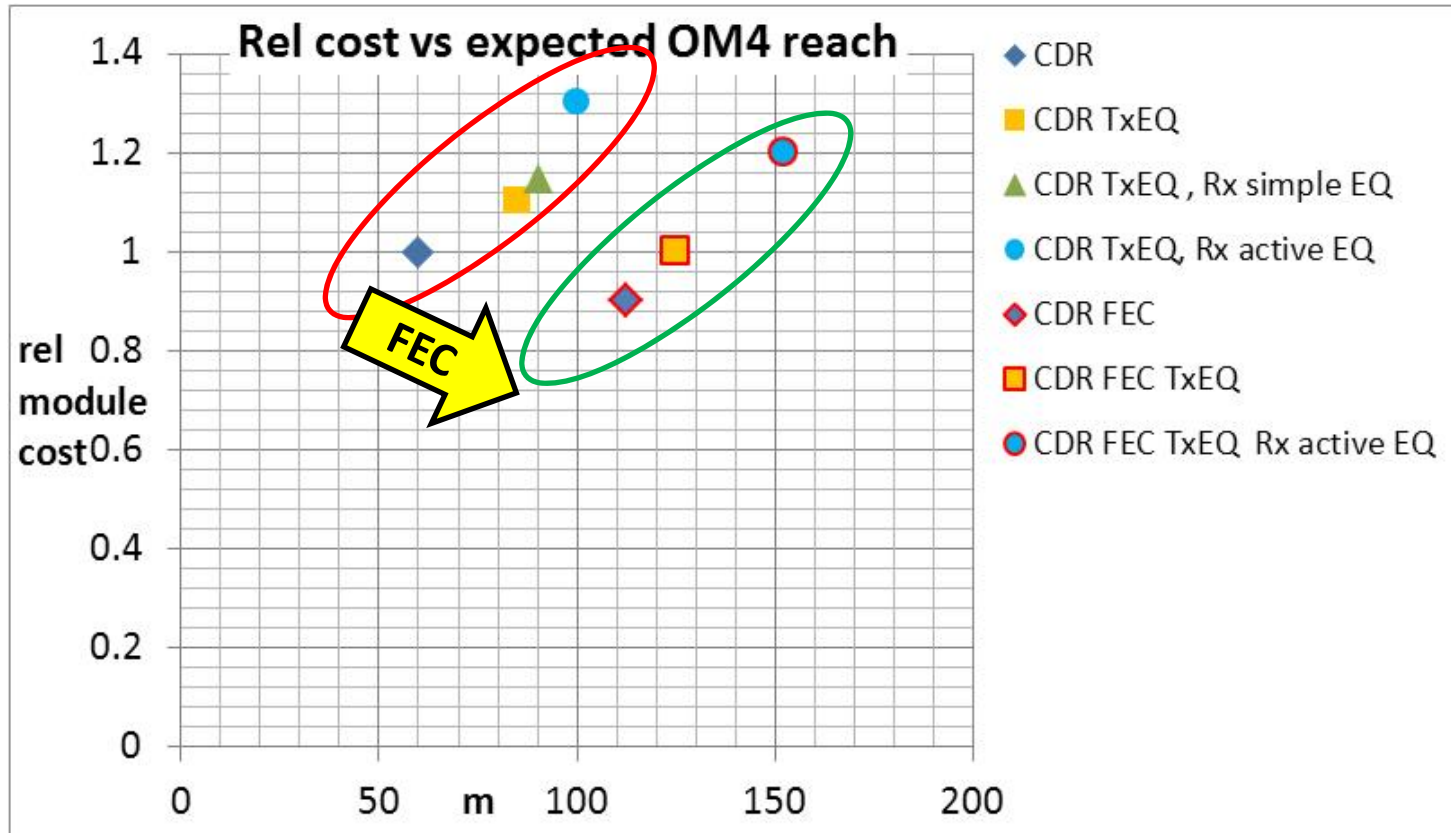
- VCSEL performance
 - Link budget modeling, using anticipated 25G VCSEL Tx and Rx and characteristics, and a fully retimed module, predicts
 - with FEC: 100m to 150m on OM4
 - without FEC: from 50 to 70m on OM4 for a simple retimed module
 - » Up to 70 to 100m on OM4 with simple Tx and Rx EQ, but with higher cost and power compared to a FEC enabled module
 - Similar reach expectations in ***King_01_1111*** and ***"100G Next Gen SR4 vis-à-vis SR10", John Petrilla***
 - If VCSEL performance ends up at worst case expectations, we have these low power (~30mW/channel) performance enhancements to fall back on inside the module:
 - Simple equalization in optical Tx chain may enable 1 to 1.5 dB lower Tx penalties
 - Simple (fixed) Rx chain 'peaking' or CTLE may enable 1 to 1.5 dB of SRS improvement for worst case channel, depending on Tx characteristics

Technical feasibility - measurements

- 25G receiver results
 - 100GBASE-LR4
 - *Jiang_01_0911*
- 25G VCSEL results
 - This meeting: ***“Measured Results of 25.78G VCSEL over OM3 Fiber with and Without Equalization”, Ali Ghiasi et al***

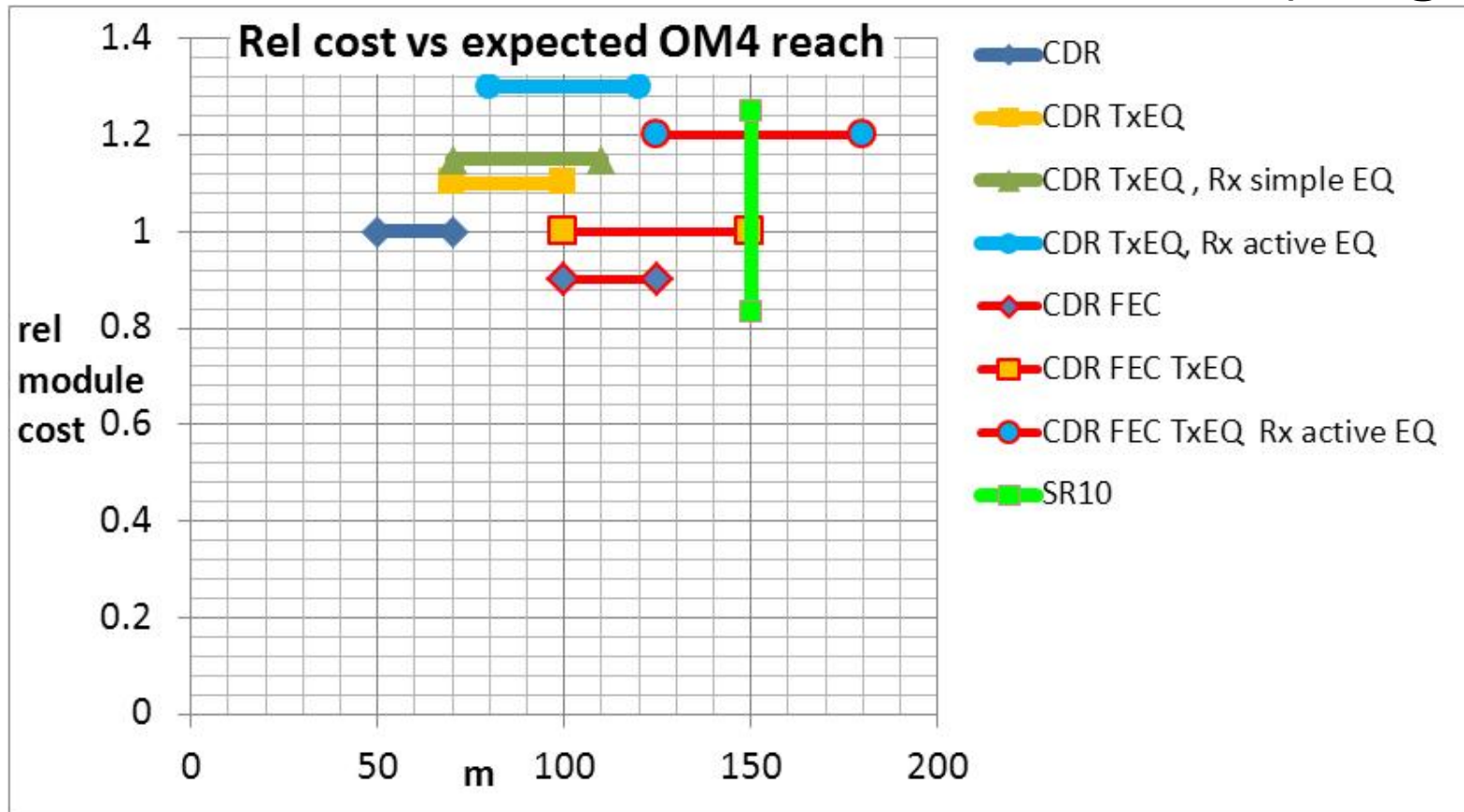
Relative cost and power estimates vs reach

Estimated relative module cost vs reach



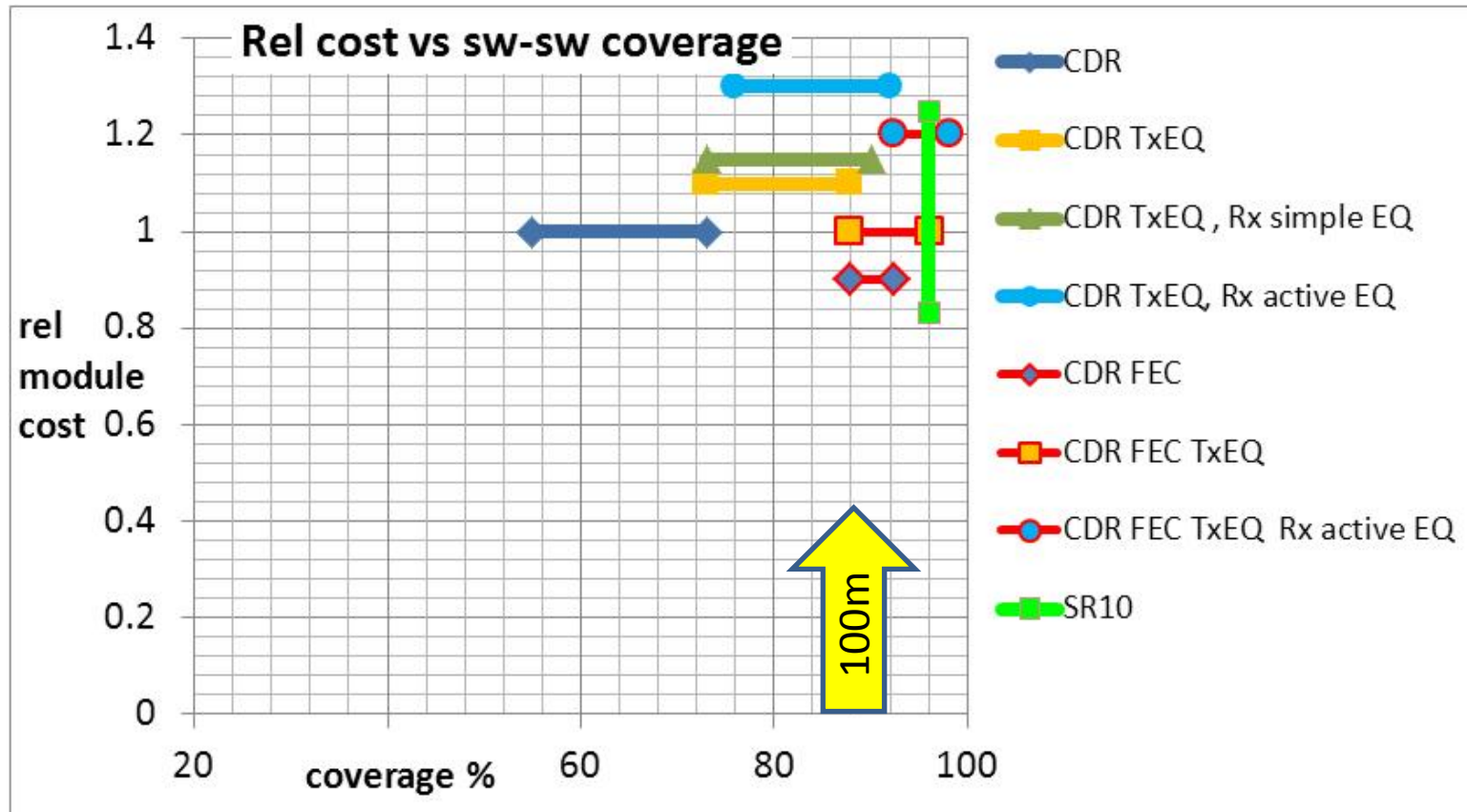
- Expected reach numbers based on *King_01_1111* , approximate cost numbers based on estimated set up and test time. Where a range of reach values were estimated (eg for slow or fast rise times) a mid point was taken.
- (slide from “*MMF-ad-hoc-mid-term-review*” in MMF ad hoc materials archive)
- Noted: FEC is a very cost effective performance enhancer

Estimated relative module cost vs reach (ranges)



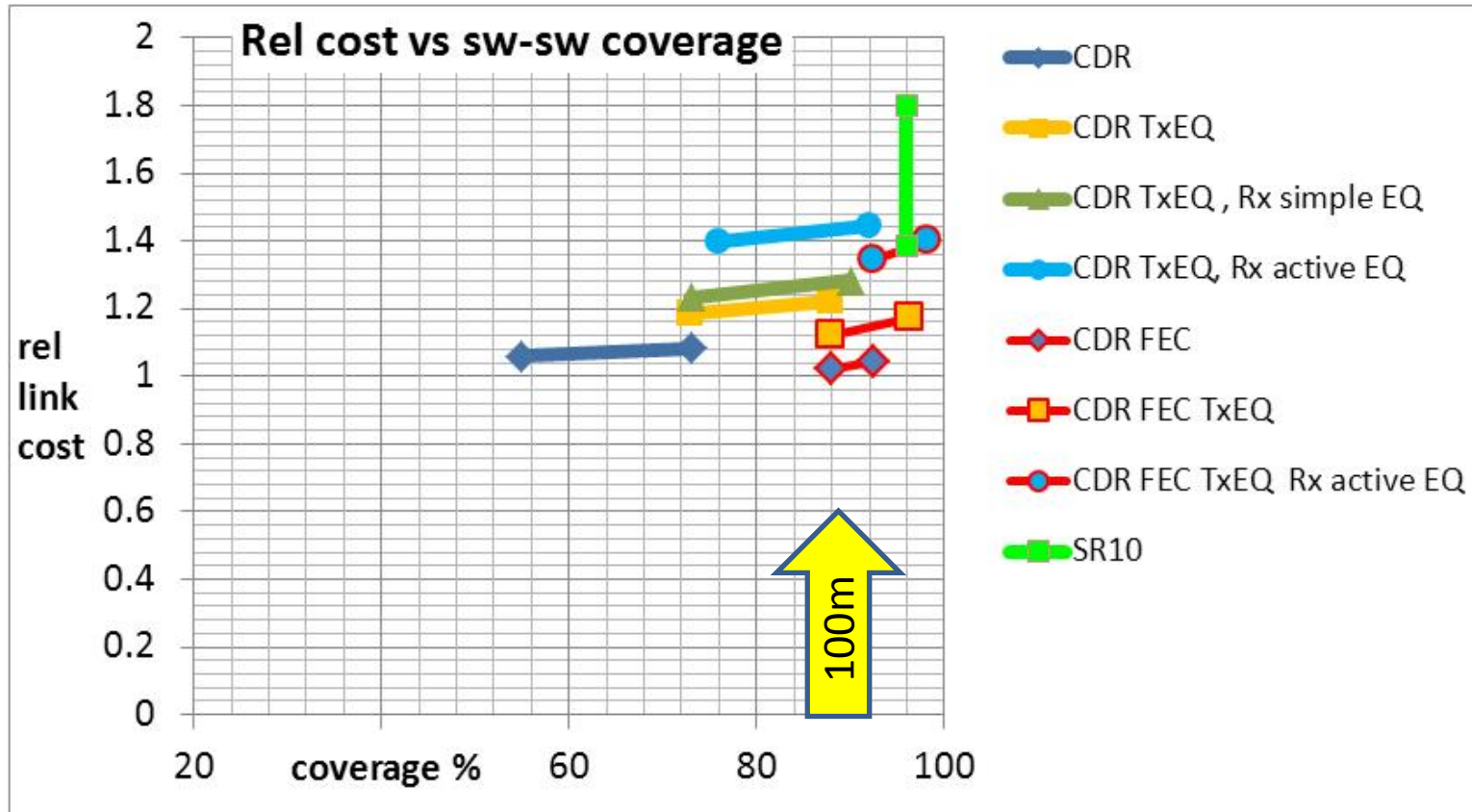
- Same reach numbers based on *King_01_1111* , but range of reach values plotted (for slow or fast VCSEL rise times); approximate cost numbers based on estimated set up and test time .
- Relative cost of 100G-SR10 added (high and low estimates are consistent with **"100G Next Gen SR4 vis-à-vis SR10"** by *John Petrilla* (MMF ad hoc materials archive) and estimated relative module cost 100G-SR10 vs 100G-SR4 included in back up slides in this presentation.

Estimated relative module cost vs coverage



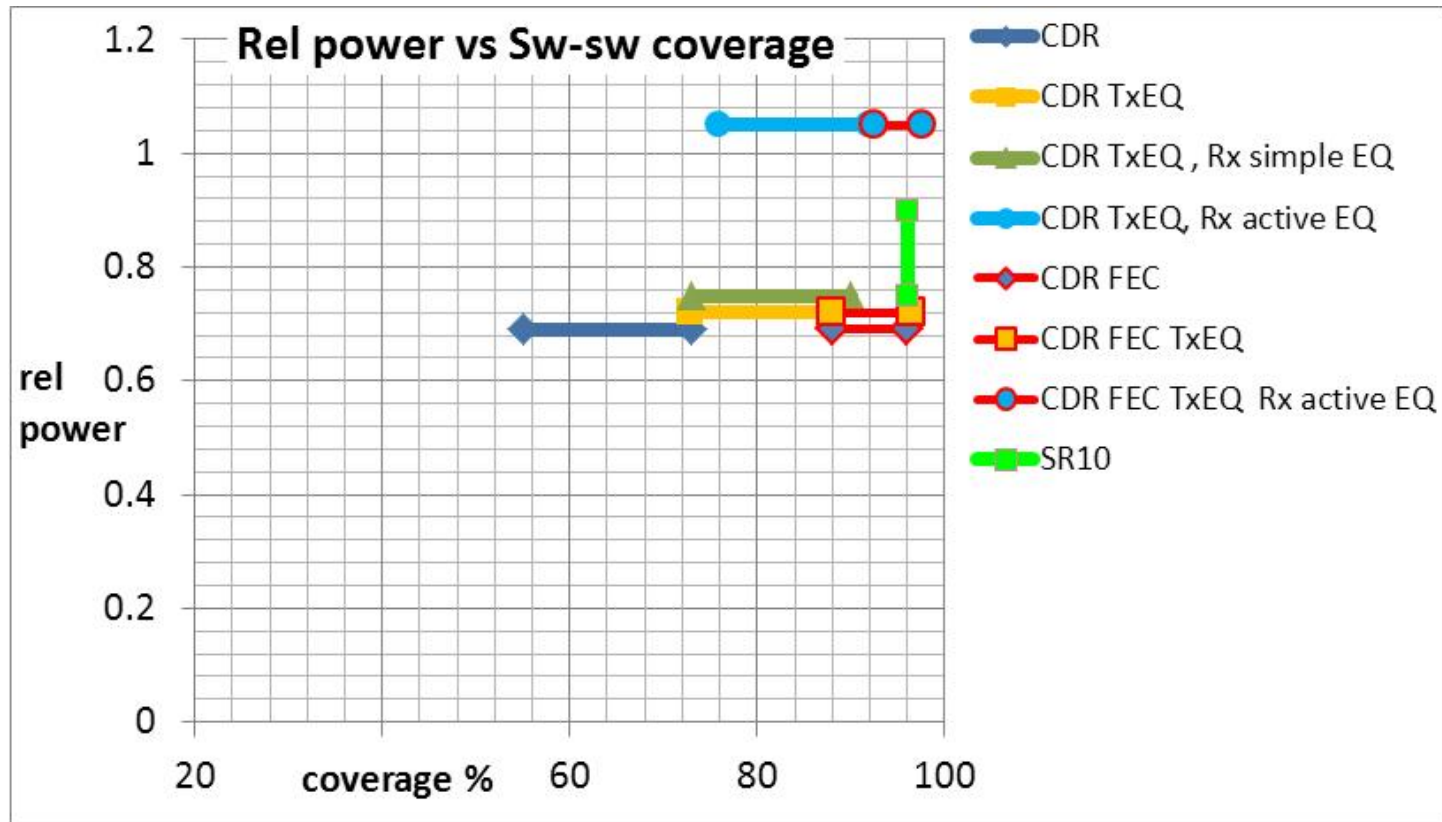
- Same examples, but plotted against % coverage of switch to switch links (*Flatman_01_0911*)
 - Relative cost of fibres and connectivity not included (i.e. = '0')
 - Relative module cost of SR4 and SR10 is similar

Estimated relative link cost vs coverage



- As previous slide, but attempting to include the cost of connectivity
 - relative total link cost estimated from **“Low Cost 100GbE Links” by Scott Kipp (Brocade), Doug Coleman and Steve Swanson (Corning) (Kipp_01_0112)**
 - Assuming (SR4 module cost + connection)=(SR10 module cost + connection) = 1 at 0 metres of fibre
 - Relative fibre cost vs distance for SR10 is 3x that of SR4
- Lower fibre count and higher faceplate density make SR4 attractive cf SR10

Relative module power vs coverage



- Coverage and power are similar for FEC enabled SR4 and SR10
 - Relative power of SR4 variants and SR10 consistent with ***"100G Next Gen SR4 vis-à-vis SR10"*** by John Petrilla, and ***King_01_1111***

Strawman objective for 100GBASE-SR4

- “Define a FEC enabled 4-lane 100 Gb/s PHY for operation over MMF with reach up to at least 100m”
- Wide range of applications
 - 100m reach meets requirements of the data center, HPC cluster connections, symbiotic with Fiber Channel objectives
- Technically feasible
 - Several known low power techniques available to help achieve the distance.
- Economically feasible
 - Lowest cost, highest performance SR4 module will be enabled by FEC
 - Lower system cost because fibre count significantly less than 100GBASE–SR10
- Distinct from 100GBASE-SR10
 - 4-lane wide 100Gb/s electrical interface – lower system cost because faceplate density can be significantly higher than 100GBASE–SR10

Back up

FEC vs non FEC: 20 ps VCSEL effective rise time

Rate/FEC	Reach limit definition	OM4 reach	Typ. latency: 50m fiber + FEC	Max. latency: max reach + FEC	Notes
25.8 GBd, no FEC	power budget	70 m	250 ns	350 ns	~2.5 dB VECP
25.8 GBd, high latency FEC	power budget	155 m	550 ns	1075 ns	high ~4.5dB VECP
25.8 GBd, high latency FEC	3.6 dB VECP	125 m	550 ns	925 ns	1.7 dB margin for spec relaxation
25.8 GBd, high latency FEC	3.0 dB VECP	100 m	550 ns	800 ns	2.6 dB margin for spec relaxation
28 GBd, low latency FEC	power budget	140 m	280 ns	730 ns	high ~4.8 dB VECP !
28 GBd, low latency FEC	3.6 dB VECP	100 m	280 ns	530 ns	2.0 dB margin for spec relaxation

From King_01_1111

FEC vs non FEC: 16 ps VCSEL effective rise time

Rate/FEC	Reach limit definition	OM4 reach	Typ. latency: 50m fiber + FEC	Max. latency: max reach + FEC	Notes
25.8 GBd, no FEC	power budget	100 m	250 ns	500 ns	~2.2 dB VECP
25.8 GBd, high latency FEC	power budget	170 m	550 ns	1150 ns	high ~4 dB VECP !
25.8 GBd, high latency FEC	3.6 dB VECP	155 m	550 ns	1075 ns	1.2 dB margin for spec relaxation
25.8 GBd, high latency FEC	3.0 dB VECP	135 m	550 ns	975 ns	2.2 dB margin for spec relaxation
28 GBd, low latency FEC	power budget	160 m	280 ns	830 ns	high ~4.5 dB VECP !
28 GBd, low latency FEC	3.6 dB VECP	135 m	280 ns	705 ns	1.7 dB margin for spec relaxation

From King_01_1111

Estimated relative module cost 100G-SR10 vs 100G-SR4

100G-SR10	Rel cost	100G-SR4	Rel cost
10G VCSEL	10x	25G VCSEL	8x
10G Driver	10x	quad 25G driver	8x
10G PIN-TIA	10x	quad 25G PIN TIA	8x
10 channel electrical input EQ's & line drivers	10x	4xCDR pairs and electrical input EQ & line drivers (integrated with quad driver)	8x
10 channel testing	~10x	4 channel testing	~6x
PCBA and shell	1x	PCBA and shell	2x
Weighted relative cost	~10x		~ 8x

Cost of CDRs is a fraction of the total IC cost, and a relatively small fraction of total cost