Feasibility of Transimpedance Amplifiers and CDRs for PAM Modulation

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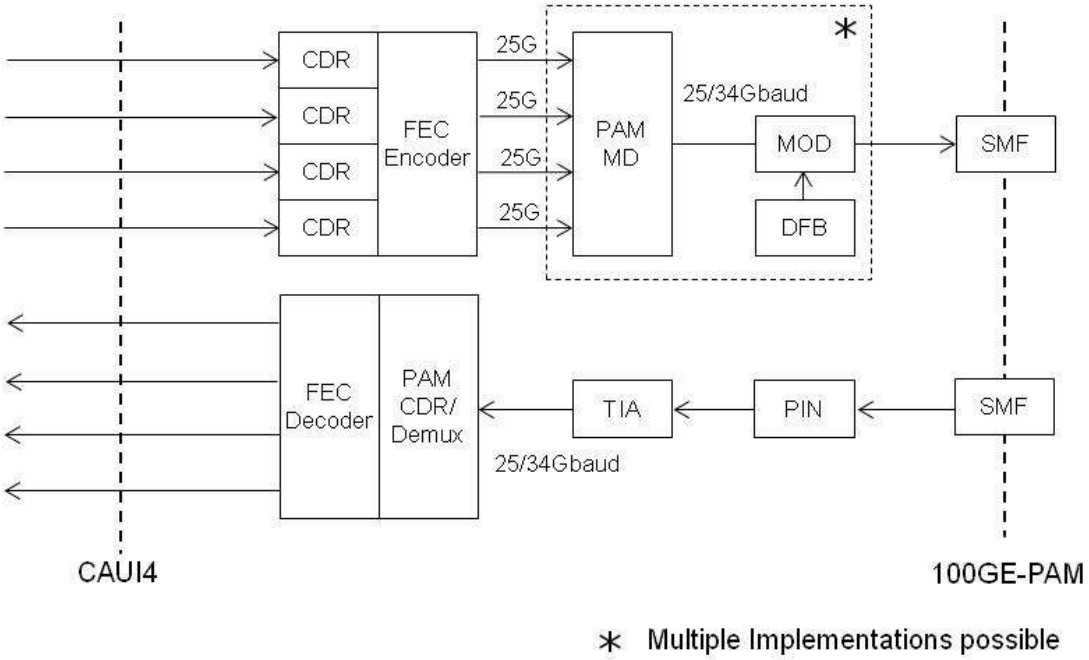
Introduction

- PAM modulation with a single laser has potential to significantly reduce cost over 100GBASE-LR4
- Linear transimpedance amplifiers and PAM-N CDRs are key components required for the receiver
- This work investigates the feasibility of these components

PAM-N Transceiver



- Linear TIA and PAM-N CDR are key components in the PAM-N receiver
- Important TIA parameters are gain, bandwidth, noise and linearity
- Analog and digital CDR architectures are feasible, with different tradeoffs

Linear Receiver Specs

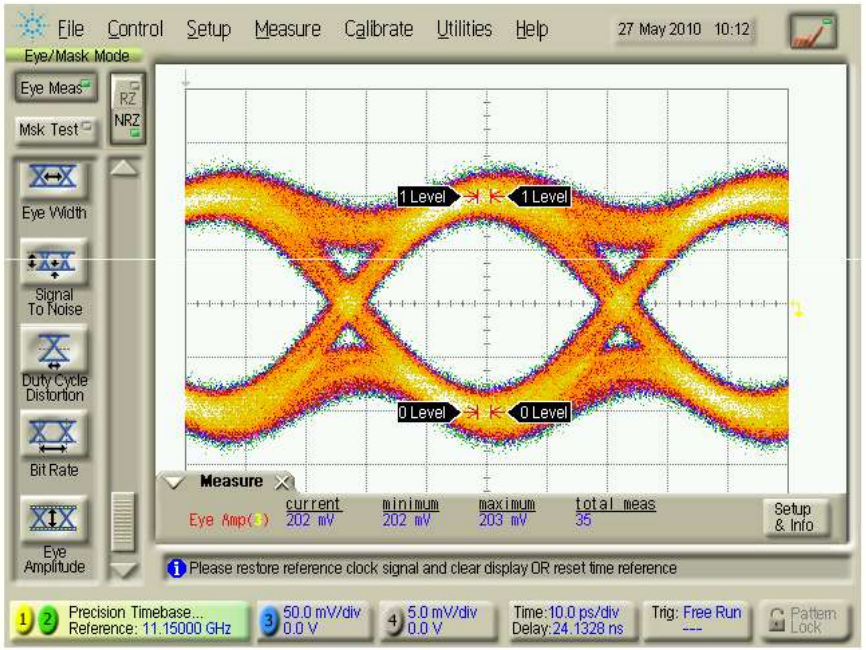
- Specs for linear receivers have been adopted at OIF for 32 GBaud QPSK systems[1]:

Parameter	Units	Min	Typical	Max
Linear Output Swing	mVppd	300	500	900
3dB Bandwidth	GHz		22	
THD	%			5
AGC Bandwidth	MHz		5	

- Additional parameters such as noise, gain ripple, phase ripple etc are also important to PAM-8/16
- Compliant receivers with linear TIAs are commercially shipping today

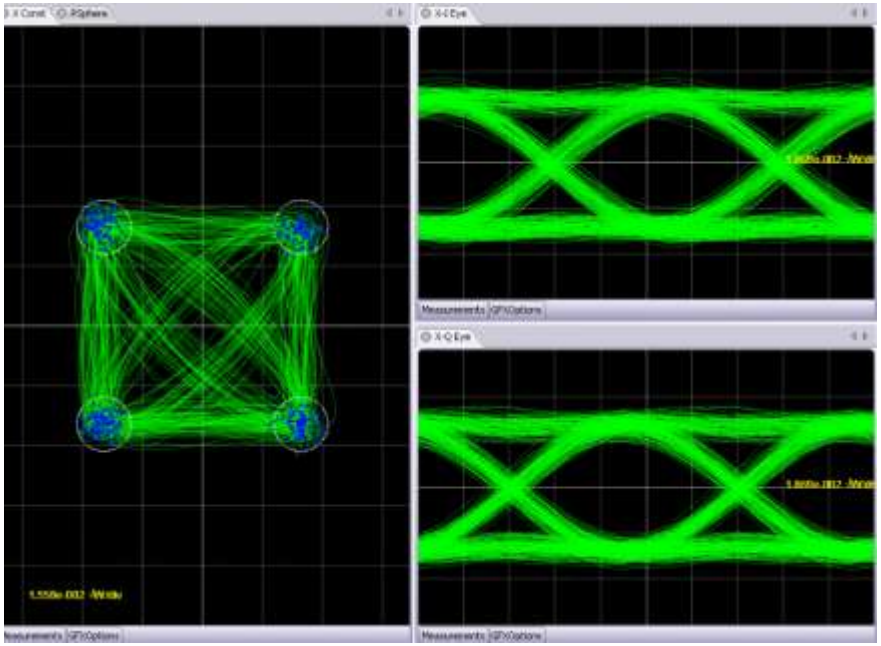
[1]Optical Internetworking Forum, "Implementation Agreement for Integrated Dual Polarization Intradyne Coherent Receiver," April 16, 2010, IA # OIF-DPC-RX-01.

Linear Receiver Examples



Source: Inphi

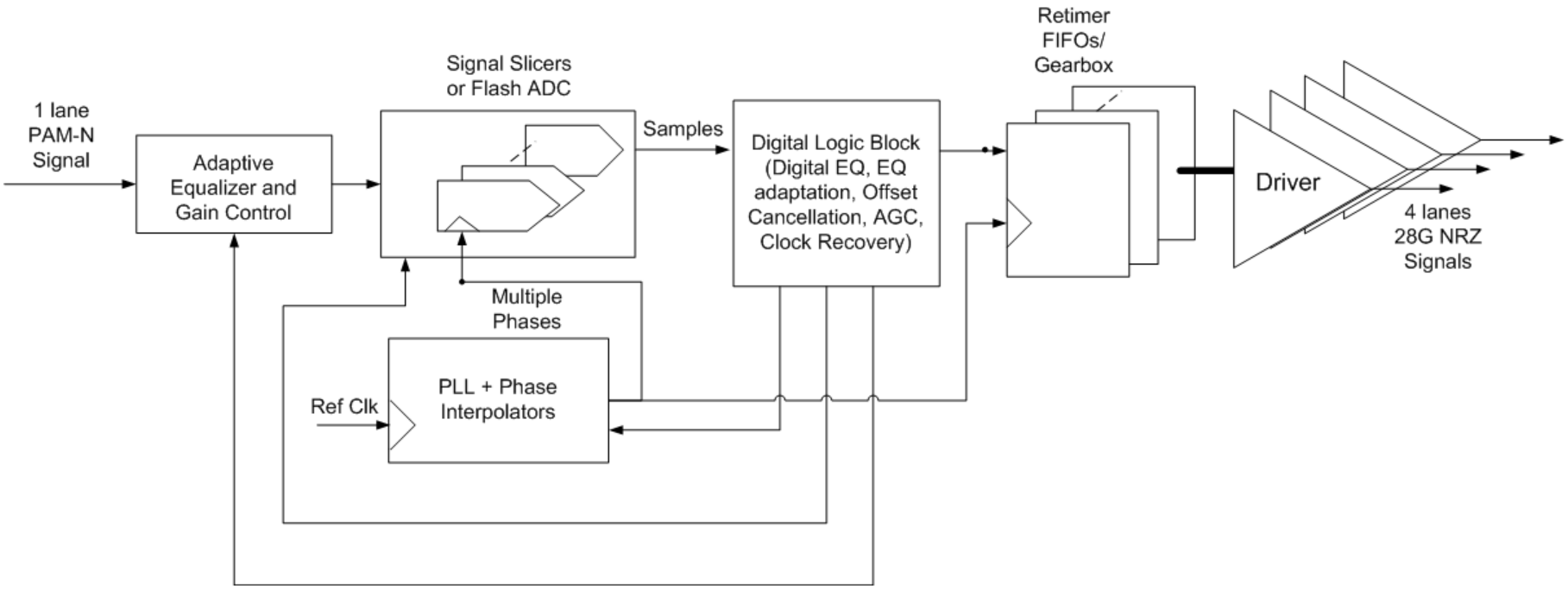
DQPSK Eye (22.3 GBaud)



Source: Inphi and Optametra (now Tektronix)

Coherent QPSK (30 GBaud)

PAM-N Rx CDR Block Diagram



- Analog and digital CDR architectures are feasible, with different tradeoffs
- 10G ADC-based SerDes have been available for ~5 years; similar techniques can be used at higher rates for PAM signaling

Feasibility of PAM-8/16 Rx CDRs

- Examples of CDR technologies
  - A 22 Gb/s PAM-4 receiver at 228 mW in 90 nm CMOS was presented in 2006[1]
  - A 12.5Gb/s NRZ Tx/Rx SerDes at 330mW in 65nm CMOS using baud-rate 4.3 Bit ADC was presented in 2007[2]
  - Multiple announcements of commercial 4x25G NRZ CDR products were made in 2011
- Estimate for PAM-8/16 CDR power
  - Receiver CDR chip power is estimated based on 40nm CMOS process at TT, 85C, 1V supply condition.
  - Receiver CDR includes one PAM-8/16 input lane and four NRZ output lanes.
  - No FEC functions are included in the power estimates.

100 Gbps RX CDR Power Estimates					
Input Signaling	Input Data Rate (GSymbols/s)	Input Bits/Symbol	Number of RX Lanes	Number of TX Lanes @28G	Total Power (Normalized to NRZ power)
NRZ	25	1	4	4	100%
PAM-8	34	3	1	4	~80%
PAM-16	25	4	1	4	~85%

[1] T. Toifl et al., “A 22-Gb/s PAM-4 Receiver in 90-nm CMOS SOI Technology”, IEEE JSSC, Vol. 41, No. 4, April 2006
[2] M. Harwood et al., "A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital Receiver Equalization and Clock Recovery," 2007 IEEE International Solid-State Circuits Conference, ISSCC 2007, Digest of Technical Papers

Summary

- Linear receivers at 32 GBaud/s for coherent QPSK systems are commercially shipping today
- Power consumption for PAM-N CDRs appear to be in line with NRZ CDRs
- Overall, feasibility for linear TIAs and PAM-N CDRs appears promising, and merits further investigation